

# SIEMENS

## ICs for Consumer Electronics

### MEGATEXT

Sync Applications

Edition 10.94

<b>MEGATEXT® Sync Applications</b>	
<b>Revision History:                      Original Version 10.94</b>	
Previous Releases:	
Page	Subjects (changes since last revision)

## Data Classification

## Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

## Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25\text{ °C}$  and the given supply voltage.

## Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about “**Processing Guidelines**” and “**Quality Assurance**” for ICs, see our “**Short Form Catalog**”.

## Edition 10.94

This edition was realized using the software system FrameMaker®.

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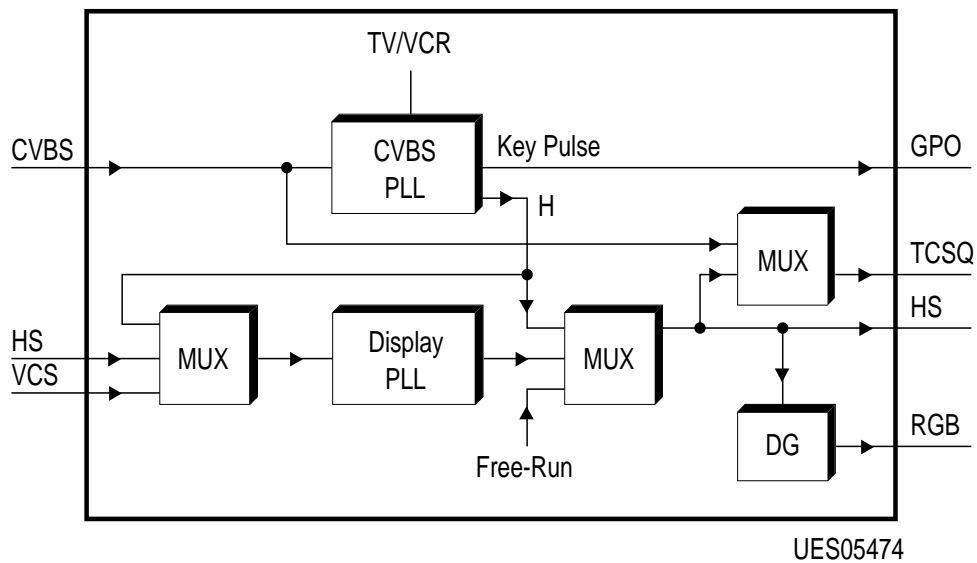
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### PLLs of MEGATEXT®: Main Interconnections



	R 114	R 113	
Signal Input	DPLL Lock	DSL SRC 1	DSL SRC 0
A	x	1	1
B	x	0	0
C	x	0	1
D	0	1	0
E	1	x	x
F	0	0	

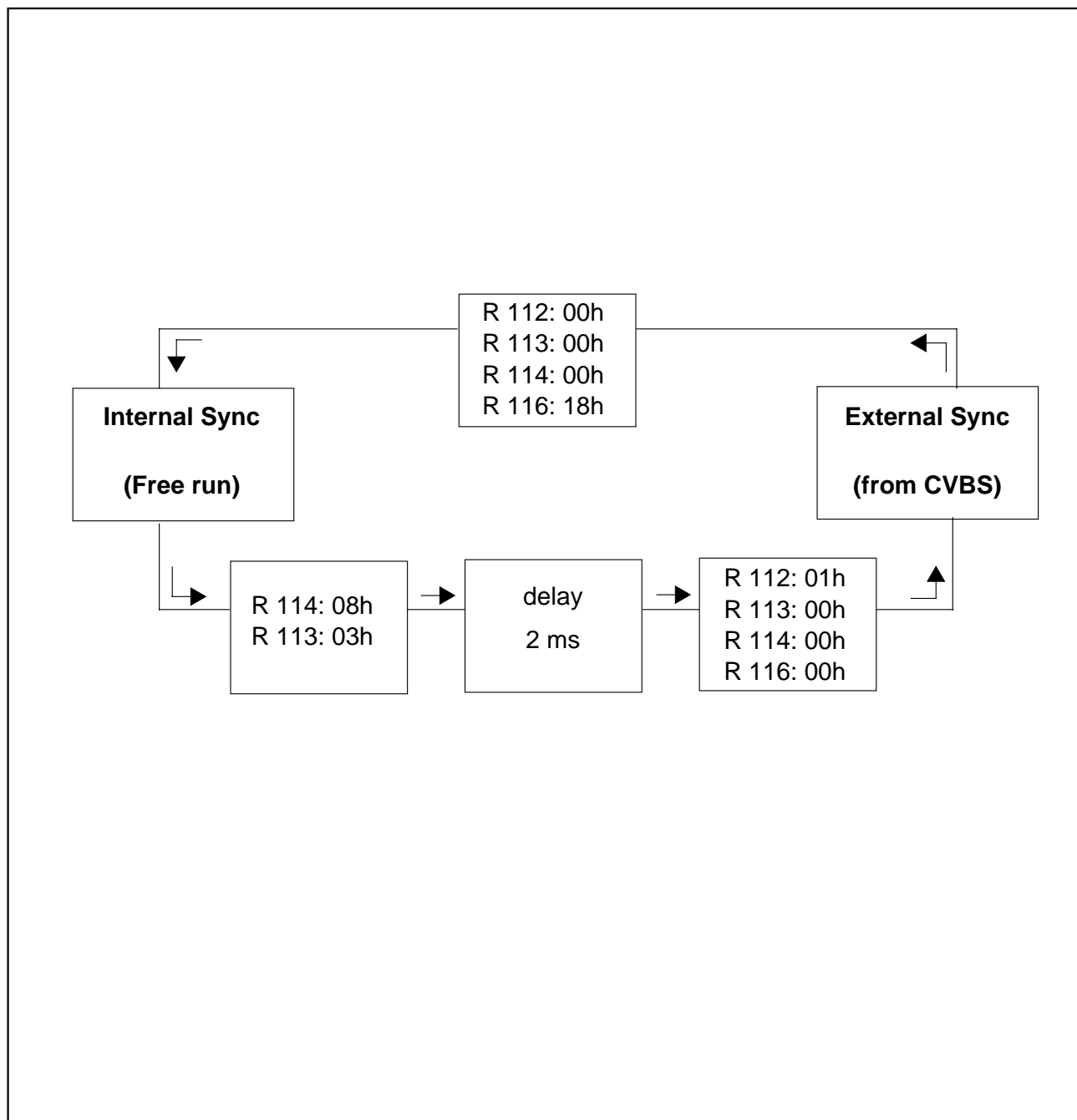
Pin Name	I/O	Function	Remarks
CVBS	input	CVBS	V <sub>pp</sub> = 0.6 V ... 2.0 V
GPO	output	burst gate pulse	TTL level
	output	or static 0, 1 or tristate	for general control purposes
TCSQ	output	H/V composite sync	H pulse is negativ, TTL level, open Drain
	output	or CVBS	amplitude like CVBS-input/ DC-sync level is app. 1 V
HS	input	external H-pulse	rising edge is start of line
	output	or H output	positive pulse 2 µs TTL level
VS/VCS	input	external H/V comp. sync	H pulse is positiv, TTL level
	input	or external V	V pulse is positiv, TTL level
	output	or V	V pulse is positiv, TTL level

### Changing the Sync Mode

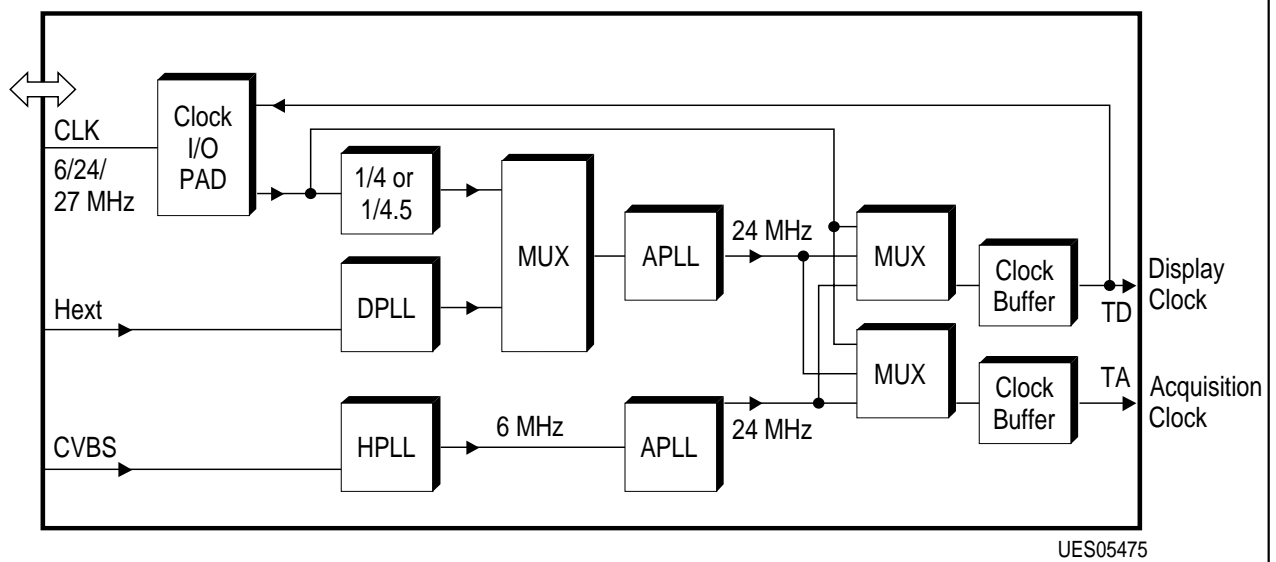
For changing the sync mode, following sequence is recommended.

It is not allowed to switch the input of the display generator directly to the output of the CVBS PLL. Phase differences between the freerun H pulse and the CVBS signal may generate data losses in the memory. So it is useful to connect both PLL's in series to have a smooth lock in.

As this mode generates more jitter, the Display PLL should be bypassed after the delay time.



**MEGATEXT® Clock Source Selection**



**Clock Source Selection Overview**

### Selection of Display Sync Sources

Application	ACQ-Clock Source	Display Clock Source	R112
Standard	CVBS	HS/VCS	xxxxx000
Possible if acquisition and display have the same CVBS-source	HS/VCS		xxxxx010
	CVBS		xxxxx001
Special applications	CVBS	extern	xxxxx100
	extern		xxxxx110

Application	ACQ-Sync Source	Display Sync Source	R112 R113 R114
Standard	CVBS	HS/VCS	xxxxx000 xxxxxx0x xxxx1xxx
Possible if acquisition and display have the same CVBS-source	CVBS	HS/VCS	xxxxx010 xxxxxx0x xxxx1xxx
	CVBS		xxxxx001 xxxxxx01 xxxx0xxx
Display forced to an external clock	CVBS	free	xxxxx100 xxxxxx00 xxxx0xxx
Acquisition and display forced to an external clock	CVBS	free	xxxxx110 xxxxxx00 xxxx0xxx



### Forbidden Combinations of Clock and Sync Source Selection

	R112	R113	R114
Forbidden	xxxxx1xx	xxxxxxx01 or xxxxxxx10 or xxxxxxx11	xxxx0xxx
Forbidden	xxxxx010	xxxxxxx1x or xxxxxxx1	xxxx0xxx
Forbidden	xxxxx0x1	xxxxxxx1x	xxxx0xxx

There are forbidden combinations of clock source selection and sync modes. They may lead to a PU “run away” and have to be avoided as intermediate states when changing the clock or sync source.

### MEGATEXT® Synchronization Modes

#### MEGATEXT® as Display Sync Master / Freerun Modes

##### Outputs

- H: pulse width typ. 2  $\mu$ s in 15.6-kHz modes  
pulse width typ. 2  $\mu$ s in 31.2-kHz modes  
rising edge is sync reference
- V: pulse width typ. 1 line non-interlaced in fly wheel mode  
pulse width typ. 1.5 line at interlace point  
rising edge is sync reference
- TCSQ: falling edge is sync reference  
for waveforms please refer to IC data sheet

### Freerun modes (values for 20.5-MHz crystal)

Mode	Vertical Output Frequency	Horizontal Output Frequency	Lines per Field	TCSQ Out
F1	50 Hz	15.625 kHz	313/312	H- and V-component
F1N	60 Hz	15.750 kHz	263/262	H- and V-component
F2	50 Hz	15.625 kHz	312/312	H- and V-component
F2N	60 Hz	15.750 kHz	262/262	H- and V-component
F3	50 Hz	15.625 kHz	312.5/312.5	H- and V-component
F3N	60 Hz	15.750 kHz	262.5/262.5	H- and V-component
F4	100 Hz	31.25 kHz	313/312	H- and V-component
F4N	120 Hz	31.50 kHz	263/262	H- and V-component
F5	100 Hz	31.25 kHz	312/312	H- and V-component
F5N	120 Hz	31.50 kHz	262/262	H- and V-component
F6	100 Hz	31.25 kHz	312.5/312.5	H- and V-component
F6N	120 Hz	31.50 kHz	262.5/262.5	H- and V-component
F7	50 Hz	31.25 kHz	625/625	only H-component
F7N	60 Hz	31.50 kHz	525/525	only H-component

### Important control bits of MEGATEXT bus registers for sync adjustment:

Mode	Register Control Bits	
F1 ... F7N	R116	Freerun mode selection
F4 ... F6	R114	DPLL 100 Hz = 1
F7, F7N	R114	DPLL 2HS = 1
		(alternatively HALF DLC = 1, DPLL 100 Hz = 1)

The display/pixel clock and the horizontal frequency are proportional to the crystal frequency.

### MEGATEXT® as Display Sync Slave

Synchronization on HS, VS/VCS input signals

Input signals:

- H: rising edge is sync reference  
200 ns minimum pulse width  
15.6 kHz  $\pm$  10 % (with 20.5-MHz XTAL)  
31.2 kHz  $\pm$  10 % (with 20.5-MHz XTAL)
- V: rising edge is sync reference  
200 ns minimum pulse width
- VCS: rising edge is sync reference  
for waveforms please refer to the IC data sheet

For norm sync input signals supported by freerun modes the fly wheel can be used for vertical stabilization. For out-of-norm sync input signals vertical filter circuits have to be adjusted or switched off. TCSQ is only valid for norm signals supported by freerun modes. In other cases TCSQ contains no vertical component. Doublification of vertical display frequency (sync mode SL3) is possible only for 50-/60-Hz sync formats supported by MEGATEXT freerun modes (e.g. 50-Hz/15.6-kHz input, 100-Hz/31.2-kHz display).

Mode	Input	Vertical Display Frequency	Horizontal Display Frequency	Lines per Field
SL1-HV SL1-VCS for progressive line scan:	H/V VCS	like VS like VCS	like HS like VCS	like VS like VCS
SL2-HV for progressive field scan:	H/V	like VS	2 $\times$ HS	like VS
SL3-HV	H/V	2 $\times$ VS	2 $\times$ HS	2 $\times$ VS

### Important control bits of MEGATEXT bus registers for sync adjustment:

Sync Mode	Register Control Bits	
SL1 ... SL2	R113 R116	sync source selection freerun mode selection
SL2	R114	DPLL 2HS = 1
SL3	R114	DPLL 100 Hz = 1

The centre frequency of the horizontal PLL is proportional to the external crystal frequency.

### Sync Separation from CVBS

CVBS-input signals:

- H: 15.6 kHz  $\pm$  5,3 % (with 20.5-MHz XTAL)
- V: – norm signals with 50 Hz, 60 Hz (PAL, NTSC, SECAM)  
 – out-of-norm signals with 5 ... 511 lines per field

Mode	Vertical Output Frequency	Horizontal Output Frequency	Lines per Field
For standard displays (e.g. 50 Hz, 15.6 kHz) C1	like CVBS	like CVBS	like CVBS
For double line displays (e.g. 50 Hz, 32 kHz) C2	like CVBS	2 $\times$ CVBS	2 $\times$ CVBS
For double field displays (e.g. 100 Hz, 32 kHz) C3	2 $\times$ CVBS	2 $\times$ CVBS	2 $\times$ CVBS

Doublication of vertical display frequency (sync mode C3) is possible only for 50-/60-Hz sync formats supported by MEGATEXT freerun modes (e.g. 50-Hz/15.6-kHz input, 100-Hz/31.2-kHz display). TCSQ is only valid for norm signals supported by freerun modes. In other cases TCSQ contains no vertical component.

The vertical processing is done in the acquisition timing chain. The display V processing should be switched off (R116 = 87).

### Important control bits of MEGATEXT bus registers for sync adjustment:

Sync Mode	Register Control Bits	
C1 ... C3	R108 R109 R113 R114 R112 R116	NTSC VCR/TV sync source selection to CVBS freerun mode selection TA-to-TD display V processing
C2	R114	DPLL 2HS = 1
C3	R114	DPLL 100 Hz = 1

### MUSE

#### Characteristics

562.5 line per field (16.666 ms)  
 1125 lines per frame (33.33 ms)  
 1035 visible lines per frame  
 29.63  $\mu$ s horizontal period  
 33.75 kHz horiz. frequency  
 33.75 (MUSE) / 31.25 (PAL/2HS) = 1.08

#### MEGATEXT and MUSE

- MEGATEXT has to be synchronized by an external V-sync
- no MUSE freerun mode available
- optimum crystal frequency for MUSE is 22.14 MHz for horizontal freerun and sync slave mode
- horizontal PLL will still lock on 33.75-kHz even with 20.5-MHz crystal
- MEGATEXT display has to be operated in “double scan mode”:
  - PLL-prescaler 2:1 activated (R114, D1)
  - 2HS mode (20 lines per character/line repetition) activated (R114, D5)
- vertical fly wheel and filtering has to be switched off
- the pixel width is selectable between
 

768 pixels/line	= 25.92-MHz pixel clock
816 pixels/line	= 27.55-MHz pixel clock
768 pixels/line + 16:9 acceleration	= 32.40-MHz pixel clock
816 pixels/line + 16:9 acceleration	= 34.43-MHz pixel clock (16:9) mode

#### Compromise for PAL/NTSC and MUSE Applications

crystal frequency = 21.0 MHz

display PLL range:  $f_H = 31.25 \text{ kHz} + 12.7 \% - 7.8 \%$   
 display PLL range:  $f_H = 33.75 \text{ kHz} + 4.3 \% - 14.7 \%$   
 acquisition PLL range:  $f_H = 15.625 \text{ kHz} + 7.8 \% - 3.0 \%$

### Clock Modes

To enable the display PLL to lock the VCO-select bits of R85 have to be set to their correct value.

#### Normal operation

Acquisition and display have independant clocks generated by the CVBS-PLL and the display PLL.

#### Other modes of operation

The acquisition and the display can be forced to other clocks than the “internal” ones generated by the corresponding PLL. Special care must be taken when switching display or acquisition clock from their internal clock source to a foreign clock.

If an external clock is used MEGATEXT has to be in freerun mode.

Otherwise an external PLL has to be used that generates a 24-MHz clock and a 15.625 kHz horizontal pulse with a ratio clock/hor. frequency of 1536. To switch to an external PLL the bits of R112 to R114 have to be set in special sequence. Otherwise the PU may setup. If you need this type of application please contact Siemens Semiconductors, Consumer Electronic IC Development in Munich.

R112 D2	R112 D1	R112 D0	R114 D3	R113 D1.D0	Acquisition		Display	
TAPLL	TD-to- TA	TA-to- TD	PLL- LOCK	DS- LS1,0	clock source	hor. sync source	clock source	hor. sync source
0	0	0	0	00	int.	CVBS	int.	freerun
0	0	0	1	00	int.	CVBS	int.	ext. H
0	1	0	1	00	display	CVBS	int.	CVBS
0	0	1	0	01	int.	CVBS	acqu.	CVBS
0	0	0	1	01	int.	CVBS	int.	CVBS
1	0	0	0	10	int.	CVBS	ext. clock	ext. H
1	1	0	0	10	ext. clock	CVBS	ext. clock	ext. H
1	1	0	0	00	ext. clock	CVBS	ext. clock	freerun

### Changing the Clock Source

- If MEGATEXT shall work with synchronous clocks generated by the display PLL or an external clock source the CVBS-PLL has to be 10 ms in its normal mode before it may be forced to the display clock (R112, D1 = 1) or an external clock. Otherwise the CVBS-PLL may stay in a deadcycle: no acquisition timing will be generated and no text acquisition will be possible.

#### Example:

R112 = 00<sub>H</sub>

wait 10 ms

R112 = 02<sub>H</sub> (display clock) or R112 = 06<sub>H</sub> (external clock)

- If MEGATEXT shall work with synchronous clocks generated by the CVBS-PLL or an external clock source the display-PLL has to be 2 ms in its lock mode before it may be forced to the acquisition clock (R112, D0 = 1) or an external clock. Otherwise there is a chance of 1 to 764 that the display timing shows a phase shift of half a line.

#### Example:

R112 = 00<sub>H</sub>

R113 = 02<sub>H</sub>

R114 = 08<sub>H</sub> display PLL locking on the CVBS

wait 2 ms

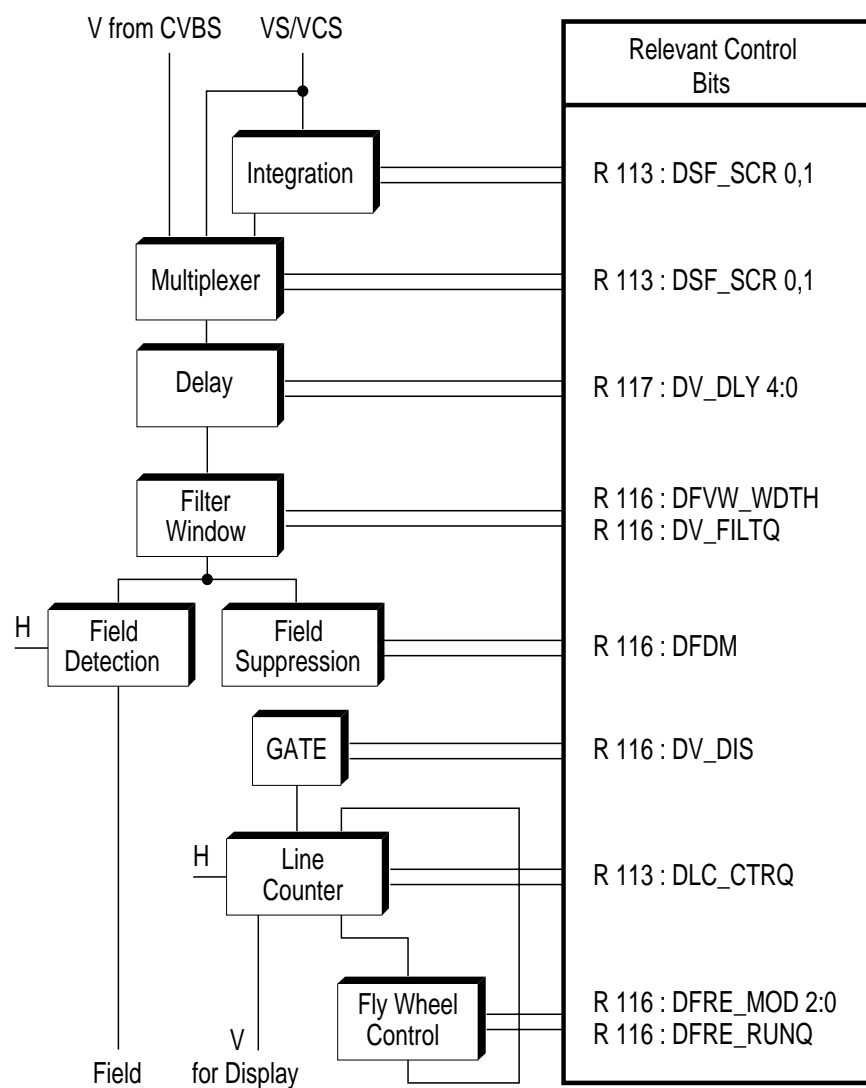
R112 = 01<sub>H</sub>

R113 = 01<sub>H</sub>

R114 = 00<sub>H</sub> display clock generated by the CVBS-PLL

### Vertical Processing for Display

#### Influence of Control Bits



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#### Flow Chart of Vertical Processing for Display



### Control Bits for Vertical Sync Processing

VSA_SRC	R108, D1
ASF_SRCXE	R108, D0
AFDM	R108, D1
AVFW_WDTH	R108, D2
VSAW_WDTH	R109, D3
V_THRE	R109, D4
ACQ_NTSC	R109, D5
DSF_SRC_1,0	R113, D3:2
DFDM	R116, D0
DVFW_WDTH	R116, D1
DV_FILTQ	R116, D2
DV_DIS	R116, D3
DFRE_MOD_2 ... 0	R116, D6:4
DFRE_RUNQ	R116, D7
DV_DLY_4 ... 0	R117, D4:0

#### VSA SRC

Source selection for vertical sync analysis.

The V-pulse is analyzed with respect to lines per frame (S525) and signal quality (V\_FINE).

0: Input is CVBS-signal.

1: Input is VS-pin.

#### ASF SRC

Acquisition start of field source.

0: ACQ V-sync processing is made with ACQ V-sync.

1: ACQ V-sync processing is made with display V-sync.

Set to 0 for normal text acquisition modes.

#### AFDM

Acquisition field detection mode.

A field suppression circuit can suppress all V-pulses that appear in the second half of a line. With standard signals having interlaced sync the V-pulse of the second field is suppressed.

0: Suppression active.

1: No suppression.

The acquisition flywheel needs only a V-trigger for the first field.

For standard signals this bit should be set to 0.

### **AVFW WIDTH**

Acquisition V-sync distortion filter window width.

0: Small window.

1: Broad window.

The acquisition V-sync signal is accepted only if it is inside the window.

A broad window should be used for VCR-applications.

The small window suppresses distortion in the V-sync signal until line

312 of each field in 625-line mode (ACQ\_NTSC = 0) or

262 of each field in 525-line mode (ACQ\_NTSC = 1).

For broad window suppresses distortion in the V-sync signal until line

300 of each field in 625-line mode or

250 of each field in 525-line mode.

### **VSAW WIDTH**

V-sync analysis distortion filter window width.

0: Small window.

1: Broad window.

The selected V-sync signal is accepted only if it is inside the window. The broad window should be used for VCR-applications.

The small window suppresses distortion in the V-sync signal until line

312 of each field in 625-line mode (ACQ\_NTSC = 0) or

262 of each field in 525-line mode (ACQ\_NTSC = 1).

For broad window suppresses distortion in the V-sync signal until line

300 of each field in 625-line mode or

250 of each field in 525-line mode.

### **V THRE**

Vertical sync pulse threshold.

Switches the time length which detects the V-sync pulse of the CVBS-signal.

In case of noisy CVBS-signals V\_THRE = 1 can be used.

1: Time length is 13.3  $\mu$ s.

0: Time length is 22.6  $\mu$ s.

### **ACQ NTSC**

ACQ\_NTSC controls the number of lines per frame (625/525) and the TTX-bit rate and format.

0: Acquisition works in PAL-mode.

1: Acquisition works in NTSC-mode.

ACQ\_NTSC controls the number of lines per frame (625/525) and the TTX-bit rate and format.

### DSF SRC 1, DSF SRC 0

Display start of field source.

The following table shows the source selection with DSF\_SRC\_1 and DSF SRC\_0 bits to generate internal start of display field.

DSF_SRC_1	DSF_SRC_0	Source
0	0	CVBS-pin
0	1	reserved
1	0	VS-pin (without internal V-integration)
1	1	VCS-pin (with internal V-integration)

### DFDM

Display field detection mode.

A field suppression circuit can suppress all V-pulses that appear in the second half of a line. If the V-delay is correct the pulses of the second field are suppressed.

0: Suppression active.

1: No suppression.

The flywheel needs only a V-trigger for the first field. When flywheel is used this bit should be set to 0.

### DVFW WDTN

Display V-sync distortion filter window width.

0: Small window.

1: Broad window.

The display V-sync signal is accepted only if it is inside the window. The broad window should be used for VCR-applications ☐ or "VCR-application" ☐.

The small window suppresses distortion in the V-sync signal until line

312 of each field in 625-line mode or

262 of each field in 525-line mode.

The broad window suppresses distortion in the V-sync signal until line

300 of each field in 625-line mode or

250 of each field in 525-line mode.

### DV FILTQ

Display V-sync distortion filter disable.

0: V-sync distortion filter enable.

1: V-sync distortion filter disable.

### DV DIS

External display V-sync disable. This bit is for test purposes only. Set to 0.

0: V-sync selected by sync source selection bits is processed for display V-sync generation.

1: Display V-sync is generated only by the display line counter (flywheel or counter overflow).

Referenced bits:

VS\_OUT\_EN.

### DFRE MOD 2 ... DFRE MOD 0

Display raster selection.

These bits take effect to:

- the sync pulses of the TCS-signal which is available at TCSQ-pin
- the VS-signal which is available at VS-pin (interlaced/non-interlaced)
- V-sync distortion filter window (50/60 Hz)

The possible raster selections are:

- 625 lines interlace,
- 625 lines non-interlace,
- 525 lines interlace,
- 525 lines non-interlace.

They are listed in the following table:

DFRE_MOD_2,1,0	Raster	Lines in Field 1/Field 2
000	non-interlaced	313 / 312 (text mode 50/100 Hz)
001	non-interlaced	312 / 312 (terminal mode 50/100 Hz)
010	interlaced	313 / 312 (mix mode 50/100 Hz)
011	non-interlaced	625 / 625 (progressive scan mode 50 Hz)
100	non-interlaced	263 / 262 (text mode 60/120 Hz)
101	non-interlaced	262 / 262 (terminal mode 60/120 Hz)
110	interlaced	263 / 262 (mix mode 60/120 Hz)
111	non-interlaced	525 / 525 (progressive scan mode 60 Hz)

### DFRE RUNQ

Display V-sync flywheel control.

0: Display V-sync flywheel enabled. Display V-sync is processed with flywheel.

1: Display V-sync flywheel disable. Display V-sync is processed without flywheel.

### DV DLY 4 ... DV DLY 0

Display vertical sync delay for out of standard signals.

The display vertical sync signal is delayed from 0 up to 62  $\mu$ s.

Delay resolution is 2  $\mu$ s.

$0 \leq DV\_DLY\_4 \dots DV\_DLY\_0 \leq 31$ .

To detect the right frame information of non-standard signals, the display vertical sync has to be shifted to the right position in the line, done by delay. Note that the display line counter may be affected by that delay.

### How to Set MEGATEXT® Registers for Your Text Display Synchronization

To define your MEGATEXT sync environment please check the following list for characteristics of your MEGATEXT application.

For each item you will find in the second part of this paper the bits of the control registers which have to be set correctly to get MEGATEXT synchronized. Although the list will most likely cover your application it does not cover all possible (exotic) MEGATEXT application modes. Sync modes with external clock are not covered by this paper. Register value “x” means: not relevant for the current context.

The following table gives an fast overview to the register settings for different sync sources.

#### Horizontal Sync

	External H - Sync Source					Freerun
	CVBS	HS			VCS	
		15.625 kHz Input		32.25 kHz Input		
		15.625 kHz Display	32.25 kHz Display			
R 112	xxxx xx01					xxx0 0000
R 113	xxxx xx01	xxxx xx00			xxxx xx01	xxxx xx00
R 114	xxxx 0xxx	x0xx 1x0x	x1xx 1x0x	x1xx 1x1x	xxxx 1xxx	xxxx 0xxx

#### Vertical Sync

	External V - Sync Source			Freerun
	CVBS	VS	VCS	
R 113	xxxx 00xx	xxxx 10xx	xxxx 11xx	xxxx 01xx
R 116				0xxx xxx0

### V Processing

Flywheel and filter for external vertical sync

### V Pulse Supression Window

An external V pulse can be suppressed in one of the following windows

Scan Mode	Count Mode	Line Count				R 114
Normal or progr. field	every line	1 ... 250	1 ... 262	1 ... 300	1 ... 313	0xxx xxxx
Prog. line	every 2nd line	1 ... 500	1 ... 524	1 ... 600	1 ... 626	1xxx xxxx
		x1xx xx1x	x1xx xx0x	x0xx xx1x	x0xx xx0x	
		R 116				

### V Pulse Restoration by Flywheel

V pulse will be generated internally, when

- No external V pulse has been detected
- The flywheel function is enabled (Bit "DFRE\_RUNQ" in Register 116)

The bits "DFRE\_MOD\_2.1.0" in Register 116 define the line, where the artificial V pulse is generated.

### Freerun Modes

In the freerun mode, no external Sync is used. The MEGATEXT chip is Sync master.

The TV set can be synchronised by following outputs:

- TCS output (composite sync)
- VCS signal at VS output (composite sync)
- Horizontal sync at HS output and vertical sync at VS output

The outputs are controlled by Register 82.

Selection of the freerun mode:

R 112	R 113
xxx0 0000	xxxx 0100

	R 114	R 116
PAL or Secam (50 Hz, 626 lines)	xxxx 0000	x0xx xxxx
NTSC (60 Hz, 525 lines)	xxxx 0001	x1xx xxxx
Normal scan	0000 xxxx	
Progressive field scan	0110 xxxx	
Progressive line scan	1100 xxxx	xx11 xxxx
Non interlaced (text mode)		xx00 xxxx
Non interlaced (terminal mode)		xx01 xxxx
Interlaced (mix mode)		xx10 xxxx