Firmware and Hardware Summary

Parameter	Specification
Device	SkyRC MC3000 Multi-Chemistry Battery Charger & Analyzer
MCU Family	STMicroelectronics STM32F103 (High/Medium-Density Series)
CPU Architecture	32-bit ARM Cortex-M3 (ARMv7-M architecture)
Instruction Set	Thumb-2 (utilizing hardware integer division `udiv`/`sdiv` and bitfield instructions)
Clock Configuration	72 MHz Core Clock (8 MHz HSE external crystal × 9 PLL multiplier)
Flash Layout	Bootloader: `0x08000000`–`0x08003FFF` (16 KB)Main Firmware: `0x08004000`–`0x08019583` (V1.25: 87,428 bytes)Main Firmware: `0x08004000`–`0x0801994B` (V1.27: 88,396 bytes, +968 bytes)
SRAM Layout	Base `0x20000000`; Initial Stack Pointer: `0x200036F8` (~14 KB used: 3,176 B RW data + 10,896 B ZI data)
Peripheral Stack	USB Full-Speed Device (HID protocol), Microchip MCP3424 external 18-bit $\Delta\Sigma$ ADCs (I2C), Hardware Timers (PWM current generation), UART (BLE interface)
Toolchain	Keil ARM Compiler 5 (`armcc` / ARM RealView compilation engine)

Component & File Analysis

`MC3000_Firmware_Update__V1.25.exe` and `MC3000_Firmware_Update__V1.27.exe` are .NET Framework 4.8 GUI loaders containing two embedded Intel HEX resources:

1. `UpgradeFirmware.loader.hex` (20,955 bytes): **100% byte-identical** between versions 1.25 and 1.27.

2. `UpgradeFirmware.rom.hex`: Contains the Cortex-M3 application firmware.

3. Static Read-Only Data (`rodata` string tables, chemistry names, menu trees): **100% byte-identical** between versions.

Relevant Functional Differences (V1.25 vs V1.27)

The total code delta between 1.25 and 1.27 is **968 bytes** distributed across 15 function units. The changes isolate to five concrete functional areas:

1. Internal Resistance (IR) Measurement Routine Overhaul

- **Test Current Modification**:
  - **V1.25**: Phase 1 applied a 200 mA test load (`0xC8`), followed by 1200 mA (`0x4B0`) in Phase 2 ($\Delta I = 1.00\,\text{A}$).
  - **V1.27**: Phase 1 reduced to 100 mA test load (`0x64`), followed by 1200 mA in Phase 2 ($\Delta I = 1.10\,\text{A}$).
- **Calculation Engine Replacement**:
  - **V1.25**: Computed internal resistance using external software-emulated double-precision floating-point calls (`__aeabi_i2d`, `__aeabi_ddiv`, `__aeabi_dmul`).
  - **V1.27**: Removed soft-float routines in favor of direct 32-bit hardware integer arithmetic:

$$\text{IR}\,(\text{m}\,\Omega) = \frac{(V_1 - V_2) \times 800}{I_2 - I_1}$$

    using native Cortex-M3 `muls` and `udiv` instructions, with hard-clamping to $1\,\text{m}\,\Omega$ on sub-$2\,\text{m}\,\Omega$ readings to prevent division underflow artifacts.

2. Slot State Machine & Cutoff Validation (Func 1, 2, 3)

- **Threshold Comparison Ordering**:
  - **V1.25**: The over-voltage / cutoff condition evaluated raw unscaled ADC readings directly against upper voltage bounds (e.g. 4500 mV / `0x1194`, 1305 mV / `0x519`) concurrently with power-scaling math (10000 base).
  - **V1.27**: Restructured branch logic: the hard voltage limit (4500 mV) is evaluated before scaling calculations.
- **Debounce Filtering**:
  - Added 3-cycle consecutive sample confirmation before latching slot termination errors, suppressing false-positive cutoff triggers caused by transient voltage spikes or contact resistance fluctuations.

3. Preset / Profile Persistence Logic (Func 14, 15)

- **Memory Alignment Fix**:
  - **V1.25**: Used 64-bit double-word store (`strd`) at offset `0x1FC` into slot profile memory.
  - **V1.27**: Replaced with two independent 32-bit single-word stores (`str.w`) to avoid unaligned 64-bit access faults on Cortex-M3.
- **Preset Initialization Clearing**:
  - **V1.27** explicitly zeroes out slot runtime registers (`0x60`, `0x1F2`, `0x5E`, `0x1FC`) upon loading a saved profile preset (profiles 1–30), preventing stale current/voltage targets from persisting across chemistry changes.

4. LCD User Interface & Slot Navigation (Func 11, 12)

- **Slot Switching Synchronization**:
  - Fixed a state-leak bug where pressing slot keys (1–4) during active charging could cause target voltage (offset `0x1E`) and timer ticks (offset `0x54`) from the previous slot to display in the new slot's view.
  - Added bounds-checking on menu navigation index offsets to eliminate submenu wrap-around glitches.

5. Safety Flagging during Chemistry Mode Transitions (Func 4)

- **V1.27** adds explicit status byte clears (`strb r2, [r4, #3]`) when toggling between Li-Ion, LiFePO4, LTO, and NiMH/NiCd chemistries, ensuring slot parameters are re-validated against chemical limits before output stage activation.