4 AI8051U Series Selection Overview, Features / Price / Pinout / ISP Download / Programming Circuits

4.1 AI8051U-LQFP48 General Introduction, USB Download, Programming / Emulation Circuits

4.1.1 Features and Price

➤ Selection and price (no external crystal required, no external reset required, 12-bit ADC, 15 channels)

MCU model	Operating voltage (V)	Flash program memory, 100k cycles (bytes)	edata internal extended DATA RAM; stack/variables (bytes)	xdata internal large-capacity SRAM; variables (bytes)	EEPROM, 100k cycles (bytes)	Maximum I/O count	Legacy I/O interrupts INT0/INT1/INT2/INT3/INT4; wake from power-down	All I/O: high/low-level and rising/falling-edge interrupts; wake from power-down	DMA 8080/6800 interface TFT LCD driver (8/16-bit)	RTC independent clock Y/M/D/h/m/s; clock tracking; wake from power-down	DMA UART asynchronous serial; wake from power-down	DMA USART synchronous/asynchronous serial; wake from power-down; 2 extra SPI/LIN groups	Full-speed USB; USB-CDC and USB-HID	DMA I2S audio bus; wake from power-down	DMA SPI; wake from power-down	DMA QSPI	DMA I2C; wake from power-down	TFPU (108 MHz): hardware floating-point / trig / inverse-trig	MDU32: hardware 32-bit multiply/divide	Timers/counters T0/T1/T2/T3/T4/T11; external-pin interrupt wake-up	144 MHz, 16-bit advanced PWM timer; complementary/dead-time control	Legacy PCA/CCP/PWM; external interrupt + wake; rising/falling/edge interrupt	Dedicated power-down wake-up timer	DMA 15-channel high-speed ADC (8 PWM channels usable as 8-channel D/A)	Comparator (usable as 1-channel A/D; external wake source)	Internal low-voltage-detect interrupt; wake from power-down	Watchdog reset timer	Internal reliable reset (selectable reset threshold voltage)	Internal high-precision clock (adjustable <=42 MHz); serial communication / frequency tracking	Clock and reset can be output externally	Encrypted program transfer (anti-interception)	Programmable port command for next firmware update	Supports RS485 download	Hardware USB direct download and hardware USB emulation	On-chip online emulation	Price / package			
																																							LQFP48	LQFP44	PDIP40	Supply information
AI8051U-34K64	1.9-5.5	64K	2K	32K	IAP	45	Yes	Yes	Yes	Yes	2	2	Yes	Yes	3	Yes	Yes	Yes	Yes	6	8	3	Yes	12-bit	Yes	Yes	Yes	4 levels	Yes	Yes	Yes	Yes	Yes	Yes	Yes	¥1.9	¥3.9	¥4.0	
AI8051U-34K32	1.9-5.5	32K	2K	32K	32K	45	Yes	Yes	Yes	Yes	2	2	Yes	Yes	3	Yes	Yes	Yes	Yes	6	8	3	Yes	12-bit	Yes	Yes	Yes	4 levels	Yes	Yes	Yes	Yes	Yes	Yes	Yes				
AI8051U-34K16	1.9-5.5	16K	2K	32K	48K	45	Yes	Yes	Yes	Yes	2	2	Yes	Yes	3	Yes	Yes	Yes	Yes	6	8	3	Yes	12-bit	Yes	Yes	Yes	4 levels	Yes	Yes	Yes	Yes	Yes	Yes	Yes				

▸ Core

- ✓ Ultra-high-speed 32-bit 8051 core (1T), more than about 70x faster than a traditional 8051.
- ✓ 4 interrupt priority levels.
- ✓ Supports online emulation.

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▸ Operating voltage

- ✓ 1.9 V to 5.5 V (when the operating temperature is below -40°C, the supply voltage must not be below 3.0 V).

▸ Operating temperature

- ✓ -20°C to 65°C (internal high-speed IRC temperature drift: -0.76% to +0.98%).
- ✓ -40°C to 85°C (internal high-speed IRC temperature drift: ±1.3%).
- ✓ -40°C to 125°C (internal high-speed IRC temperature drift: ±3%; above 85°C, use an external crystal of 35 MHz or lower).

▸ Flash memory

- ✓ Up to 64K bytes of FLASH program memory (ROM), used to store user code.
- ✓ A user-configurable portion of FLASH can be used as DATA FLASH/EEPROM. Page erase size: 512 bytes. A typical sector can reach 100,000 erase cycles; for conservative design, regard 20,000 cycles as the guaranteed-use figure.
- ✓ Supports direct downloading through hardware USB and through the serial port.
- ✓ Flash data retention: 100 years @25°C, 20 years @105°C, 10 years @125°C. Because the average temperature in automotive and MCU applications cannot remain above 105°C for long periods, practical retention can exceed 20 years; 100 years is not guaranteed.

SRAM, 34K bytes total

- ✓ 2K bytes internal SRAM (edata).
- ✓ 32K bytes internal extended RAM (internal xdata).

Clock control

- ✓ Internal high-precision, high-stability high-speed IRC (can be fine-adjusted up/down during ISP programming).
  - ◇ Error ±0.3% (room temperature, 25°C).
  - ◇ -1.35% to +1.30% temperature drift (full temperature range, -40°C to 85°C).
  - ◇ -0.76% to +0.98% temperature drift (temperature range, -20°C to 65°C).
- ✓ Internal 32 kHz low-speed IRC (used for low-power modes; includes temperature- and voltage-compensation circuitry, but has relatively large error).
- ✓ External crystal (4 MHz to 42 MHz) and external clock. A dedicated anti-interference circuit for the external clock is provided and can be enabled by software.
- ✓ Internal PLL output clock (note: the 144 MHz / 96 MHz PLL outputs can independently serve as clock sources for high-speed PWM and high-speed SPI).

  The user can freely select any one of the above four clock sources.
- ✓ Note: the internal PLL output clock can reach up to 144 MHz / 148 MHz. If high-speed PWM uses the PLL as its clock source, at 125°C it is recommended to keep the PWM input clock below 138 MHz; at 105°C the PWM input clock may use 144 MHz.

(When the chip powers up normally, powers up after reset, watchdog reset, or low-voltage-detect reset, it initially executes the ISP system program using the fixed internal 24 MHz high-speed IRC. When downloading a user program and then resetting into the user application, or when resetting directly into the user application without a download, the default high-speed IRC frequency is the value set during the previous user download. If the application requires an external high-speed crystal, an external 32.768 kHz crystal, or the internal 30 kHz low-speed IRC, the corresponding clock must first be enabled in software, then selected by configuring the CLKSEL register.)

Reset

- ✓ Hardware reset
  - ◇ Power-on reset; reset voltage 1.7 V to 1.9 V (effective when the chip low-voltage-reset function is not enabled).
  - ◇ Reset-pin reset. The reset function is brought out on P4.7 by default; during ISP downloading of the user program, P4.7 can be configured as the reset pin. Note: when P4.7 is configured as the reset pin, reset is active low.
  - ◇ Watchdog overflow reset.
  - ◇ Low-voltage-detect reset; four selectable thresholds: 2.0 V, 2.4 V, 2.7 V, 3.0 V.
- ✓ Software reset
  - ◇ Write the reset-trigger register by software.

Interrupts

- ✓ Interrupt sources: INT0, INT1, INT2, INT3, INT4, Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, USART1, USART2, UART3, UART4, ADC conversion, LVD (low-voltage detect), SPI, I2C, comparator, PWMA, PWMB, USB, TFT/LCD-interface interrupt, RTC, all I/O interrupts (8 groups), DMA receive/transmit interrupts for serial ports 1/2/3/4, I2C DMA receive/transmit, SPI DMA, ADC DMA, LCD-driver DMA, and memory-to-memory DMA.
- ✓ Provides 4 interrupt priority levels.

Digital peripherals

- ✓ Six 16-bit timers: Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, Timer 11. Timer 0 mode 3 provides an NMI (non-maskable interrupt) function. Timer 0 and Timer 1 mode 0 are 16-bit auto-reload modes. Timer 11 has a selectable clock source.
- ✓ Two high-speed synchronous/asynchronous serial ports: Serial Port 1 (USART1) and Serial Port 2 (USART2); baud-rate clock source up to FOSC/4. Supports synchronous mode, asynchronous mode, SPI mode, LIN mode, infrared mode (IrDA), and smart-card mode (ISO7816).
- ✓ Two high-speed asynchronous serial ports: Serial Port 3 and Serial Port 4; baud-rate clock source up to FOSC/4.

- ✓ Two advanced PWM groups, implementing 8 PWM channels (4 complementary pairs) with dead-time control and support for external fault detection.
- ✓ Three 16-bit CCP/PCA/PWM modules: CCP0, CCP1, CCP2; usable for capture, high-speed pulse output, and 6/7/8/10-bit PWM output.
- ✓ SPI: 3 hardware SPI interfaces (one independent SPI plus the SPI modes of two USARTs), supporting master mode, slave mode, and automatic master/slave switching. Note: all 3 SPI interfaces support DMA.
- ✓ QSPI: supports single, dual, and quad modes.
- ✓ I2C: supports master mode and slave mode.
- ✓ ICE: hardware-supported emulation.
- ✓ RTC: supports year, month, day, hour, minute, second and sub-second (1/128 s), plus clock interrupts and one alarm.
- ✓ USB: USB2.0/USB1.1-compatible full-speed USB, 6 bidirectional endpoints, supporting four endpoint transfer types (control, interrupt, bulk, and isochronous); each endpoint has a 64-byte buffer.
- ✓ I2S: audio bus.
- ✓ MDU32: hardware 32-bit multiply/divide unit (including 32-bit / 32-bit division and 32-bit × 32-bit multiplication).
- ✓ TFPU: single-precision floating-point unit (supports floating-point add, subtract, multiply, divide, sine, cosine, tangent, and arctangent operations).
- ✓ I/O interrupts: all I/O pins support interrupts. Each I/O group has its own interrupt-vector address. All I/O interrupts support four modes: high-level, low-level, rising-edge, and falling-edge. I/O interrupts can wake the device from power-down and provide 4 interrupt-priority levels.
- ✓ LCD driver module: supports both 8080 and 6800 interfaces and 8-bit or 16-bit data widths.
- ✓ DMA: supports SPI receive register to memory, memory to SPI transmit register, data to the I2C transmit register, I2C receive data to memory, receive data from serial ports 1/2/3/4 to memory, memory to the transmit registers of serial ports 1/2/3/4, ADC automatic sampling to memory (while calculating an average), data to the LCD-driver transmit register, and memory-to-memory copying.
- ✓ Hardware digital ID: supports 32 + 32 bytes.

▸ Analog peripherals

- ✓ ADC: ultra-high-speed ADC with 12-bit accuracy and 15 analog input channels (channels 0 to 14). ADC channel 15 is used to measure the internal reference voltage during testing. At the factory, the internal reference voltage is adjusted to 1.19 V, error ±1%.
- ✓ Comparator: one comparator.

▸ GPIO

- ✓ Up to 46 GPIO pins: P0.0-P0.7, P1.0-P1.7, P2.0-P2.7, P3.0-P3.7, P4.0-P4.7, P5.0-P5.3, P5.6-P5.7.
- ✓ All GPIO pins support four modes: quasi-bidirectional, push-pull output, open-drain, and high-impedance input.
- ✓ Except for P3.0 and P3.1, all other I/O pins power up in high-impedance input mode. The user must configure the I/O mode before using a pin.
- ✓ Each I/O pin can independently enable an internal 10 kΩ pull-up resistor and a 10 kΩ pull-down resistor.

▸ Packages

- ✓ LQFP48, LQFP44, PDIP40.