# Preliminary Specification

**PRODUCT NAME:** RGS15128128WR000
**PRODUCT NO.:** 9922102000

| CUSTOMER |
|---|
|  |
| **APPROVED BY** |
|  |
| **DATE:** |

| RITDISPLAY CORP. APPROVED |
|---|
|  |

# REVISION RECORD

| REV. | REVISION DESCRIPTION | REV. DATE | REMARK |
|------|----------------------|-----------|--------|
| X01 | ■ INITIAL RELEASE | 2008. 07. 10 | |
| X02 | ■ Modify definition of panel thickness<br>■ Add lifetime specifications<br>■ Modify D.C electrical characteristics<br>■ Add panel electrical specifications<br>■ Add application circuit | 2009. 04. 24 | Page 5, 6, 7, 8 & 16 |

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## 1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

## 2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

## 3. FEATURES

- Small molecular organic light emitting diode.
- Color : White
- Panel resolution : 128*128
- Driver IC : SSD1327
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design : 1.41 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface, $I^2C$ Interface.
- Wide range of operating temperature : -40 to 70°C
- Anti-glare polarizer.

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## 4. MECHANICAL DATA

| NO | ITEM | SPECIFICATION | UNIT |
|----|------|---------------|------|
| 1 | Dot Matrix | 128 x 128 | dot |
| 2 | Dot Size | 0.19 (W) x 0.19 (H) | mm$^2$ |
| 3 | Dot Pitch | 0.21 (W) x 0.21 (H) | mm$^2$ |
| 4 | Aperture Rate | 82 | % |
| 5 | Active Area | 26.86 (W) x 26.86 (H) | mm$^2$ |
| 6 | Panel Size | 33.8 (W) x 36.5 (H) | mm$^2$ |
| 7* | Panel Thickness | 1.22 $\pm$ 0.1 | mm |
| 8 | Module Size | 33.8 (W) x 43.7 (H) x 1.41 (T) | mm$^3$ |
| 9 | Diagonal A/A size | 1.5 | inch |
| 10 | Module Weight | TBD | gram |

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

## 5. MAXIMUM RATINGS

| ITEM | MIN | MAX | UNIT | Condition | Remark |
|---|---|---|---|---|---|
| Supply Voltage ($V_{CI}$) | -0.3 | 4 | V | Ta = 25°C | IC maximum rating |
| Supply Voltage (Vcc) | 8 | 19 | V | Ta = 25°C | IC maximum rating |
| Operating Temp. | -40 | 70 | °C | | |
| Storage Temp | -40 | 85 | °C | | |
| Humidity | | 85 | % | | |
| Life Time | 10,000 | - | Hrs | 100 cd/m$^2$, 50% checkerboard | Note (1) |
| Life Time | 11,000 | - | Hrs | 90 cd/m$^2$, 50% checkerboard | Note (2) |
| Life Time | 12,000 | - | Hrs | 80 cd/m$^2$, 50% checkerboard | Note (3) |

Note:

    (A) Under Vcc = 15V, Ta = 25°C, 50% RH.

    (B) Life time is defined the amount of time when the luminance has decayed
        to less than 50% of the initial measured luminance.

(1) Setting of 100 cd/m$^2$ :
-   Contrast setting : 0x9b
-   Frame rate : 105Hz
-   Duty setting : 1/128

(2) Setting of 90 cd/m$^2$ :
-   Contrast setting : 0x77
-   Frame rate : 105Hz
-   Duty setting : 1/128

(3) Setting of 80 cd/m$^2$ :
-   Contrast setting : 0x60
-   Frame rate : 105Hz
-   Duty setting : 1/128

## 6. ELECTRICAL CHARACTERISTICS

### 6.1 D.C ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETERS | TEST CONDITION | MIN | TYP | MAX | UNIT |
|--------|-----------|----------------|-----|-----|-----|------|
| $V_{CC}$ | Driver power supply (for OLED panel) | - | 14.5 | 15 | 15.5 | V |
| $V_{CI}$ | Low voltage power supply | - | 2.6 | - | 3.5 | V |
| $V_{OH}$ | High logic output level | Iout=100 uA, | $0.9* V_{CI}$ | - | $V_{CI}$ | V |
| $V_{OL}$ | Low logic output level | Iout=100uA, | 0 | - | $0.1* V_{CI}$ | V |
| $V_{IH}$ | High logic input level | Iout=100uA, | $0.8* V_{CI}$ | - | $V_{CI}$ | V |
| $V_{IL}$ | Low logic input level | Iout=100uA, | 0 | - | $0.2* V_{CI}$ | V |
| $I_{CC}$ | $V_{CC}$ Supply Current | $V_{CI}$ = 3.5V, $V_{CC}$ = 18V, Display ON, No panel attached, contrast = FF | External $V_{DD}$= 2.5V — 600 / Internal $V_{DD}$= 2.5V — 600 | 600 / 600 | 750 / 750 | uA |
| $I_{CI}$ | $V_{CI}$ Supply Current | $V_{CI}$ = 3.5V, $V_{CC}$ = 18V, Display ON, No panel attached, contrast = FF | External $V_{DD}$= 2.5V / Internal $V_{DD}$= 2.5V | 35 / 95 | 50 / 120 | uA |
| $I_{SEG}$ | Segment output current Setting $V_{CC}$=18V, IREF=10uA | Contrast=FF | - | 300 | 370 | uA |
| | | Contrast=AF | - | 206 | - | uA |
| | | Contrast=7F | - | 150 | - | uA |
| | | Contrast=3F | - | 75 | - | uA |
| | | Contrast=1F | - | 37.5 | - | uA |

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## 6.2 ELECTRO-OPTICAL CHARACTERISTICS

## PANEL ELECTRICAL SPECIFICATIONS

| PARAMETER | MIN | TYP. | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|
| Normal mode current consumption | - | 32 | 34 | mA | All pixels on |
| Standby mode current consumption | - | 3 | 4 | mA | Standby mode 10% pixels on |
| Normal mode power consumption | - | 480 | 510 | mW | All pixels on |
| Standby mode power consumption | - | 45 | 60 | mW | Standby mode 10% pixels on |
| Pixel Luminance | 70 | 90 | | cd/m$^2$ | Display Average |
| Standby Luminance | | 20 | | cd/m$^2$ | |
| CIEx (White) | 0.24 | 0.28 | 0.32 | | CIE1931 |
| CIEy (White) | 0.28 | 0.32 | 0.36 | | CIE1931 |
| Dark Room Contrast | 2000:1 | | | | |
| Viewing Angle | 160 | | | degree | |
| Response Time | | 10 | | µs | |

Normal mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x77
- Frame rate : 105Hz
- Duty setting : 1/128

Standby mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x14
- Frame rate : 105Hz
- Duty setting : 1/128

# 7. INTERFACE

## 7.1 FUNCTION BLOCK DIAGRAM
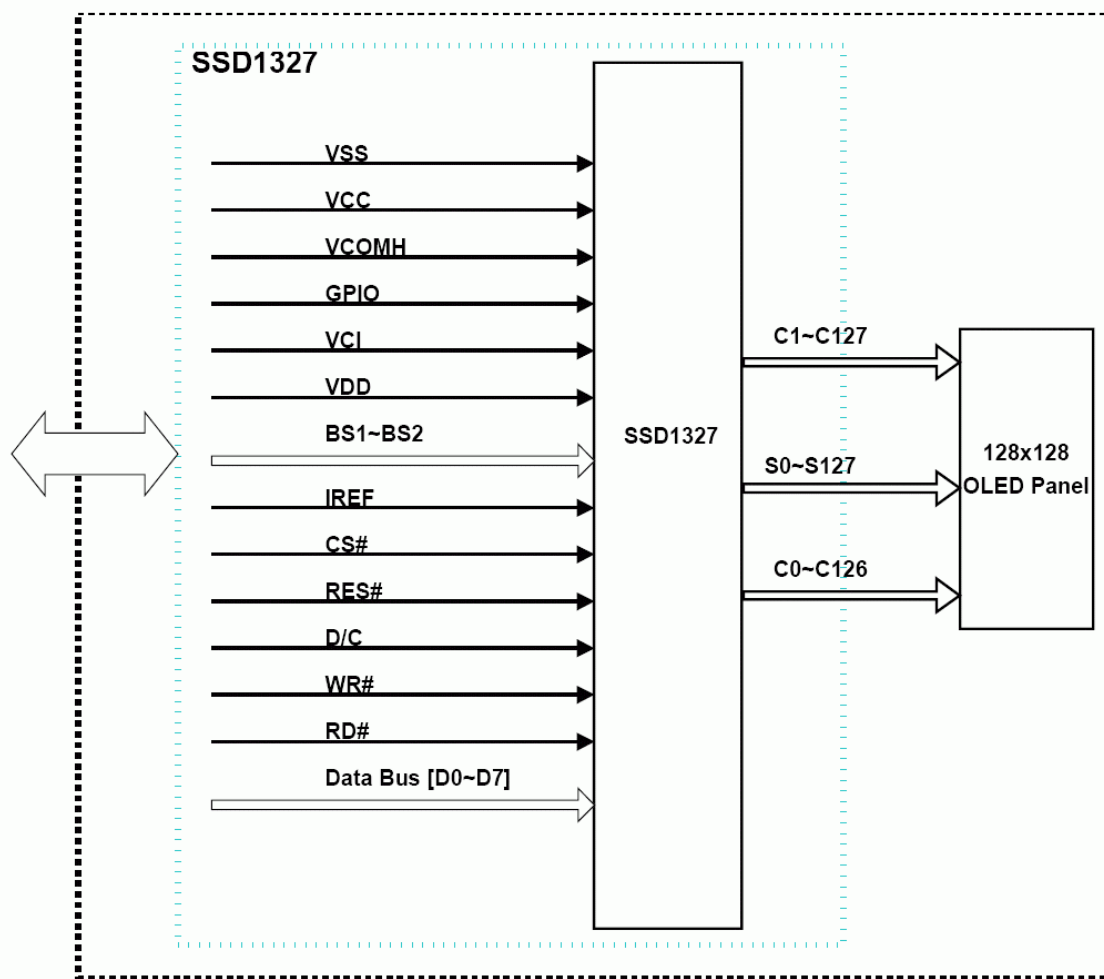


RiTdisplay 128X128 OLED Module

## 7.2 PANEL LAYOUT DIAGRAM



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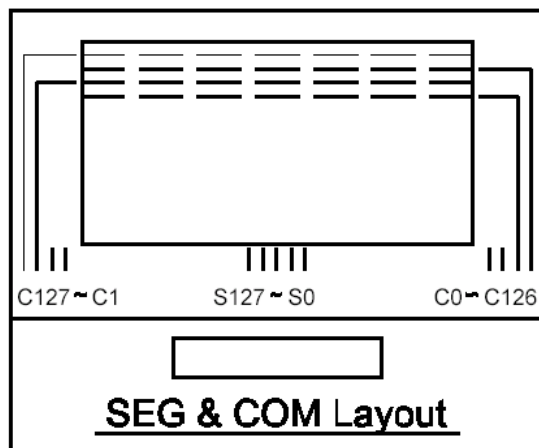
## 7.3 PIN ASSIGNMENTS

| PIN NAME | PIN NO | DESCRIPTION |
|---|---|---|
| VSS | 1 | Ground. |
| VCC | 2 | Power supply for analog circuit. |
| VCOMH | 3 | Com Voltage Output. A capacitor should be connected between this pin and $V_{SS}$. |
| GPIO | 4 | General I/O port. |
| VCI | 5 | Power supply for logic circuit. |
| VDD | 6 | A capacitor should be connected between this pin and $V_{SS}$. |
| BS1 | 7 | MCU bus interface selection pins. |
| BS2 | 8 | MCU bus interface selection pins. |
| VSS | 9 | Ground. |
| IREF | 10 | Reference current input pin. A resistor should be connected between this pin and $V_{SS}$. |
| CS# | 11 | Chip select input. |
| RES# | 12 | Reset signal input. When it's low, initialization of SSD1327 is executed. |
| D/C | 13 | Data/ Command control. Pull high for write/read display data. Pull low for write command or read status. |
| WR# | 14 | MCU interface input. Data write operation is initiated when it's pull low. |
| RD# | 15 | MCU interface input. Data read operation is initiated when it's pull low. |
| D0 | 16 | Data bus(for parallel interface) |
| D1 | 17 | |
| D2 | 18 | |
| D3 | 19 | |
| D4 | 20 | |
| D5 | 21 | |
| D6 | 22 | |
| D7 | 23 | |
| VCC | 24 | Power supply for analog circuit. |
| VSS | 25 | Ground. |

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## 7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x128x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps below tables show some examples on using the command "Set Re-map" A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 … D8189, D8190, D8191 represent the 128x128 data bytes in the GDDRAM.

The GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
  Disable Column Address Re-map (A[0]=0)
  Disable Nibble Re-map (A[1]=0)
  Enable Horizontal Address Increment (A[2]=0)
  Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

**GDDRAM address map 1**

| COM Outputs | Row Address (HEX) | SEG0 | SEG1 | SEG2 | SEG3 | | SEG124 | SEG125 | SEG126 | SEG127 | SEG Outputs |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 00 | | 01 | | | 3E | | 3F | | Column Address |
| COM0 | 00 | D0[3:0] | D0[7:4] | D1[3:0] | D1[7:4] | | D62[3:0] | D62[7:4] | D63[3:0] | D63[7:4] | (HEX) |
| COM1 | 01 | D64[3:0] | D64[7:4] | D65[3:0] | D65[7:4] | | D126[3:0] | D126[7:4] | D127[3:0] | D127[7:4] | |
| | | | | | | | | | | | |
| COM126 | 7E | D8064[3:0] | D8064[7:4] | D8065[3:0] | D8065[7:4] | | D8126[3:0] | D8126[7:4] | D8127[3:0] | D8127[7:4] | |
| COM127 | 7F | D8128[3:0] | D8128[7:4] | D8129[3:0] | D8129[7:4] | | D8190[3:0] | D8190[7:4] | D8191[3:0] | D8191[7:4] | |

Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
  Disable Column Address Re-map (A[0]=0)
  Disable Nibble Re-map (A[1]=0)
  Enable Vertical Address Increment (A[2]=1)
  Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

**GDDRAM address map 2**

| | | SEG0 | SEG1 | SEG2 | SEG3 | | SEG124 | SEG125 | SEG126 | SEG127 | SEG Outputs |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 00 | | 01 | | | 3E | | 3F | | Column Address (HEX) |
| COM0 | 00 | D0[3:0] | D0[7:4] | D128[3:0] | D128[7:4] | | D7936[3:0] | D7936[7:4] | D8064[3:0] | D8064[7:4] | |
| COM1 | 01 | D1[3:0] | D1[7:4] | D129[3:0] | D129[7:4] | | D7937[3:0] | D7937[7:4] | D8065[3:0] | D8065[7:4] | |
| \| | \| | | | | | | | | | | |
| COM126 | 7E | D126[3:0] | D126[7:4] | D254[3:0] | D254[7:4] | | D8062[3:0] | D8062[7:4] | D8190[3:0] | D8190[7:4] | |
| COM127 | 7F | D127[3:0] | D127[7:4] | D255[3:0] | D255[7:4] | | D8063[3:0] | D8063[7:4] | D8191[3:0] | D8191[7:4] | |

COM Outputs | Row Address (HEX)

(Display Startline=0)
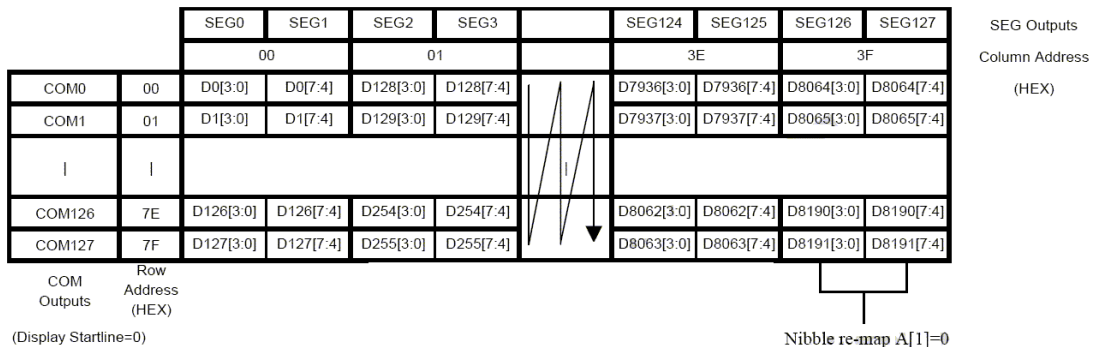
Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
  Enable Column Address Re-map (A[0]=1)
  Enable Nibble Re-map (A[1]=1)
  Enable Horizontal Address Increment (A[2]=0)
  Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

**GDDRAM address map 3**

| | | SEG0 | SEG1 | SEG2 | SEG3 | | SEG124 | SEG125 | SEG126 | SEG127 | SEG Outputs |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 3F | | 3E | | | 01 | | 00 | | Column Address (HEX) |
| COM0 | 00 | D63[7:4] | D63[3:0] | D62[7:4] | D62[3:0] | | D1[7:4] | D1[3:0] | D0[7:4] | D0[3:0] | |
| COM1 | 01 | D127[7:4] | D127[3:0] | D126[7:4] | D126[3:0] | | D65[7:4] | D65[3:0] | D64[7:4] | D64[3:0] | |
| \| | \| | | | | | | | | | | |
| COM126 | 7E | D8127[7:4] | D8127[3:0] | D8126[7:4] | D8126[3:0] | | D8065[7:4] | D8065[3:0] | D8064[7:4] | D8064[3:0] | |
| COM127 | 7F | D8191[7:4] | D8191[3:0] | D8190[7:4] | D8190[3:0] | | D8129[7:4] | D8129[3:0] | D8128[7:4] | D8128[3:0] | |

COM Outputs | Row Address (HEX)

(Display Startline=0)

Nibble re-map A[1]=1

The example in which the display start line register is set to 10h with the following condition:

- Command "Set Re-map" A0h is set to:
    Disable Column Address Re-map (A[0]=0)
    Disable Nibble Re-map (A[1]=0)
    Enable Horizontal Address Increment (A[2]=0)
    Enable COM Re-map (A[4]=1)
- Display Start Line=78h (corresponds to COM119)
- Data byte sequence: D0, D1, D2 … D8191

**GDDRAM address map 4**

| COM Outputs | Row Address (HEX) | SEG0 | SEG1 | SEG2 | SEG3 | | SEG124 | SEG125 | SEG126 | SEG127 | SEG Outputs |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 00 | | 01 | | | 3E | | 3F | | Column Address (HEX) |
| COM119 | 00 | D0[3:0] | D0[7:4] | D1[3:0] | D1[7:4] | | D62[3:0] | D62[7:4] | D63[3:0] | D63[7:4] | |
| COM118 | 01 | D1[3:0] | D64[7:4] | D65[3:0] | D65[7:4] | | D126[3:0] | D126[7:4] | D127[3:0] | D127[7:4] | |
| \| | \| | | | | | | | | | | |
| COM121 | 7E | D126[3:0] | D8064[7:4] | D8065[3:0] | D8065[7:4] | | D8126[3:0] | D8126[7:4] | D8127[3:0] | D8127[7:4] | |
| COM120 | 7F | D127[3:0] | D8128[7:4] | D8129[3:0] | D8129[7:4] | | D8190[3:0] | D8190[7:4] | D8191[3:0] | D8191[7:4] | |

(Display Startline=78H)

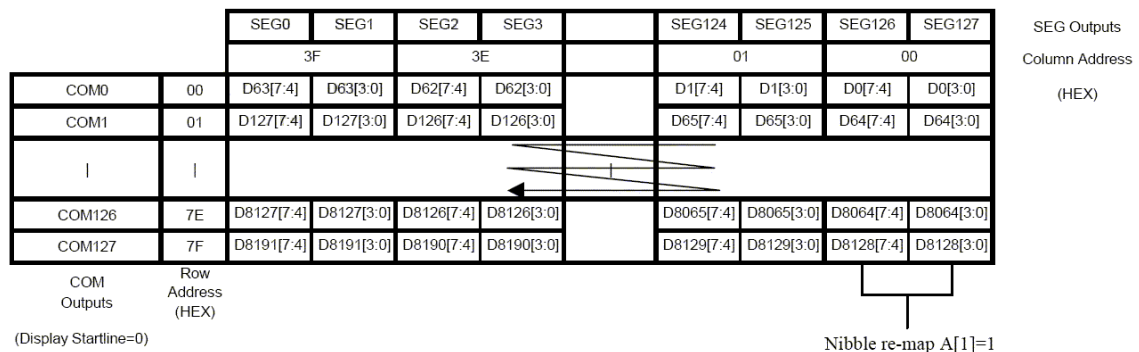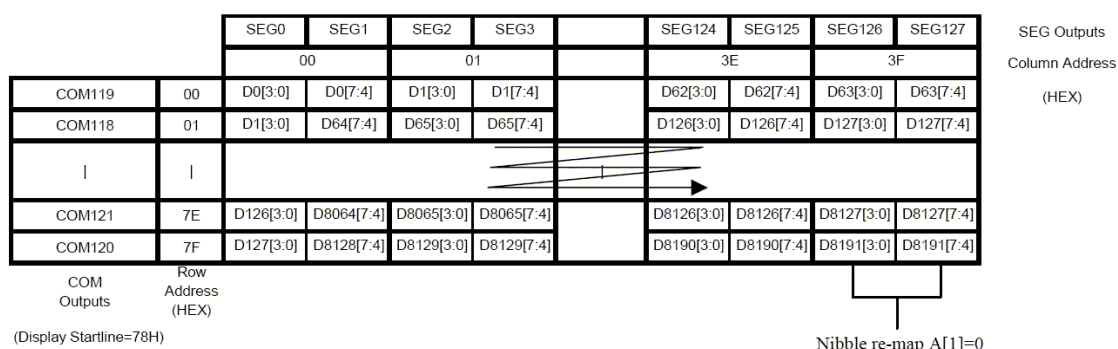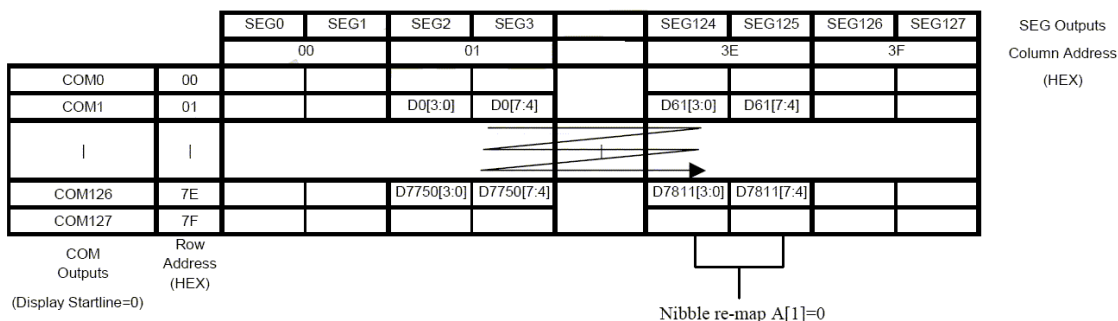Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
    Disable Column Address Re-map (A[0]=0)
    Disable Nibble Re-map (A[1]=0)
    Enable Horizontal Address Increment (A[2]=0)
    Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=7Eh
- Data byte sequence: D0, D1, D2 … D7811

**GDDRAM address map 5**

| COM Outputs | Row Address (HEX) | SEG0 | SEG1 | SEG2 | SEG3 | | SEG124 | SEG125 | SEG126 | SEG127 | SEG Outputs |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 00 | | 01 | | | 3E | | 3F | | Column Address (HEX) |
| COM0 | 00 | | | | | | | | | | |
| COM1 | 01 | | | D0[3:0] | D0[7:4] | | D61[3:0] | D61[7:4] | | | |
| \| | \| | | | | | | | | | | |
| COM126 | 7E | | | D7750[3:0] | D7750[7:4] | | D7811[3:0] | D7811[7:4] | | | |
| COM127 | 7F | | | | | | | | | | |

(Display Startline=0)

Nibble re-map A[1]=0

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## 7.5 INTERFACE TIMING CHART

**8080-Series MCU Parallel Interface Timing Characteristics**

$(V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{CI} = 3.3V$, $T_A = 25°C)$

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 300 | - | - | ns |
| $t_{AS}$ | Address Setup Time | 10 | - | - | ns |
| $t_{AH}$ | Address Hold Time | 0 | - | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 40 | - | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 7 | - | - | ns |
| $t_{DHR}$ | Read Data Hold Time | 20 | - | - | ns |
| $t_{OH}$ | Output Disable Time | - | - | 70 | ns |
| $t_{ACC}$ | Access Time | - | - | 140 | ns |
| $t_{PWLR}$ | Read Low Time | 150 | - | - | ns |
| $t_{PWLW}$ | Write Low Time | 60 | - | - | ns |
| $t_{PWHR}$ | Read High Time | 60 | - | - | ns |
| $t_{PWHW}$ | Write High Time | 60 | - | - | ns |
| $t_R$ | Rise Time | - | - | 15 | ns |
| $t_F$ | Fall Time | - | - | 15 | ns |
| $t_{CS}$ | Chip select setup time | 0 | - | - | ns |
| $t_{CSH}$ | Chip select hold time to read signal | 0 | - | - | ns |
| $t_{CSF}$ | Chip select hold time | 20 | - | - | ns |

**8080-series MCU parallel interface characteristics**



Write cycle

Read cycle
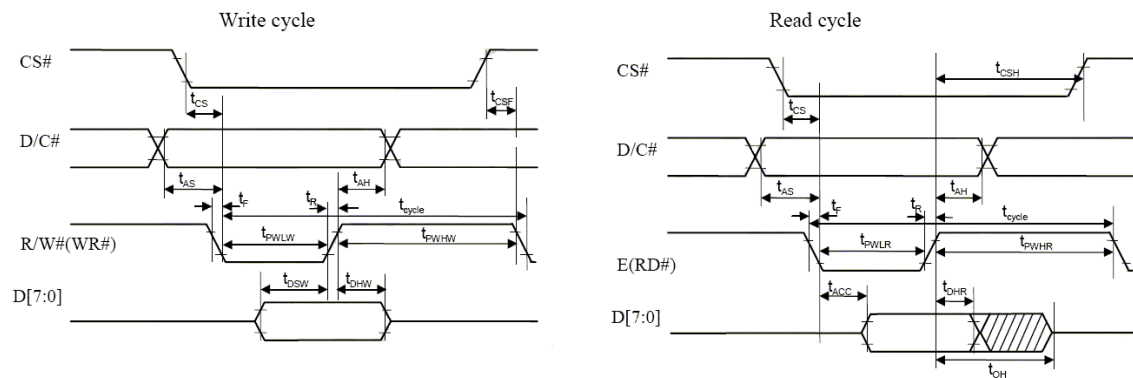
## 8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

### 8.1 POWER ON / OFF SEQUENCE

*Power ON sequence:*

1. Power ON $V_{CI}$.
2. After $V_{CI}$ becomes stable, set wait time at least 1ms ($t_0$) for internal $V_{DD}$ become stable. Then set RES# pin LOW (logic low) for at least 100us ($t_1$) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us ($t_2$). Then Power ON $V_{CC}$. [1]
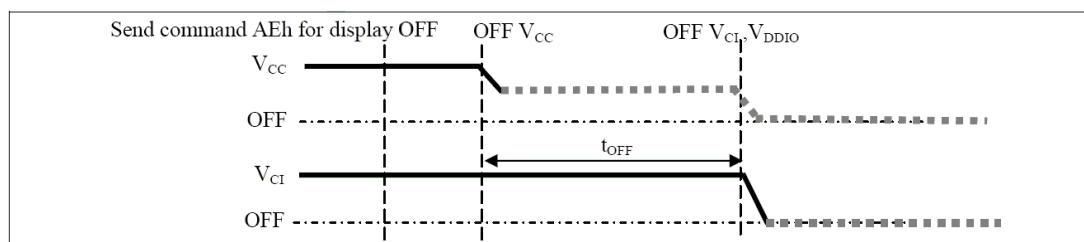4. After $V_{CC}$ become stable, send command AFh for display ON. SEG/COM will be ON after 200ms($t_{AF}$).

The Power ON sequence.
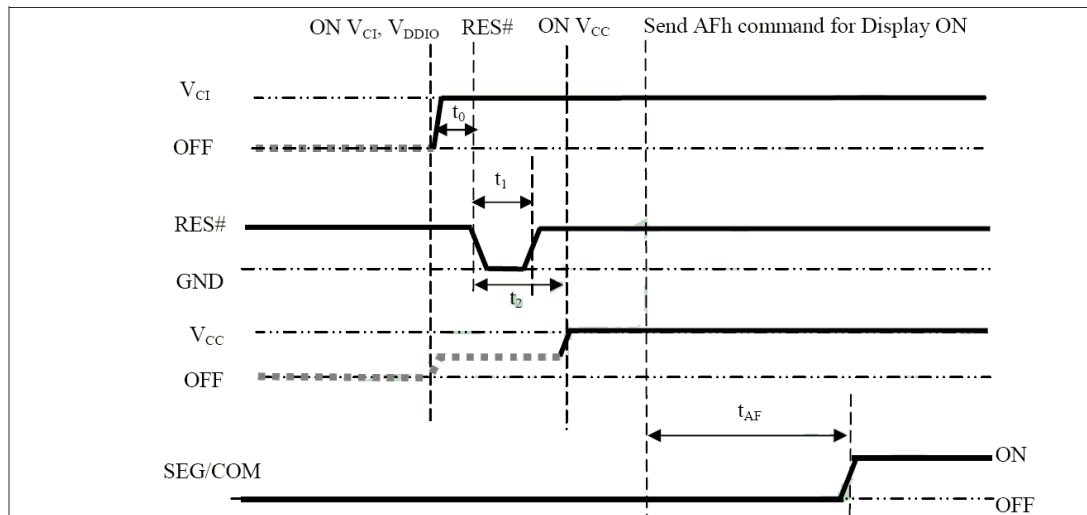


*Power OFF sequence:*

1. Send command AEh for display OFF.
2. Power OFF $V_{CC}$. [1], [2], [3]
3. Wait for $t_{OFF}$. Power OFF $V_{CI}$.(where Minimum $t_{OFF}$=80ms [5], Typical $t_{OFF}$=100ms)

The Power OFF sequence



**Note:**

(1) Since an ESD protection circuit is connected between $V_{CI}$ and $V_{CC}$, $V_{CC}$ becomes lower than $V_{CI}$ whenever $V_{CI}$ is ON and $V_{CC}$ is OFF as shown in the dotted line of $V_{CC}$ in above figures.
(2) $V_{CC}$ should be kept disable when it is OFF.
(3) Power pins ($V_{CI}$, $V_{CC}$) can never be pulled to ground under any circumstance.
(4) The register values are reset after $t_1$.
(5) $V_{CI}$ should not be Power OFF before $V_{CC}$ Power OFF

## 8.2 APPLICATION CIRCUIT

| U1 | | |
| --- | --- | --- |
| 24 VCC | GPIO 4 | GPIO |
| 2 VCC | D7 23 | D7 |
| 3 VCOMH | D6 22 | D6 |
| 5 VCI | D5 21 | D5 |
| | D4 20 | D4 |
| 10 IREF | D3 19 | D3 |
| 6 VDD | D2 18 | D2 |
| 7 BS1 | D1 17 | D1 |
| 8 BS2 | D0 16 | D0 |
| | CS# 11 | CS# |
| | RES# 12 | RES# |
| 25 VSS | D/C 13 | D/C |
| 9 VSS | WR# 14 | WR# |
| 1 VSS | RD# 15 | RD# |
| P22102 | | |

VCC
VCI
C1  C2  C3  R1  C4
VSS
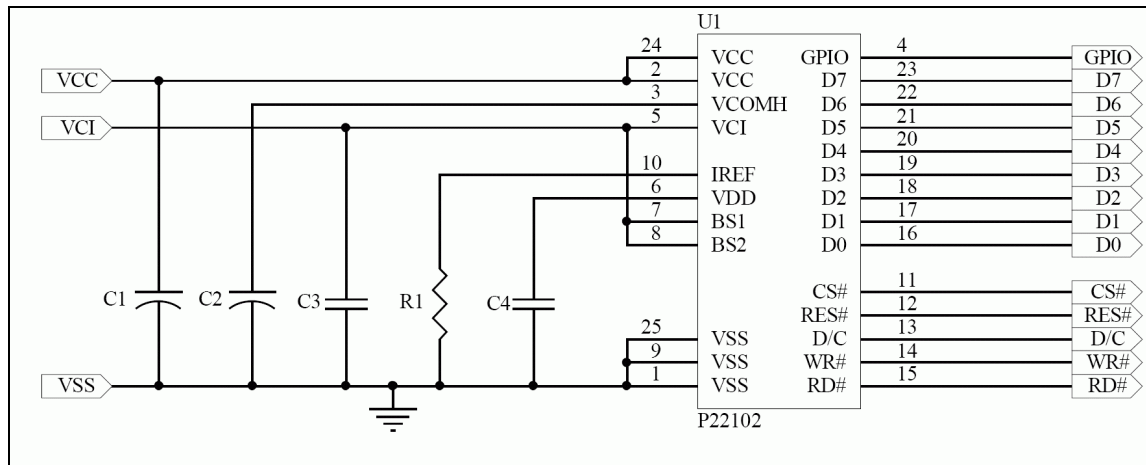
**Component:**

C1, C2: 4.7uF/35V(Tantalum type) or VISHAY (572D475X0025A2T)

C3, C4: 1uF/16V(0603)

R1: 1M ohm (0603) 1%

**This circuit is for 8080 8bits interface.**

## 8.3 COMMAND TABLE

Refer to IC Spec.: SSD1327

## 9. RELIABILITY TEST CONDITIONS

| No. | Items | Specification | Quantity |
|---|---|---|---|
| 1 | High temp. (Non-operation) | 85°C, 240hrs | 5 |
| 2 | High temp. (Operation) | 70°C, 120hrs | 5 |
| 3 | Low temp. (Operation) | -40°C, 120hrs | 5 |
| 4 | High temp. / High humidity (Operation) | 65°C, 90%RH, 120hrs | 5 |
| 5 | Thermal shock (Non-operation) | -40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles | 5 |
| 6 | Vibration | Frequency : 5~50HZ, 0.5G<br>Scan rate : 1 oct/min<br>Time : 2 hrs/axis<br>Test axis : X, Y, Z | 1 Carton |
| 7 | Drop | Height: 120cm<br>Sequence : 1 angle、3 edges and 6 faces<br>Cycles: 1 | 1 Carton |
| 8 | ESD (Non-operation) | Air discharge model, ±8kV, 10 times | 5 |

**Test and measurement conditions**

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

**Evaluation criteria**

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

# 10. EXTERNAL DIMENSION

**Specification**
1. Display: OLED(White)
2. Dot Matrix: 128x128
3. Dot Size: 0.19x0.19mm
4. Dot Pitch: 0.21x0.21mm
5. Aperture Rate: 82%
6. Active Area: 26.86x26.86mm
7. IC: SSD1327Z

**Pin Assignment**

| NO. | SYMBOL |
|-----|--------|
| 1 | VSS |
| 2 | VCC |
| 3 | VCOMH |
| 4 | GPIO |
| 5 | VCI |
| 6 | VDD |
| 7 | BS1 |
| 8 | BS2 |
| 9 | VSS |
| 10 | IREF |
| 11 | CS# |
| 12 | RES# |
| 13 | D/C |
| 14 | WR# |
| 15 | RD# |
| 16 | D0 |
| 17 | D1 |
| 18 | D2 |
| 19 | D3 |
| 20 | D4 |
| 21 | D5 |
| 22 | D6 |
| 23 | D7 |
| 24 | VCC |
| 25 | VSS |

SEG & COM Layout

128x128 Dots(1.5")

Handler 15x5x0.15mm
AG Polarizer t=0.19mm
Symbio.Inc. PO6B (Silver) 16x4x0.07mm
Seal Cover IC,white
Seal,white
Contact Side Plating:Ni-Au

1.41±0.1 (w/o Handler)
5.7 Max.
1.5 Max.

33.8±0.2
32.8±0.3 (AG Polarizer)
28.86 (V/A)
P0.21x128-0.02=26.86(A/A)

36.5±0.2
30.8±0.2 (Civer Glass)
29.8±0.3(Polarizer)
28.86 (V/A)
P0.21x128-0.02=26.86(A/A)

W=0.65x(25-1)=15.6±0.05
P0.65x(25-1)=15.6±0.05
17.5±0.1(Alignment hole)
18.9±0.3

2-Ø0.8±0.1
Ø0.2(PTH)
R0.225
1.65±0.1

0.5±0.3
0.6±0.1
2±0.3
3.2±0.2

Pin 1

| | Revision | Date | Note |
|---|----------|------|------|
| | | 2008/05/29 | Module Ass'y(EPR0800125A,ASR0800019) |

CONFIDENTIAL
Third Angle Projection

| General Tolerance | |
|---|---|
| Length (mm) | Tolerance(mm) |
| 0 ~ 8 | ±0.1 |
| 8 ~ 25 | ±0.2 |
| 25 ~ 50 | ±0.3 |

| | |
|---|---|
| Scale | 2.5:1 |
| Unit | mm |
| Sheet | 1/1 |

Module — Valerie Lo
Spec. — HC Lin
Approved — Strong Tsai
M.E. — Valerie Lo
E.E. — Kevan Huang

PROJECT CODE: P22102
PART NAME: Module Ass'y
PARTS NO.: 9822102000
REVISION: 01

RITEK GROUP
RiTdisplay Corporation

## 11. PACKING SPECIFICATION

**TBD**

## 12. APPENDIXES

### APPENDIX 1: DEFINITIONS

### A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

### B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

### C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.
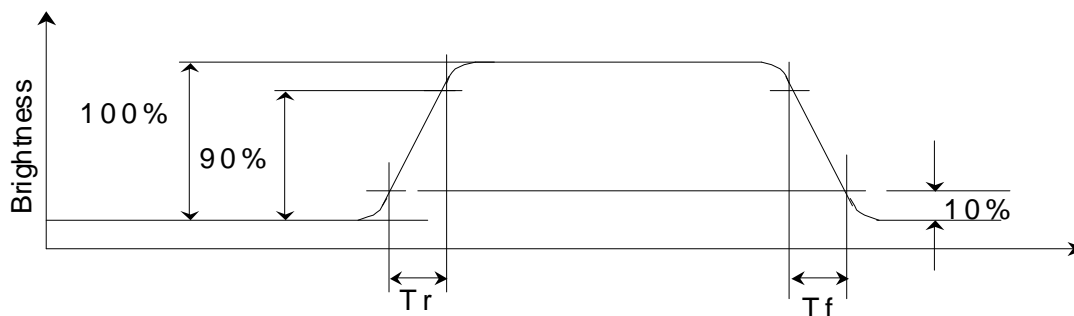


**Figure 2 Response time**

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## D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.
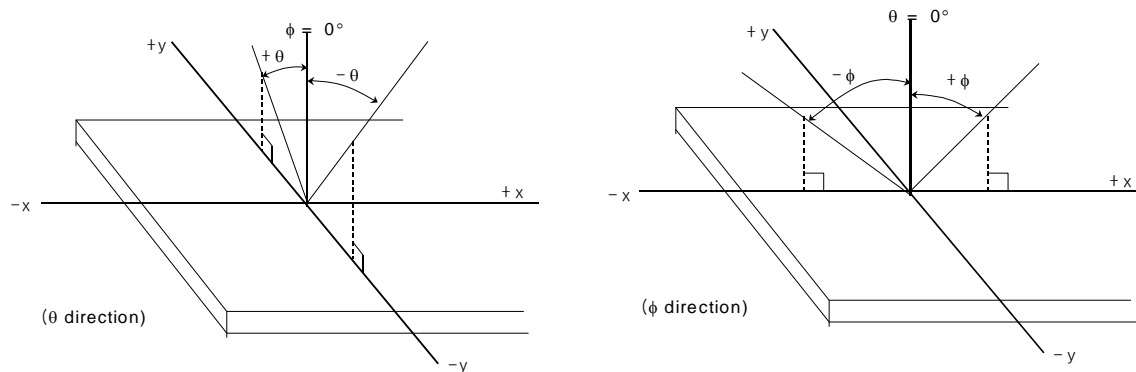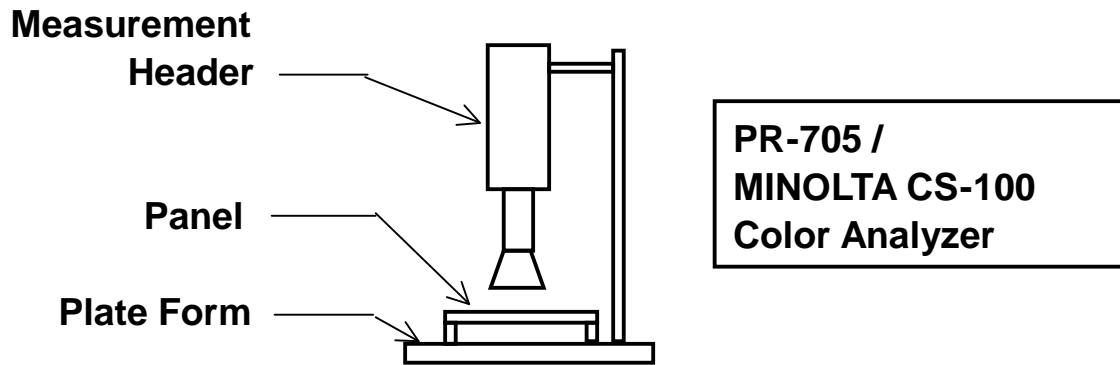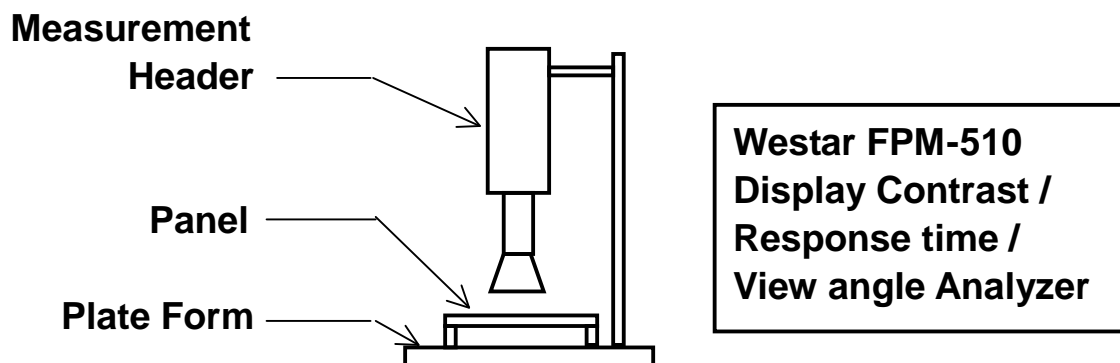


**Figure 3 Viewing angle**

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## APPENDIX 2: MEASUREMENT APPARATUS

### A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

**Measurement Header**

**Panel**

**Plate Form**

PR-705 /
MINOLTA CS-100
Color Analyzer

### B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510

**Measurement Header**

**Panel**

**Plate Form**

Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer

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## C. ESD ON AIR DISCHARGE MODE

R 330 ohms   ESD

DISCHARGE
TIP

V

C
150pF

EUT

RETURN

GROUND PLANE
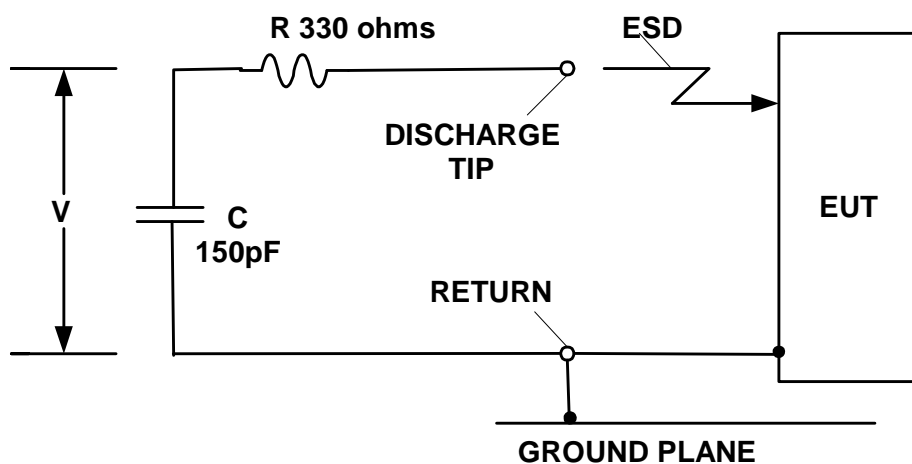
## APPENDIX 3: PRECAUTIONS

### A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.