Application note for the Philips Real Time Clocks PCF8563,73,83,93

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Directory

1. Introduction

The RTCs from Philips have a long tradition and are used in numerous application fields. Starting from VCRs, burglar alarm system and water sprinklers to (platform) timers and telecom applications such as mobile phones. The timer function is used in applications to save current, to just wake up the system periodically to check if any actions are required. Other applications are also in watch-dog function. The continues trend to lower the power consumption is followed by integrating on the evolving new semiconductor processes and by constantly researching and applying latest circuitry technologies
The focus of this paper is on the latest device from Philips Semiconductors the PCF8563. Never the less comparisons to the other devices are done where appropriate.

2. Comparison

Features	PCF8563	PCF8573	PCF8583	PCF8593
I^2C-bus interface speed	400kHz	100kHz	100kHz	100kHz
Scratch pad RAM	0	0	248 Bytes	0
Years and leap year tracking	yes	no	yes	yes
Year counter	2 digit +1 bit	no	2 bit	2 bit
1/10, 1/100 s counter	no	no	10ms	10ms
Programmable alarm	yes	yes	yes	yes
Low voltage detector	yes	no	no	no
Supply voltage for I2C-bus	1.8 – 5.5V	2.5– 6.0V	2.5– 6.0V	2.5– 6.0V
Supply voltage for clock	1.0 – 5.5V	1.1–6.0V	1.1–6.0V	1.1–6.0V
Typical power consumption	250nA @ VDD=1V	3µA@1.5V 12µA@5V	2µA@1.0V 10µA@5V	1µA@2.0V 4µA@5V
Packages	DIL/SO8 TSSOP8	DIL/SO16	DIL/SO8	DIL/SO8

3. Features

The RTCs include:

- 32kHz oscillator control for quartz crystals,
- Counters covering seconds to years. In addition a counter / timer can be used for accurately triggering of timed applications.
- Internal power-on-reset circuit
- Programmable clock output for peripheral devices: 32.768kHz, 1024Hz, 32Hz and 1Hz. (PCF8563 ony)
- Low stand-by current with operating clock: typical consumption of only 250nA @ VDD=3.0V and Tamb=25°C.

4. Power-on-reset

There is no analog power on reset circuit. The reset is finished as soon as the oscillator is running. If the oscillator is stopped the RTC is reset, this can be avoided by initiating the POR override mode.

5. Oscillator

- Description, principle of operation.
  The oscillator is built on the principle of PIERCE. The crystal is in the feedback loop, generating the necessary phase shift at the specific frequency. The resonating frequency can be pulled by a variable capacitor connected to ground. (For PCF 8583 and PCF8593 it is better to connect it to VDD). The RTC is optimized for low power consumption at VDD = 2-3V and works down to 1V. The equivalent diagram to determine the resonance frequency is in Fig. 1

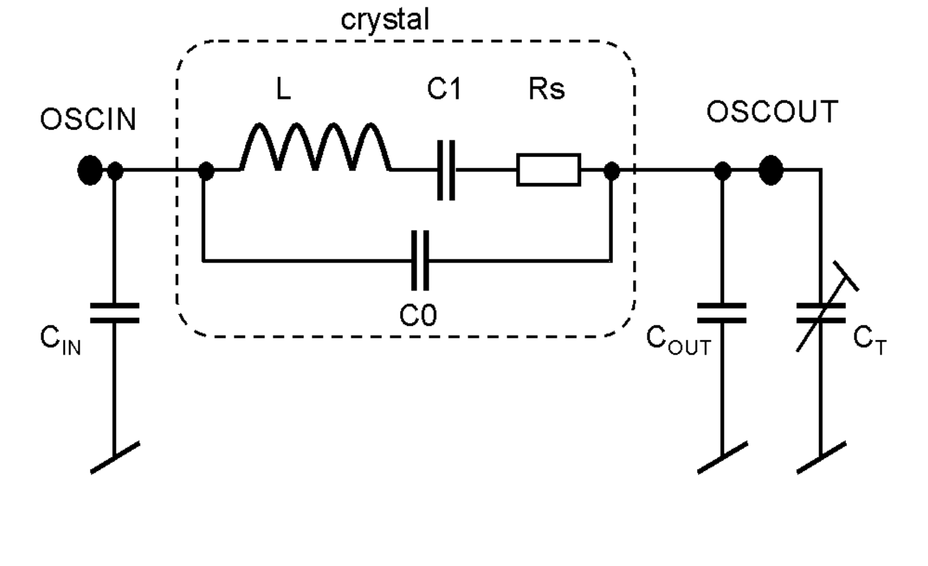

Fig. 1 oscillator equivalent diagram

The estimations of the impact of the different circuit elements to the accuracy were executed with the following equations:

The frequency is given by: C_{IN}

$$\omega = \frac{1}{\sqrt{L*C}} \quad , \omega = 2\,\pi\,f_0 \qquad (1)$$

$$C = C1 \,//\, (\,C_{IN} \,//\, (\,C_{OUT}+C_T) + C0) \qquad (2)$$

$$C_{IN} \,//\, (C_{OUT}+C_T) = \frac{C_{IN}*(C_{OUT}+C_T)}{C_{IN}+C_{OUT}+C_T} \qquad (3)$$

$$C = \frac{C1*(\frac{C_{IN}*(C_{OUT}+C_T)}{C_{IN}+C_{OUT}+C_T}+C0)}{C1+\frac{C_{IN}*(C_{OUT}+C_T)}{C_{IN}+C_{OUT}+C_T}+C0} \qquad (4)$$

$$Q = \frac{1}{w*C}*\frac{1}{Rs} \text{ ; or first order approximation: } Q_a = \frac{1}{w*C1}*\frac{1}{Rs} \qquad (5)$$

Taking the figures from the table below we receive:

$$L = \frac{1}{(2*p*fo)^2*C1} = 7900\text{ H}, \qquad Q_a = 29000.$$

This explains well why the starting up and stopping of the oscillator can take hundreds of milliseconds.

Typical values:

Parameter	value	Unit	source	parameter	value	unit	source
f_0	32768	Hz	1)	Aging: Δf/f	±5	ppm	1)
Δf/f	±100	ppm	1)	C_T variable	4…25	pF	2)
C1	3.0	fF max	1)	C_T, tc	300	ppm/°C	2)
C_{IN}*	25±10	pF	0)	C_T variable	5…30	pF	3)
C_{IN}, tc	+47	ppm/°C	0)	C_T fixed 0603	any	pF	4)
C0	1.5	pF max	1)	C_T fixed, tc	±30	ppm/°C	4)
Rs	55	kΩ	1)	C_{OUT}	4…7	pF	0)

* PCF8563 named C_{IN} is $C_{L\ (integrated)}$

Sources:

0) Philips Semiconductors data sheet PCF8563, April 1999
1) Quartz product catalog 'Thy crystal master' EPSON 1996/1997
2) MuRata TZB04 trim capacity (Farnell components)
3) Philips Components, CV05 trim capacity, (Farnell components)
4) Philips Components, ceramic multilayer capacitor

- Selecting a crystal.
  Select a crystal with characteristic as:
  Frequency: 2^{15} Hz=32768Hz
  Tolerance of e.g. ± 20 to 100ppm is ok, since it can be compensated.
  Series impedance R1 max = 40kΩ, if you take one with up to 100kΩ the current consumption will slightly increase, even then no starting up problems are expected. Currently SMD crystals with low R1 are hard to find.
  (check also paragraph 'modes which don't work' below)

- Accuracy dependence.
  How accurate is accurate!
  A clock going fast 1s / day has an accuracy of 1/24*3600= 11.57ppm. 1s/week = 1.65ppm 1s/month = 0.4ppm and 1s/year = 0.031ppm. In contrast a good mechanical watch is better than 12s/day or 1300ppm and a Cesium frequency normal has an accuracy in the order of 10^{-6} ppm or better.
  The clock accuracy dominantly depends on the parameters of the resonating quartz crystal. The frequency tolerance is compensated by the tuning capacitor C6. The temperature coefficient of the capacitor has almost no effect. The largest effect comes from the temp coefficient of the crystal. 32kHz crystals are always of the type tuning fork. They have in contrast to the AT-cuts a bell shaped curve with the maximum frequency at 28°C resulting that with lower or higher temperature the frequency decreases. For wrist watches not to bad since the temperature at the wrist is about 28°C and almost stable. Figure 2. compares the size of the different spreads and variations.

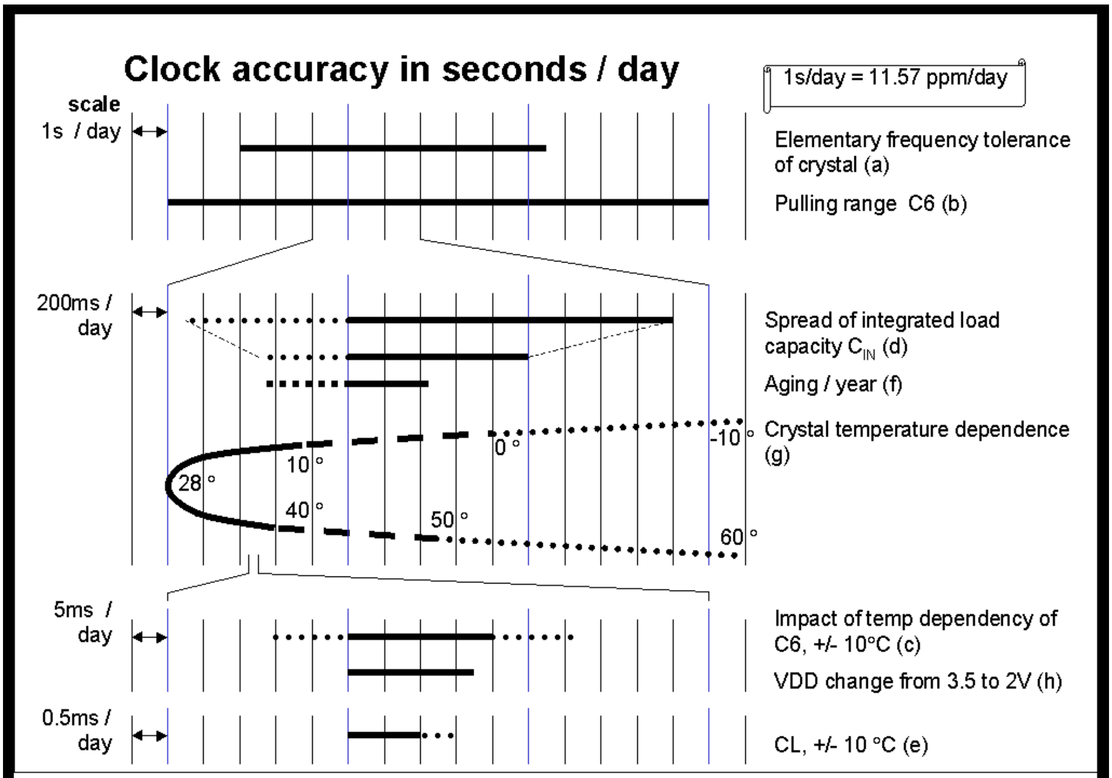

Fig. 2 Time accuracy

(a) The production spread of the crystal can be compensated by adjusting the pulling capacitor C6.
(b) The pulling range is large enough to compensate for a spread of ±100ppm.
(c) The variable capacitors have a typical temperature coefficient of ±300 to 500 ppm / °C. This capacity change has a very small influence to the accuracy. The solid line shows the impact if C6 is small. If C6 is large the variation is larger, shown with the dotted lines.
(d) The internal capacitor has a finite production tolerance influencing the accuracy depending on the tuning capacitor C6. When once compensated it is very stable (e)
(e) The internal capacitor has a very small temperature coefficient shifting the frequency almost nil.
(f) The accuracy can degrade over the years due to aging of the crystal. After a year it could be fast or slow by about 0.4s/day.
(g) The largest impact has the temperature response of the crystal.
(h) The impact of the change in VDD is small: e.g. with ΔVDD=1.5V the clock speed will change only about 17ms/day.

Consequence: place the crystal and the IC circuit at the spot with the least temperature variations.

- Modes which don't work:
  To keep time with an accuracy in the ppm range only quartz crystals can be considered. The oscillator circuit is not designed for operating with RC, LC or ceramic resonators. To design a very low power crystal oscillator requires a different set of parameters compared to an universal oscillator accepting crystals, RC, LC or ceramic resonators.

6. Oscillator tuning

The PCF8563 has the option to output the buffered xtal frequency to the pin CLK out, set the register 0DH 'CLKOUT frequency' to 80H.
The frequency can now be tuned by adjusting the variable capacitor C. Note: Touching the adjustment screw often causes the capacitance to shift.

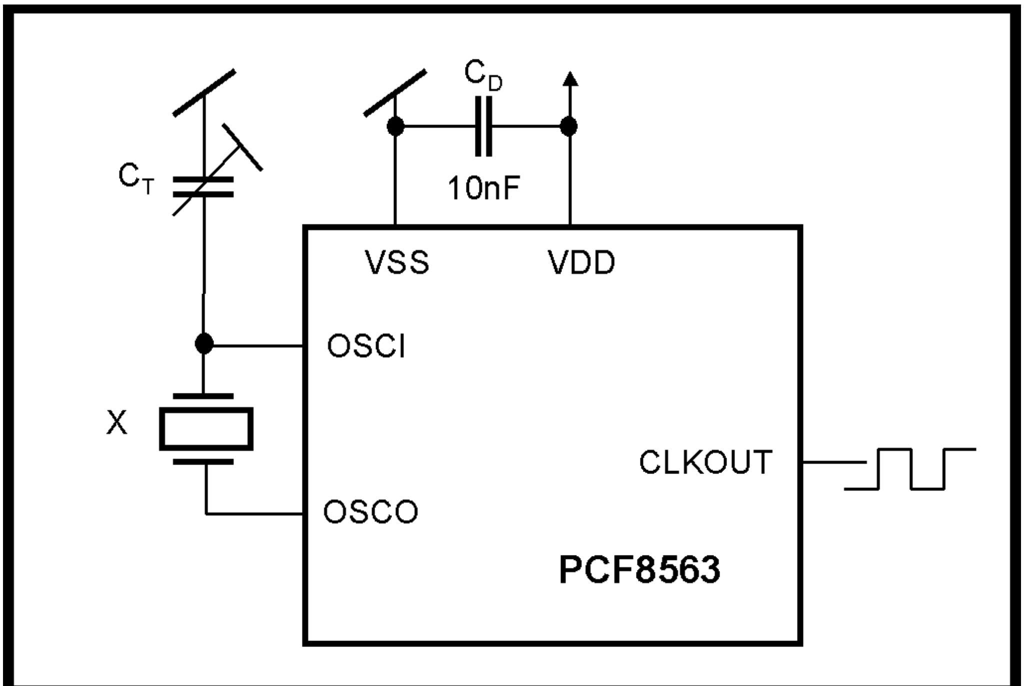

Fig. 3 oscillator tuning

Accuracy:
If the clock should go correctly to 1s per day you need at least an 8 digit frequency counter with an accuracy of 1ppm. 1ppm = 32.768mHz,
+1ppm = 32768.0327Hz,
-1ppm = 32767.9673Hz. (1 day has 86400s,1s/day→ 11.6ppm)
Tune the oscillator at the average operation temperate of the application.
The 8573 can be tuned by monitor the 128Hz signal at the FSET output.
Tuning the 83, 93 is some what more difficult, since no buffered high frequency signal is available. There are three different options:

- Measure the period of the 1s output signal, this however is time consuming.

- Attach the frequency counter probe to the OSCO pin. This adds capacity to the OSCO-pin and lowers (detunes) the oscillator frequency by Δf. The frequency adjustment has then to be lower by Δf.
- In the watch industry the frequency is coupled out acoustically. A sensitive microphone is placed near the crystal. The signal is then fed as input to the tuning gear.
- The method described in the **8583** and **8593** data sheet 14.1.2 only works well when dT is an integer figure of seconds. The 1/10s and 1/100s are derived of a combination of 1, 2, 4, 8, 16, 32,… Hz signals. The accuracy is therefor only < ±5ms. Generating an alarm after T + dT, dT=20ms a jitter of plus or minus 5ms can be detected, this makes it very complicated for automatic tuning.

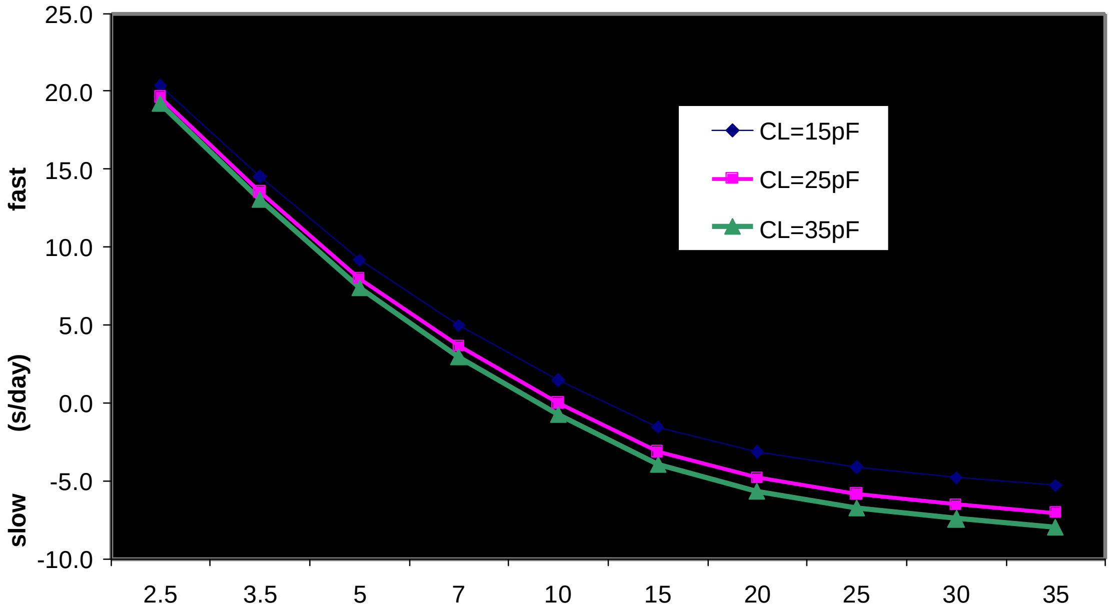

Fig 4. Tuning range

7. Y2K

The PCF8563 has a two digit year counter plus one bit for the century. In the year 2000 the counter will turn over from 99 to 00 and toggle the century bit. (19=1, 2000=0).
PCF8583 and 8593 have a 2 bit counter for the leap year. Since the year 2000 is also a regular leap year the clock does not face any irregularity in respect to the calendar.
PCF8573 has a resolution of maximum month. Leap year and year must be tracked by system software.

8. Initialization

Setting the clock is a straight forward procedure, setting first the mode and then the actual time: e.g Friday, July 16 1999, 2’45 pm

Binary	Hex	addr	comments
			generate I^{2}C-bus start condition
1 0 1 0 0 0 1 W	A2		slave address
0 0 0 0 0 0 0 0	00		word address 0, next bytes are data
0 0 0 0 0 0 0 0	00	00	control/status1, no test modes or POR override
0 0 0 0 0 0 0 0	00	01	control/status2, no alarm/timer flags and interrupts
0 0 0 0 0 0 0 0	00	02	setting seconds clear the voltage low detector
0 1 0 0 0 1 0 1	45	03	setting minutes
0 0 0 1 0 1 0 0	14	04	setting hours to 14
0 0 0 1 0 1 0 1	16	05	setting days to 16
0 0 0 0 0 1 0 1	03	06	setting weekdays to Friday
1 0 0 0 0 1 1 1	07	07	setting month to 7 and century bit to 1
1 0 0 1 1 0 0 1	99	08	setting years to 99
1 0 0 0 0 0 0 0	80	09	alarm values reset to 00
1 0 0 0 0 0 0 0	80	0A	alarm values reset to 00
1 0 0 0 0 0 0 0	80	0B	alarm values reset to 00
1 0 0 0 0 0 0 0	80	0C	alarm values reset to 00
1 0 0 0 0 0 0 0	00	0D	setting frequency out to 32768Hz e.g. for tuning
0 0 0 0 0 0 0 0	00	0E	timer switched off
			generate I^{2}C-bus stop condition

9. Alarm

Lets take the example to set an alarm such that always 15 minutes past the hour the alarm flag AF is set and an interrupt is generated.

Binary	Hex	addr	comments
			generate I^{2}C-bus start condition
1 0 1 0 0 0 1 W	A2		slave address
0 0 0 0 1 0 0 1	09		word address 9 for minute alarm.
0 0 0 1 0 1 0 1	15	09	Minute alarm enabled and set for 15 minutes
1 0 0 0 0 0 0 0	80	0A	hour alarm is disabled
1 0 0 0 0 0 0 0	80	0B	day alarm is disabled
1 0 0 0 0 0 0 0	80	0C	weekday alarm is disabled
			generate I^{2}C-bus start condition
1 0 1 0 0 0 1 W	A2		slave address
0 0 0 0 0 0 0 1	01		word address 1, next bytes are data
0 0 0 0 0 0 1 0	02	01	control/status2, clear alarm flag and enable alarm interrupt
			generate I^{2}C-bus stop condition

Remark: The interrupt is only set at the counter transition from 14 to 15. This is indicated by the dashed line in Fig 5. The interrupt has to be reset by software.

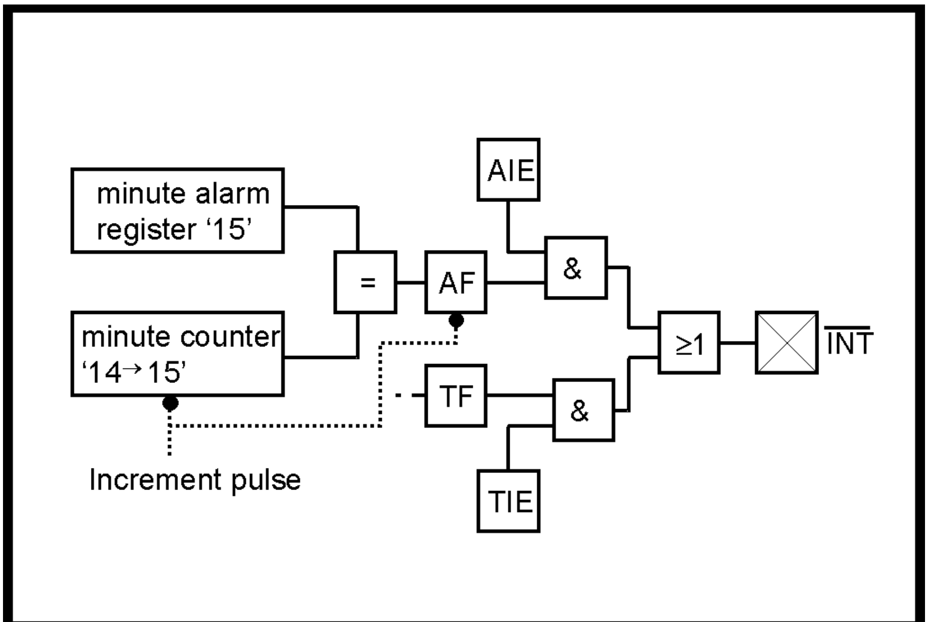

Fig. 5 Alarm (Timer) function

10. Timer

The internal timer is an 8 bit countdown timer. It can be clocked by 4 different clock frequencies: 4096,64,1 or 1/64Hz.
The example generates an interrupt after 10ms:
Clock to be used 4096 Hz, number of clock pules needed = .01*4096=40, Error = 40/4096Hz – 0.01= - 234us, length of I2C-bus initialization: 3 start-conditions, 3 pulses each + 9 bytes, 9 pulses each=90 clocks @ 400kHz = 225µs. Creating the clock asynchronously also gives an error of up to 1 clock pulse. The interrupt will start an out-put pulse after 9.991ms or if counter is set to 41 the interrupt will start after 10.236ms.

The timer is started by the acknowledge of the start timer instruction.

Binary	Hex,addr,comments		
			generate I^{2}C-bus start condition
1 0 1 0 0 0 1 W	A2		slave address
0 0 0 0 0 0 1 0	02		word address 02
0 0 0 0 0 0 0 1	01	02	clear all flags, enable timer interrupt
			generate I^{2}C-bus start condition
1 0 1 0 0 0 1 W	A2		slave address
0 0 0 0 1 1 1 1	0		word address 0F for timer value
0 0 1 0 1 0 0 0	28	0F	timer value set to 40, 28h
			generate I^{2}C-bus start condition
1 0 1 0 0 0 1 W	A2		slave address
0 0 0 0 1 1 1 0	0E		word address 0E for timer control byte
1 0 0 0 0 0 0 0	80	0E	select clock frequency and start timer
			generate I^{2}C-bus stop condition

11. PC-board layout

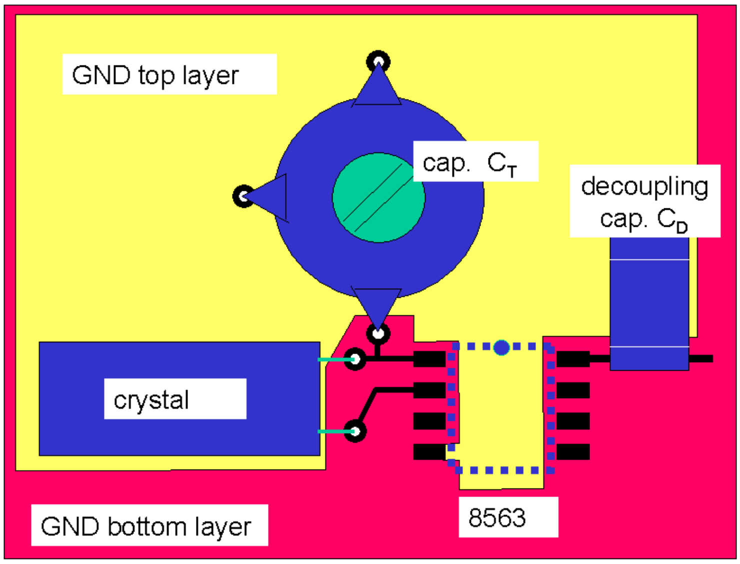

Fig. 6 PC-board layout proposal for

The high impedance inputs of the oscillator are sensitive to pick-up of spikes, resulting in the clock running fast. The best preventive measure is to shield the oscillator circuit and keep the connections to OSCI and OSCO at an absolute minimum. The crystal case of 8563,83,93 can be soldered to GND and for 8573 to V_{DD}.

12. Partial circuit switch down, (protection diodes)

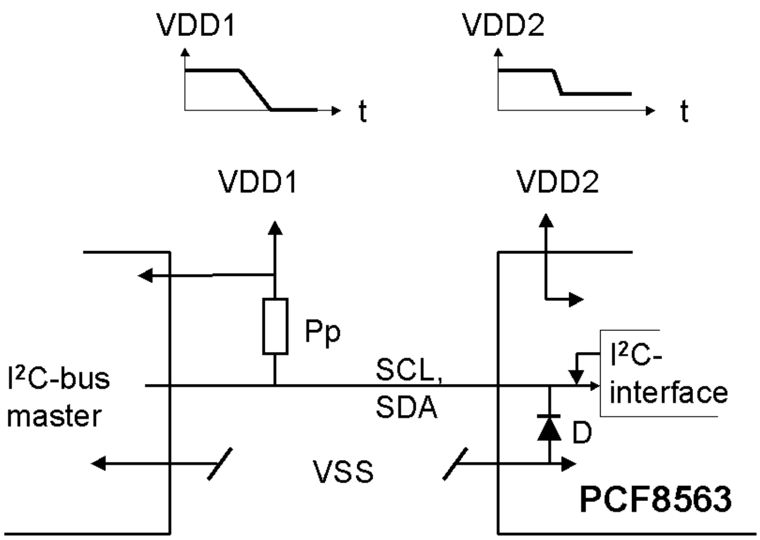

Fig. 7 protection

The Clock circuits PCF8563,and 8593 have on the pads SDA,SCL and INT a protection circuit with no diode to VDD. This allows to partially switch off the VDD. E.g. During operation the complete application is powered by 3.3V, then during stand-by just the RTC is operating and powered from a 0.47F-capacitor, which then will be slowly discharged to 1.5V. Check Fig 7 and 8. PCF8583 has no protection diode to VDD and the INT pin, but has diodes to VDD and the SCL, SDA pins!

13. Hints to keep power consumption low

Power can be saved by applying several different measures:

- Select PCF8563
- Use lowest possible $V_{DD,}$ Check Fig.8. A low leakage diode is charging a super cap of e.g. 0.47F, during standby the cap is supplying the RTC
- Access the RTC as little as reasonable, to reduce the dynamic current from the I^2C-bus
- Design I^2C-bus pull-up resistors as large as possible:
  The determining factor is the rise time. For 100 / 400 kHz I2C-bus it is 1000 / 300 ns. It is a product of the bus line capacitance (track capacitance) and the value of the pull-up resistor. First estimate the capacities:

Capacities:			
Microcontroller pin capacity	Ci	7	pF
RTC pin capacity	Ci	7	pF
Track (calculation below)	Ct	0.9	pF
Total	C =	14,9	pF

Track capacity for a track 3cm long, 0.5mm wide on copper backed 0.7mm strong PC-board made out of FR4 glass epoxy:

$$Ctr = \frac{e0 * er * A}{t} = \frac{8.85 * 10 ** (-12) * 4.6 * 0.03 * 0.0005}{0.0007} = 0.9pF$$

rise time 10..90% tr= 2 R Ctr,

400kHz I2C-bus: $R_{400kHz} = \frac{tr}{2C} = \frac{300ns}{2 * 14.9\,pF} = 10k\Omega$,

100kHz I2C-bus: $R_{100kHz} = \frac{1000ns}{2 * 14.9\,pF} = 33k\Omega$

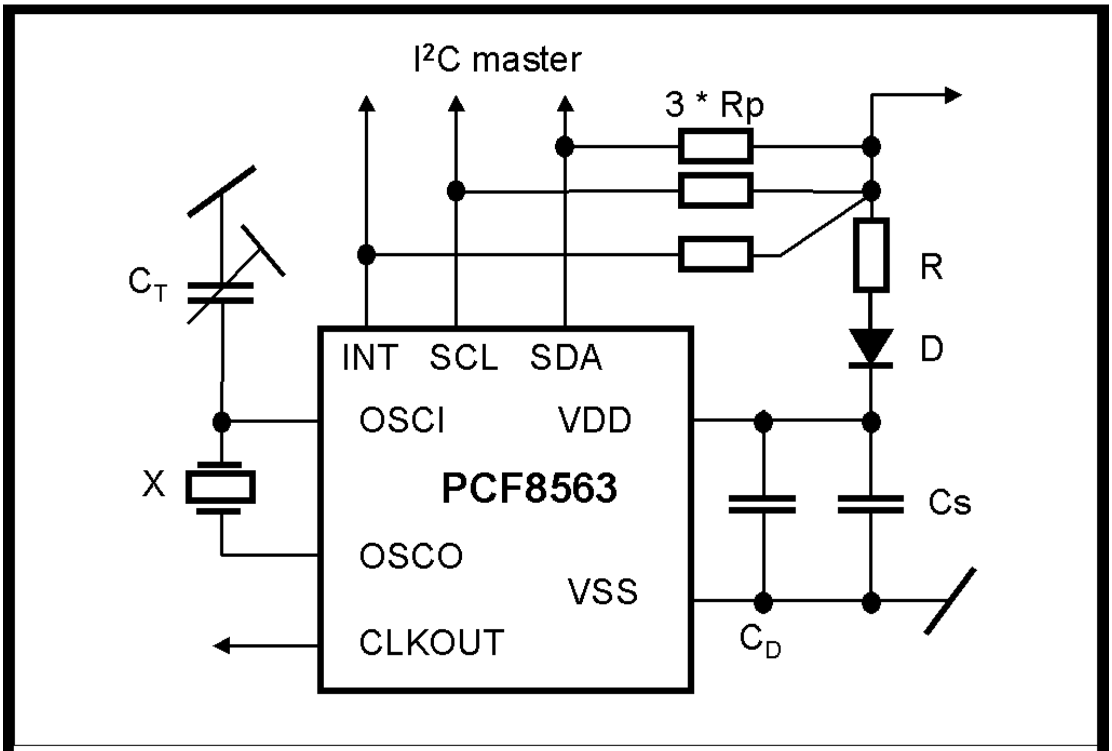

Fig. 8 application diagram

15. References:

Philips product specification PCF8563, 16. April 1999
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