Design Type III Compensation Network For Voltage Mode Step-down Converters

Introduction

This application note details how to calculate a type III compensation network and investigates the relationship between phase margin and load transient response for the AnalogicTech family of voltage mode control step-down converters. This family includes the AAT1184, AAT1185, AAT1189, AAT2687, AAT2688, and AAT2689. Voltage mode control has become a very popular topology for DC to DC converters, especially with low noise output systems including DSL and cable modems, notebook computers, satellite set-top boxes, and wireless LAN systems.

Background

In order to reduce the DC-DC converter's output voltage ripple, the equivalent series resistance (ESR) of the output capacitor needs to be reduced. Ceramic output capacitors have a very small equivalent series resistance (ESR), low cost, and small size, making them the ideal output filter solution for DC-to-DC converters. However, the use of low ESR ceramic capacitors significantly affects the design of the error amplifier in the feedback loop. The power stage consists of a double pole due to the L C_{OUT} filter and an ESR zero. The ESR zero is pushed far away from the double pole frequency which results in inadequate phase margin at the cross-over frequency. Therefore, type III compensation is used to stabilize the loop and optimize the output transient response to dynamic load changes.

Voltage Mode Control Loop

As illustrated in Figure 1, a typical voltage mode control loop has three main stages: step-down power stage, compensation network, and PWM modulator. The Type III compensation network generates two zeros and two poles. The two zeros are placed from 60% to 150% of double pole frequency to counter the 180° phase lag due to the L C_{OUT} output filter. The two poles are set at the switching frequency of the converter to nullify the ESR zero and attenuate the high frequency noise.

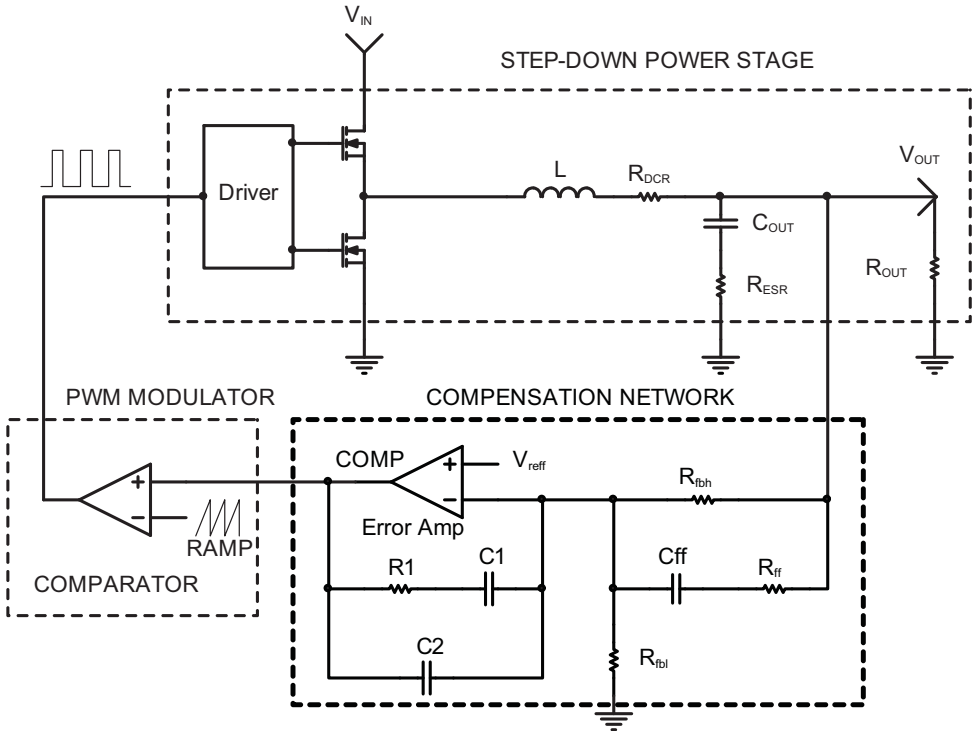

Figure 1: Closed Loop Step-Down Converter with Type III Network Compensation.

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Step-Down Power Stage Transfer Function

The transfer function of the power stage of the step-down converter can be determined by the voltage division:

Eq. 1: $$\frac{V_{OUT}}{V_{IN}} = \frac{Z_{OUT}}{Z_L + Z_{OUT}}$$

Where Z_L and Z_{OUT} are the inductor impedance and output impedance of the power stage. The R_{DCR} includes the DC winding resistance, the turn-on resistance of the MOSFET, and the trace resistance. R_{ESR} is the equivalent series resistor of the output capacitor. Z_L and Z_{OUT} are calculated using Equations 2 and 3.

Eq. 2: $$Z_{OUT} = R_{LOAD} // \left(R_{ESR} + \frac{1}{sC_{OUT}}\right) = \frac{s \cdot C_{OUT} \cdot R_{LOAD} \cdot R_{ESR} + R_{LOAD}}{s \cdot C_{OUT} \cdot (R_{LOAD} + R_{ESR}) + 1}$$

Eq. 3: $$Z_L = s \cdot L + R_{DCR}$$

Where the complex variable $s = j \cdot \omega$ and $j = \sqrt{-1}$

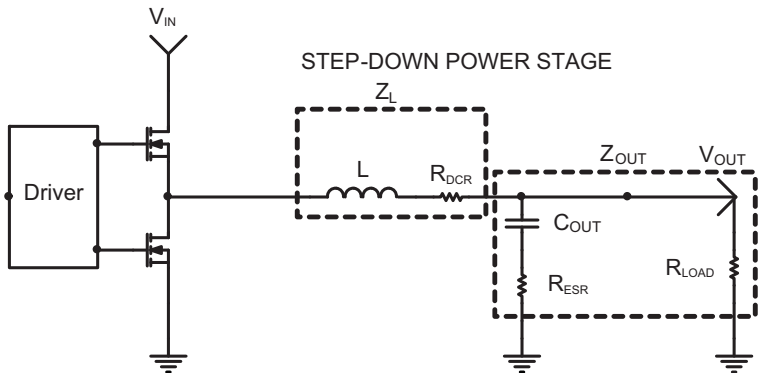

Figure 2: Step-Down Converter Power Stage.

The step-down power stage open loop gain is given by substituting Equations 2 and 3 into Equation 1. Algebraic manipulation yields the following expression for the open-loop transfer function of the power stage:

Eq. 4: $$G_P = \frac{V_{OUT}}{V_{IN}} = \frac{R_{LOAD} \cdot (s \cdot C_{OUT} \cdot R_{ESR} + 1)}{s^2 \cdot L \cdot C_{OUT} \cdot (R_{LOAD} + R_{ESR}) + s\{L + C_{OUT} \cdot [R_{DCR}(R_{LOAD} + R_{ESR}) + R_{LOAD} \cdot R_{ESR}]\} + R_{LOAD} + R_{DCR}}$$

A typical Bode plot of the step-down converter power stage is illustrated in Figure 3. A double pole at the cut-off frequency causes the gain to roll off with a -40dB/decade slope (blue) and the phase to exhibit a very sharp slope downward from 0 degree to -180 degree phase lag (red). The ESR zero is observed at a very high frequency due to the ceramic output capacitor.

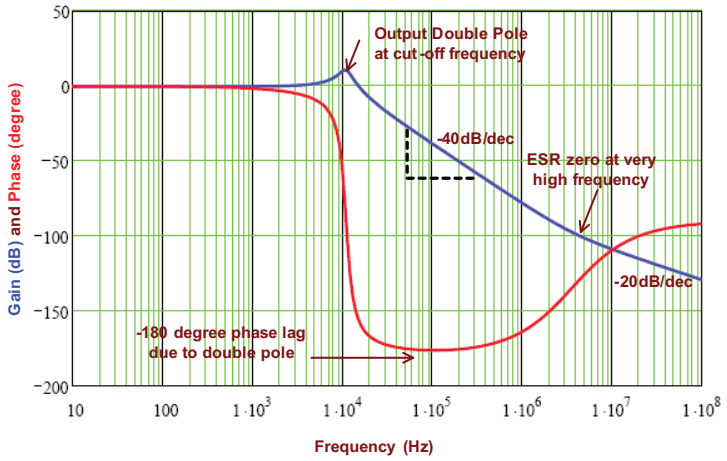

Figure 3: The Bode Plot of the Output Stage.

Error Amplifier Transfer Function Calculation

The error amplifier transfer function with type III compensation as shown in Figure 4 is calculated from Equation 5:

Eq. 5: $$G_E = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{s \cdot C_2} \;//\left(R_1 + \frac{1}{s \cdot C_1}\right)}{R_{fbh} \;//\left(R_{ff} + \frac{1}{s \cdot C_{ff}}\right)}$$

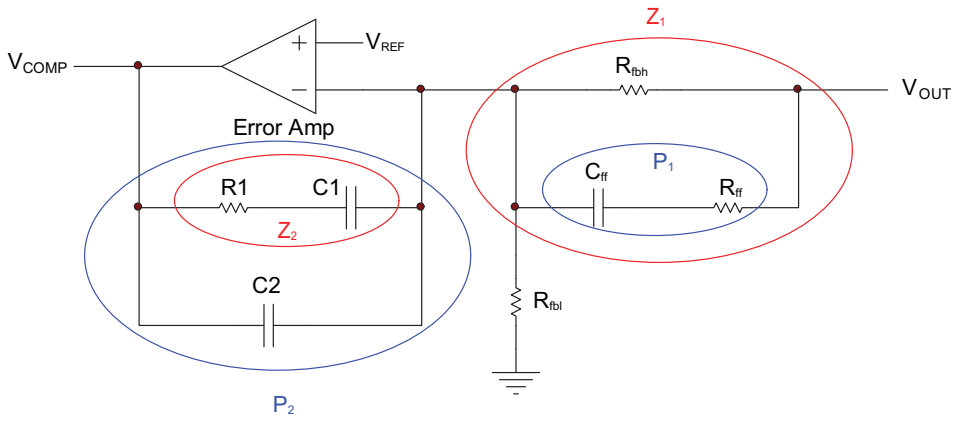

Figure 4: Error Amplifier With Type III Compensation Network.

By algebraic manipulation, G_E can be explicitly expressed in terms of zeros and poles in Equation 6.

Eq. 6: $$G_E = \frac{R_{fbh} + R_{ff}}{R_{fbh} \cdot R_{ff} \cdot C_2} \cdot \frac{\left(s + \frac{1}{R_1 \cdot C_1}\right) \cdot \left(s + \frac{1}{(R_{fbh} + R_{ff}) \cdot C_{ff}}\right)}{s \cdot \left(s + \frac{(C_1 + C_2)}{R_1 \cdot C_1 \cdot C_2}\right) \cdot \left(s + \frac{1}{R_{ff} \cdot C_{ff}}\right)}$$

Equation 6 gives two zeroes at frequencies F_{Z1} and F_{Z2} and two poles at frequencies F_{P1} and F_{P2} in the following expressions:

$$F_{Z1} = \frac{1}{2\pi \cdot (R_{fbh} + R_{ff}) \cdot C_{ff}} \text{ and } F_{Z2} = \frac{1}{2\pi \cdot R_1 \cdot C_1}$$

$$F_{P1} = \frac{1}{2\pi \cdot R_{ff} \cdot C_{ff}} \text{ and } F_{P2} = \frac{1}{2\pi \cdot R_1 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)}$$

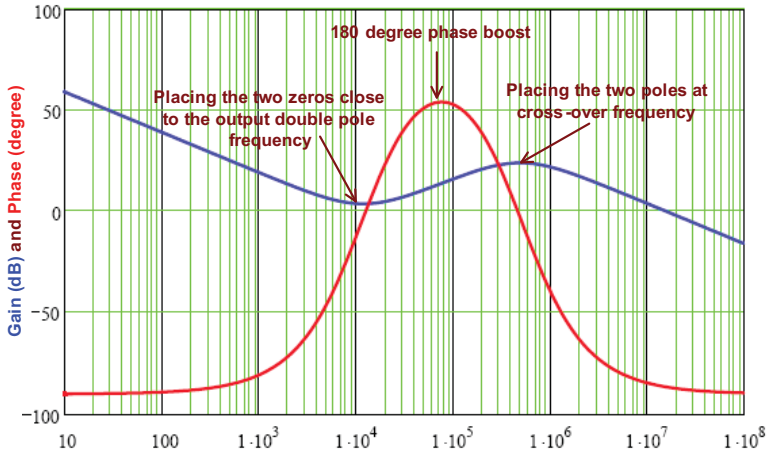

Figure 5: Error Amplifier With Type III Compensation Bode Plot.

Type III compensation provides two zeros and two poles which push the cross-over frequency as high as possible and boosts the phase margin greater than 45 degree. A higher bandwidth yields a faster load transient response. The faster transient response results in a smaller output voltage spike.

PWM Modulator Stage

The PWM modulator gain is inversely proportional to the peak-to-peak input ramp voltage of the oscillator and is derived via Equation 7.

Eq. 7: $$G_M = \frac{V_{IN}}{V_{RAMP}}$$

Step-Down Converter Loop Gain with Type III Compensation

The loop gain of the system is expressed in terms of G_M, G_E, and G_P factors as shown in Equation 8.

Eq. 8: $G_{LOOP} = G_M \cdot G_E \cdot G_P$

The magnitude in dB and the phase in degree of the converter loop gain are derived from Equations 9 and 10.

Eq. 9: $G_{LOOP}\,(dB) = 20.\log\,(G_{LOOP}) = 20.\log\,(G_M \cdot G_E \cdot G_P)$

Eq. 10: $P_{LOOP} = \arg(G_{LOOP}) \cdot \frac{180}{\pi}$

The magnitude and phase Bode plots of the converter loop gain with type III compensation are shown in Figure 5. By placing the two zeros close to the output double pole and the two poles at switching frequency, the crossover frequency is pushed to 10% to 60% of switching frequency and in the vicinity of maximum phase boost in order to achieve an optimum phase margin Φ_M.

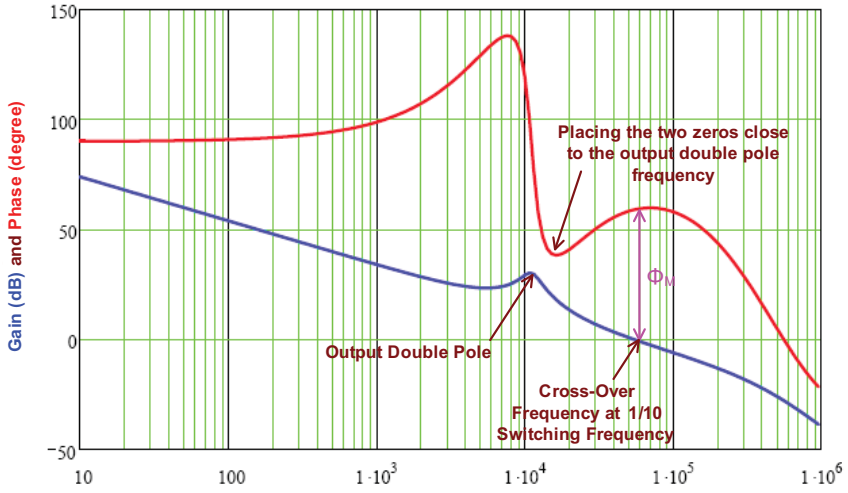

Figure 6: Step-Down Converter Loop Gain With Type III Compensation Bode Plot .

Design Type III Compensation Network For Voltage Mode Step-down Converters

Type III Compensation Design Process For Voltage Mode Control Step-Down Converter:

For example, assume the voltage mode step-down converter has the following specifications:

V_{IN} = 6V to 24V
V_{OUT} = 3.3V

$$R_{FBL} = 6.04K\Omega,\ R_{FBH} = R_{FBL} \cdot \frac{V_{OUT} - V_{REF}}{V_{REF}} = 6.04K \cdot \frac{3.3V - 0.6V}{0.6V} = 27.4K\Omega$$

$$V_{RAMP} = \frac{V_{IN}}{12}$$

L = 4.7µH
C_{OUT} = 2x22µF, ESR = 2mΩ
I_{OUT} = 2.5A
F_{SW} = 490KHz

1. Set the crossover frequency in the range of 1/6 to 1/10 of switching frequency to avoid the Niquist pole:

Eq. 11: $$F_C = \frac{F_{SW}}{10} = 49KHz$$

2. Place the first zero from 60% to 150% of the double pole frequency of the L C_{OUT} filter:

Eq. 12: $$C_{ff} = \frac{\sqrt{L \cdot C_{OUT}}}{K \cdot R_{fbh}} = \frac{\sqrt{4.7\mu H \cdot 44\mu F}}{1.1 \cdot 27.4K\Omega} = 481pF$$

Where the value of factor K is within the range of 0.6 to 1.5.

3. Set the first pole at switching frequency and calculate R_{ff} from:

Eq. 13: $$R_{ff} = \frac{1}{2\pi \cdot C_{ff} \cdot F_{SW}} = \frac{1}{2\pi \cdot 481pF \cdot 490KHz} = 675\Omega$$

4. At cross-over frequency (F_C) the loop gain is unity. Setting $|G_{LOOP}| = 1$ at $s = j\omega_c$, the value of R1 is given by Equation 14.

Eq. 14: $$R_1 = \frac{(2\pi \cdot F_C)^2 \cdot L \cdot C_{OUT} + 1}{2\pi \cdot F_C \cdot C_{ff}} \cdot \frac{V_{RAMP}}{V_{IN}} = \frac{(2\pi \cdot 49KHz)^2 \cdot 4.7\mu H \cdot 44\mu F}{2\pi \cdot 49KHz \cdot 481pF} = 11.6K\Omega$$

5. Set the second zero to coincide with the first zero, and solve for C1:

Eq. 15: $$C_1 = \frac{\sqrt{L \cdot C_{OUT}}}{K \cdot R_1} = \frac{\sqrt{4.7\mu H \cdot 44\mu F}}{1.1 \cdot 11.6K\Omega} = 112pF$$

6. Place the second pole from switching frequency to one decay higher for adequate phase margin, and solve for C2:

Eq. 16: $$C_2 = \frac{1}{2\pi \cdot R_1 \cdot F_{SW}} = \frac{1}{2\pi \cdot 11.6K\Omega \cdot 490KHz} = 28pF$$

Design Type III Compensation Network For Voltage Mode Step-down Converters

The Relationship between Frequency Domain and Time Domain in a Step-Down Converter

Knowing the relationship between the phase margin in the frequency domain and load transient response in time domain is beneficial to achieving the best results. In this way, we can select either a slow output transient response but without any overshoot or, a faster output transient response with a small amount of overshoot. Let's concentrate on the small area in the vicinity of the cross over frequency (see Figure 7). The curve has two different slopes (-20dB/ decade and -40dB/ decade) due to the location of the original pole ω_0 and the high frequency pole ω_2. Assuming the other compensation pole ω_1 and the ESR zero are cancelled out. The open loop transfer function in this region can be approximated by Equation 17:

Eq. 17: $$T(s) \approx \frac{1}{\left(\frac{s}{\omega_0}\right)\left(1+\frac{s}{\omega_2}\right)}$$

The close loop transfer function can derive from T(s):

Eq. 18: $$G_{LOOP}(s) = \frac{1}{1+T(s)} = \frac{1}{\frac{s^2}{\omega_0 \cdot \omega_2}+\frac{s}{\omega_0}+1} = \frac{1}{\frac{s^2}{\omega_r^2}+\frac{s}{\omega_r \cdot Q}+1}$$

Where the quality coefficient Q and the resonant frequency ω_r are defined using Equations 19 and 20.

Eq. 19: $$Q = \sqrt{\frac{\omega_0}{\omega_2}}$$

Eq. 20: $$\omega_r = \sqrt{\omega_0 \omega_2}$$

The cross-over frequency ω_c can be solved by equating Equation 18 to unity at the crossover frequency:

Eq. 21: $$\omega_c = \omega_2 \frac{\sqrt{\sqrt{1+4\left(\frac{\omega_0}{\omega_2}\right)^2}-1}}{\sqrt{2}} = \omega_2 \frac{\sqrt{\sqrt{1+4(Q)^2}-1}}{\sqrt{2}}$$

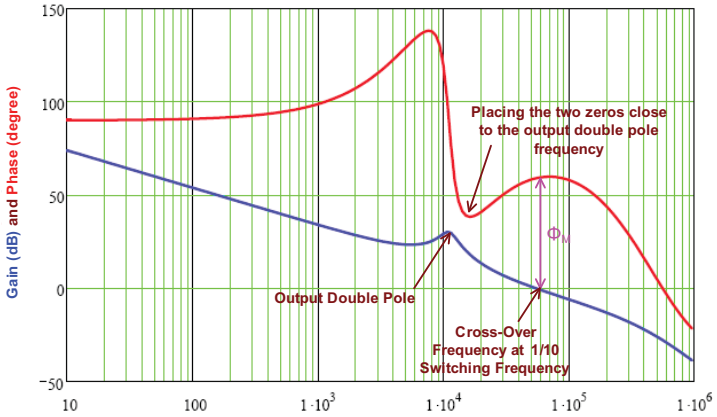

Figure 7: The Gain Curve Has Two Different Slopes (-20dB/decade and -40dB/decade) at Crossover Frequency due to the Location of the Original Pole ω_0 and the High Frequency Pole ω_2.

Eq. 22: $\arg T(\omega_C) = -\left(\tan^{-1}\frac{\frac{\omega_C}{\omega_0}}{0} + \tan^{-1}\frac{\omega_C}{\omega_2}\right) = -\tan^{-1}\frac{\omega_C}{\omega_2} - \frac{\pi}{2}$

Eq. 23: $\varphi_M = \pi + \arg T(\omega_C) = \tan^{-1}\frac{\omega_2}{\omega_C} = \tan^{-1}\left(\sqrt{\frac{2}{\sqrt{1+4Q^4}-1}}\right)$

The relationship between the phase margin and the quality coefficient can be derived from Equation 23:

Eq. 24: $Q = \frac{\sqrt{1+\tan(\varphi_M)^2}}{\tan(\varphi_M)} = \frac{\sqrt{\cos(\varphi_M)}}{\sin(\varphi_M)}$

The percent overshoot and quality factor in the second order system are given by Equation 25.

Eq. 25: $\%OS = 100 \cdot e^{\frac{-\pi}{\sqrt{4Q^2-1}}} = 100 \cdot e^{\frac{-\pi}{\sqrt{\frac{4\cos\varphi_M}{\sin^2\varphi_M}-1}}}$

Figure 8 plots the percent overshoot versus phase margin of a typical second order system.

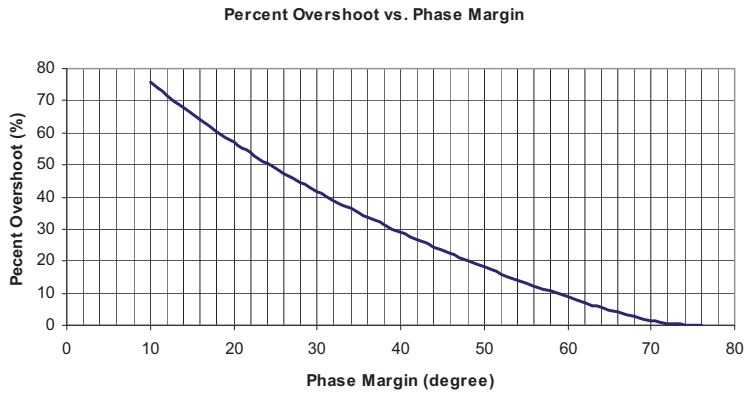

Figure 8: Percent Overshoot vs. Phase Margin for Second Order System.

The output transient response of a 3.3V output step-down converter with different phase margin is measured in Figure 9. The step load is generated from 200mA to 2.5A with 2A/µs slew rate. The red curve corresponding to 68° phase margin has 160µs recovery time without overshoot and a transient voltage spike of 404mV. The black and green curves experience very fast recovery time (40µs) with very small overshoot and a small transient voltage spike of 280mV. Finally, the blue and pink curves reveal an unstable system due to the phase margin of less than 45°.

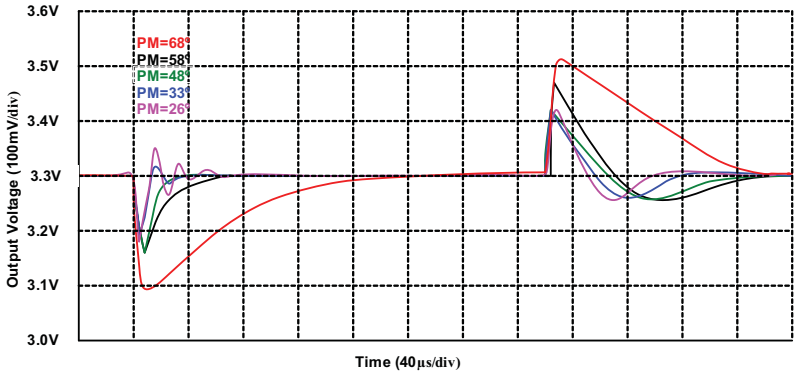

Figure 9: The Relationship Between Phase Margin, Overshoot and Recovery Time of the Output Transient Response of a 3.3V Output Buck Converter.

Phase Margin and Transient Response vs. DC Gain (F_C = 50KHz)

Based on the discussion above of the frequency domain and time domain, the recovery time can be adjusted faster to reduce the peak-to-peak output transient response of a step-down converter. This can be done by pushing the zeros a bit above the double poles frequency (K = 1.1) in order to boost the DC gain from 65dB to 75dB. Figure 10 illustrates the relationship between the phase margin and load transient response for K = 0.6 and K = 1.1 at the same crossover frequency of 50KHz. A higher DC gain along with a smaller phase margin of 58° yields a faster recovery time of 60µs, which results in a smaller peak-to-peak output transient response (280mV) for a 200mA to 2.5A dynamic load.

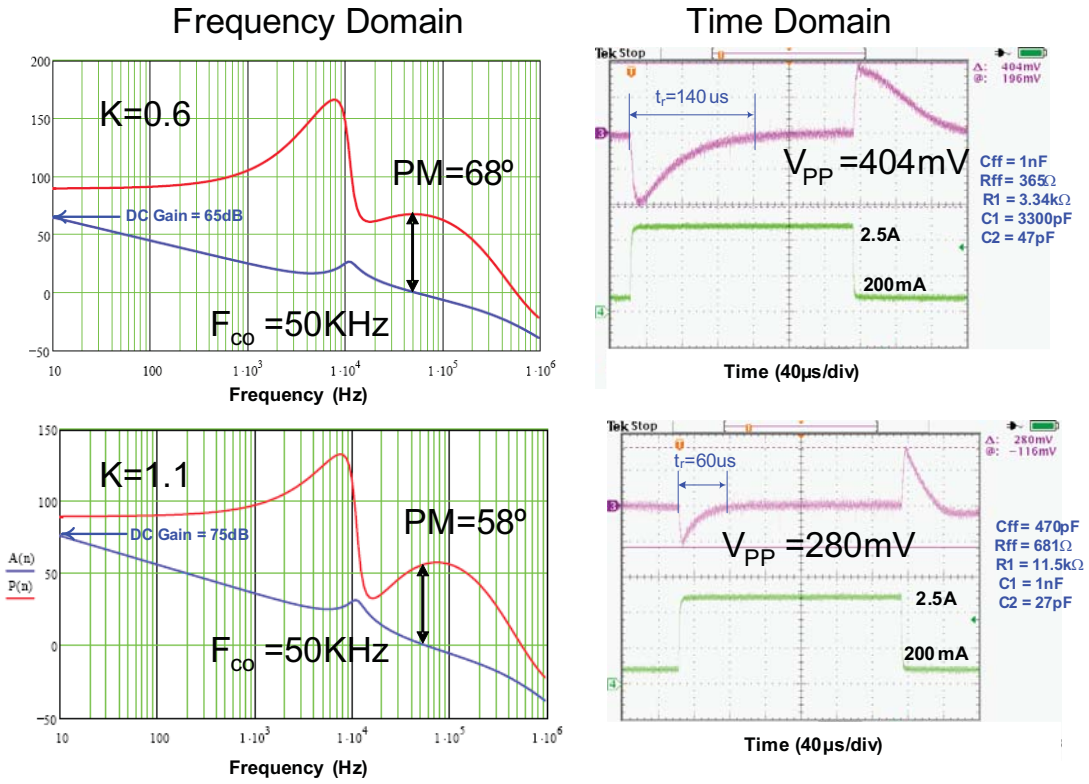

Figure 10: Phase Margin and Transient Response For Differing K Factors (K = 0.6 and K = 1.1).

Phase Margin and Transient Response vs. Bandwidth (K = 1.1)

As illustrated in Figure 11, the output voltage spike can be further improved by pushing the crossover frequency (F_C) to 80KHz if a small amount of overshoot is acceptable. However, further increasing the bandwidth reduces the phase margin below 45°, resulting in an unstable system. In addition, increasing the bandwidth to exceed the effective control bandwidth no longer reduces the output voltage spike due to the voltage drop across the ESR of the output capacitor which dominates the transient voltage spike.

For a 3.3V output voltage buck converter using a 4.7µH inductor during a load transient step from 200mA to 2.5A, the effective control bandwidth is derived from Equation 26.

Eq. 26: $$F_{CE} = \frac{V_O}{4 \cdot \Delta I_O \cdot L} = \frac{3.3V}{4 \cdot 2.5A \cdot 4.7\mu H} = 76KHz$$

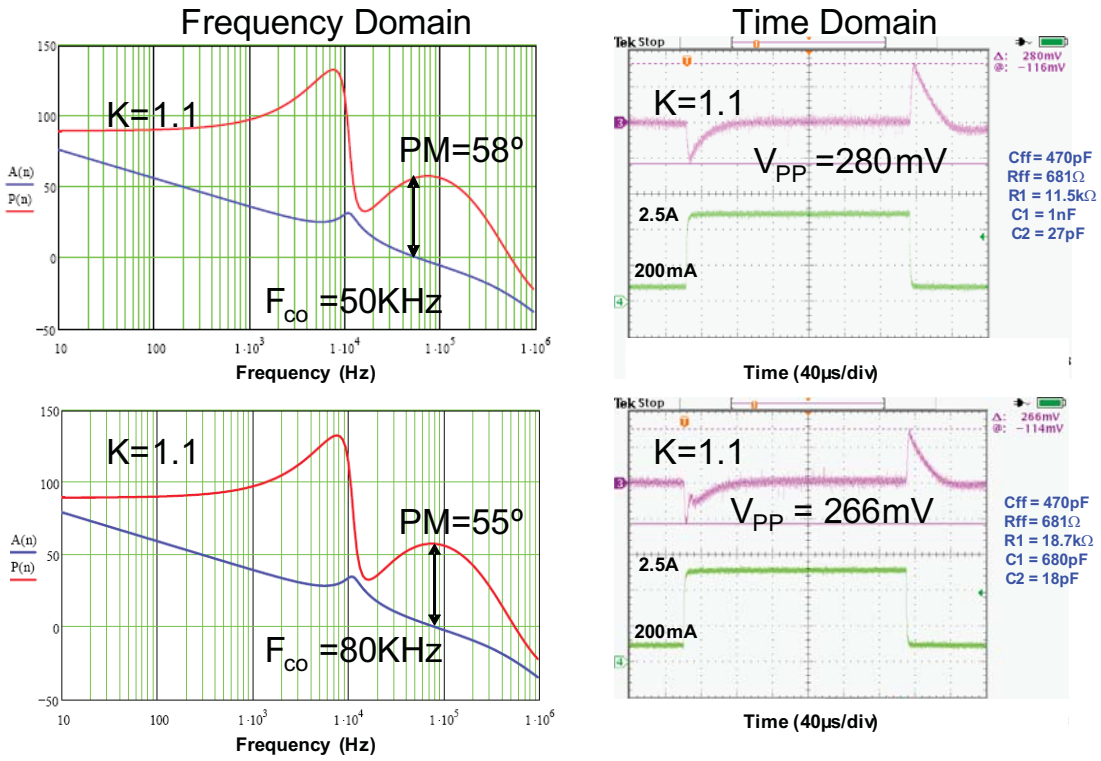

Figure 11: Frequency Domain vs. Time Domain For Different Bandwidth (F_{co} = 50KHz and F_{co} = 80KHz)

Loop Gain Measurement

The following guidelines show the method used to measure the loop gain of a DC-DC converter:

1. Break the feedback loop and insert a 50Ω resistor between the broken original connection. Insert the secondary winding terminal of the one-to-one isolation transformer between the 50Ω resistor. Configure the specified test equipment as shown in Figure 11.
2. Inject a sinusoidal signal from SOURCE OUT of the network analyzer to the loop through the primary winding terminal of the transformer while monitoring the ratio of CHA and CHB on the network analyzer.
3. Set the converter output current to heavy load while monitoring the LX node of the converter on the oscilloscope (to obtain a good result the converter must be in continuous PWM mode).
4. Sweep the frequency from SOURCE OUT of the network analyzer from 10Hz to 1MHz and adjust the magnitude of the injected signal (around 10mV to 100mV) in order to have a clean PWM waveform at the LX node.

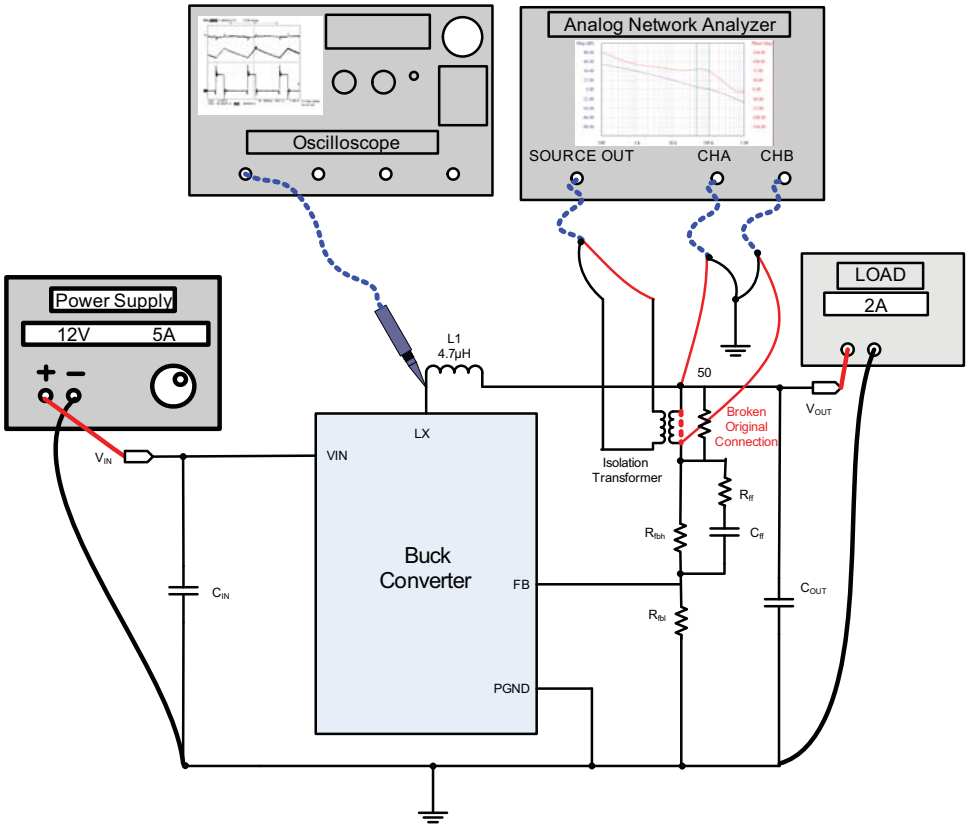

Figure 12: Loop Gain Measurement Set-up.

Conclusion

Using low ESR ceramic output capacitors for voltage mode controlled buck converters yields very low output voltage ripple, but requires type III compensation for adequate phase margin. The type III compensation network provides two zeros and two poles that push the crossover frequency to a possible maximum value with adequate phase margin for the control loop. The trade-off between the stability and output transient response can be adjusted by using the factor K, which represents the position of zeros in the vicinity frequency of the output double poles. In applications which require no overshoot, the two zeros are placed at 60% (K = 0.6) of the output double poles frequency to achieve approximately 70 degrees of phase margin. However, if the transient output voltage spike is critical, the two zeros can be placed up to 150% (K = 1.5) of the output double pole frequency if a small amount of overshoot is acceptable. In addition, a higher bandwidth yields a faster transient response. However, a bandwidth higher than the critical bandwidth can no longer reduce the transient output voltage spike. A typical bandwidth for type III compensation is in the range of 10% to 60% of switching frequency.

Advanced Analogic Technologies, Inc.
3230 Scott Boulevard, Santa Clara, CA 95054
Phone (408) 737-4600
Fax (408) 737-4611