What Is Flash Memory?

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Contents

Revision History

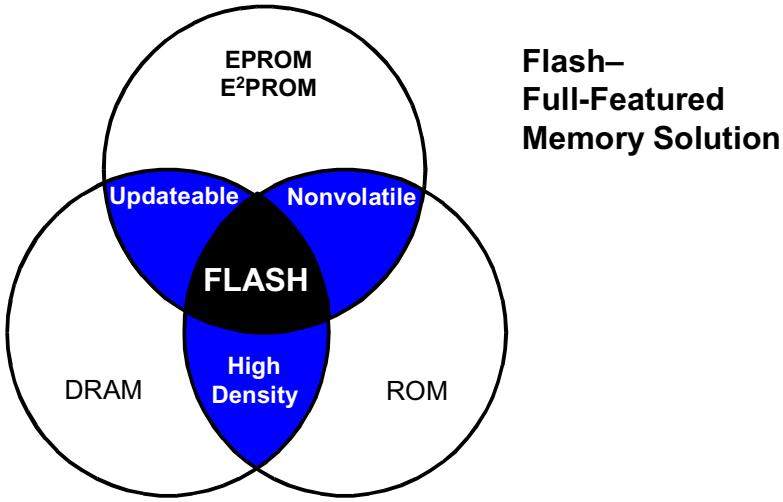
Date of Revision	Version	Description
01/12/01	-001	Original version
06/05/01	-002	Updated Figure 4 to reflect 128 Kbytes; not 64 Kbytes, for Intel Strataflash® Memory.
10/10/02	-003	Updated “Why Intel Flash Memory” section.

1.0 What is Flash Memory?

Computerized systems, from simple appliances to complex networks, contain many different parts–processors, displays, software, drives, keyboards and mice, printed circuit boards, switches, modems, and of course, memory–to name a few.

But what exactly is memory, and more specifically, what is flash memory? Memory is capable of retaining digital information under certain conditions. This retained material might be operational code or data files, or a combination of the two. The ideal memory subsystem optimizes density, preserves critical material in a nonvolatile condition, is easy to program and reprogram, can be read fast, and is cost-effective for the application. Some memory technologies meet one or more of these requirements very well, but offsetting limitations can prevent the product from becoming a genuine solution, especially in newer applications.

Figure 1. Memory Types

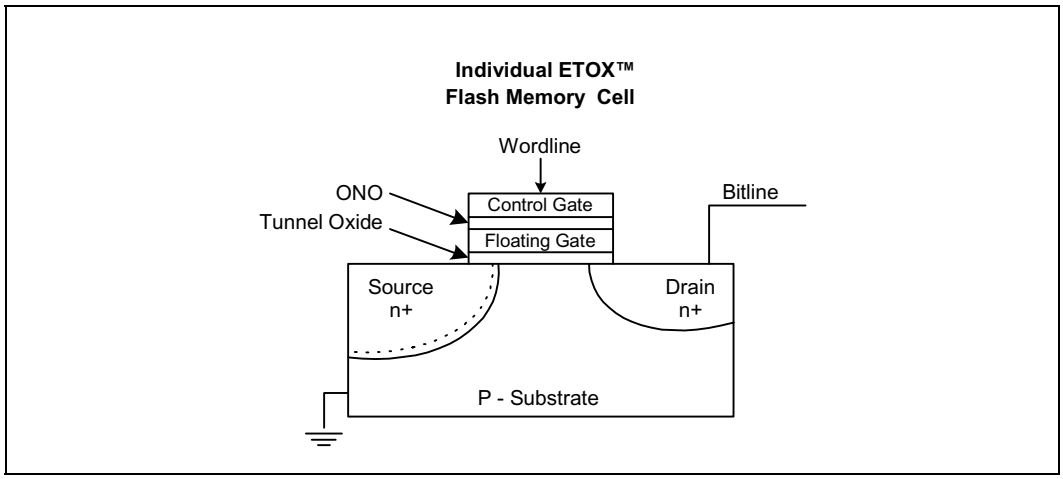


Memory Type	Features
FLASH	Low-cost, high-density, high-speed architecture; low-power, high reliability
ROM Read-Only Memory	Mature, high-density, reliable, low cost; time-consuming mask required, suitable for high production with stable code
SRAM Static Random-Access Read-Only Memory	Highest speed, high-power, low-density memory; limited density drives up cost
EPROM Electrically Programmable Read-Only Memory	High-density memory; must be exposed to ultraviolet light for erasure
EEPROM or E^2 Electrically Erasable Programmable Read-Only Memory	Electrically byte-erasable; lower reliability, higher cost, lowest density
DRAM Dynamic Random Access Memory	High-density, low-cost, high-speed, high-power

2.0 Technical Overview of Flash Memory

Flash memory is a nonvolatile memory using NOR technology, which allows the user to electrically program and erase information. Intel Flash memory uses memory cells similar to an EPROM, but with a much thinner, precisely grown oxide between the floating gate and the source (see Figure 2). Flash programming occurs when electrons are placed on the floating gate. The charge is stored on the floating gate, with the oxide layer allowing the cell to be electrically erased through the source. Intel Flash memory is an extremely reliable nonvolatile memory architecture.

Figure 2. Flash Memory Cell

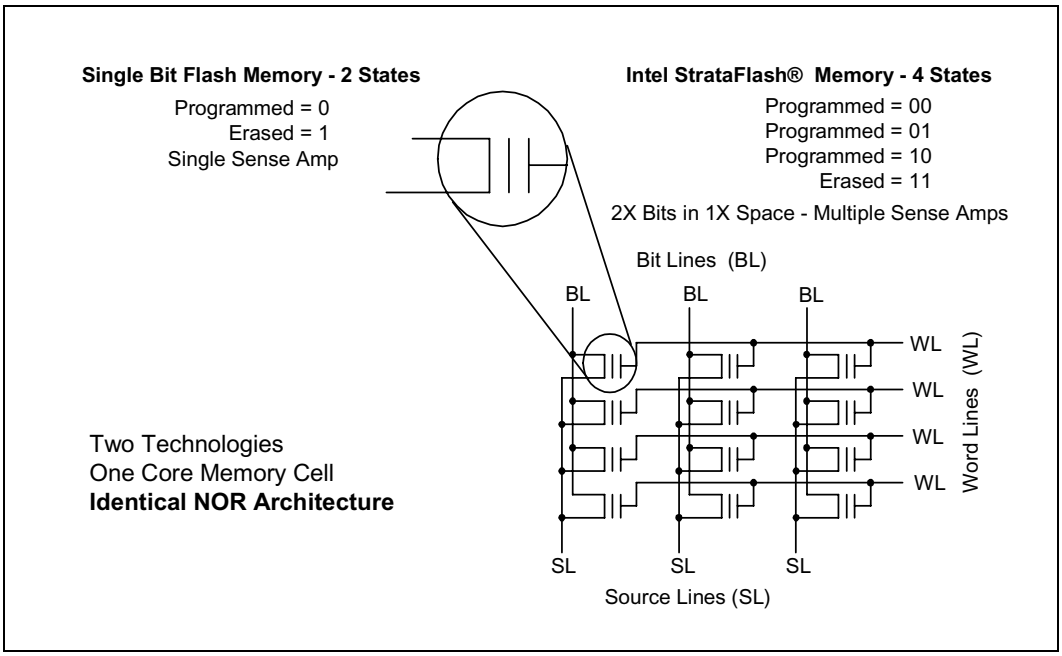


2.1 Two Technologies–One Core Memory

Intel has two highly reliable flash technologies based on the same core memory cell (see Figure 3). The first technology is the original single bit/cell flash memory that allows a single bit of information to be stored in each cell (1 = erased and 0 = programmed).

The second and most recent technology is called multi-level cell structure, used in Intel StrataFlash® memory. This technology allows two bits of information to be stored in a single transistor. Precision is the key to storing two bits per cell. Programming a cell (charge placement) and reading (sensing) must be precisely controlled in order to have four states within a single transistor. Multi-level cell flash memory is a reliable NOR-based architecture ideally suited for high-density applications.

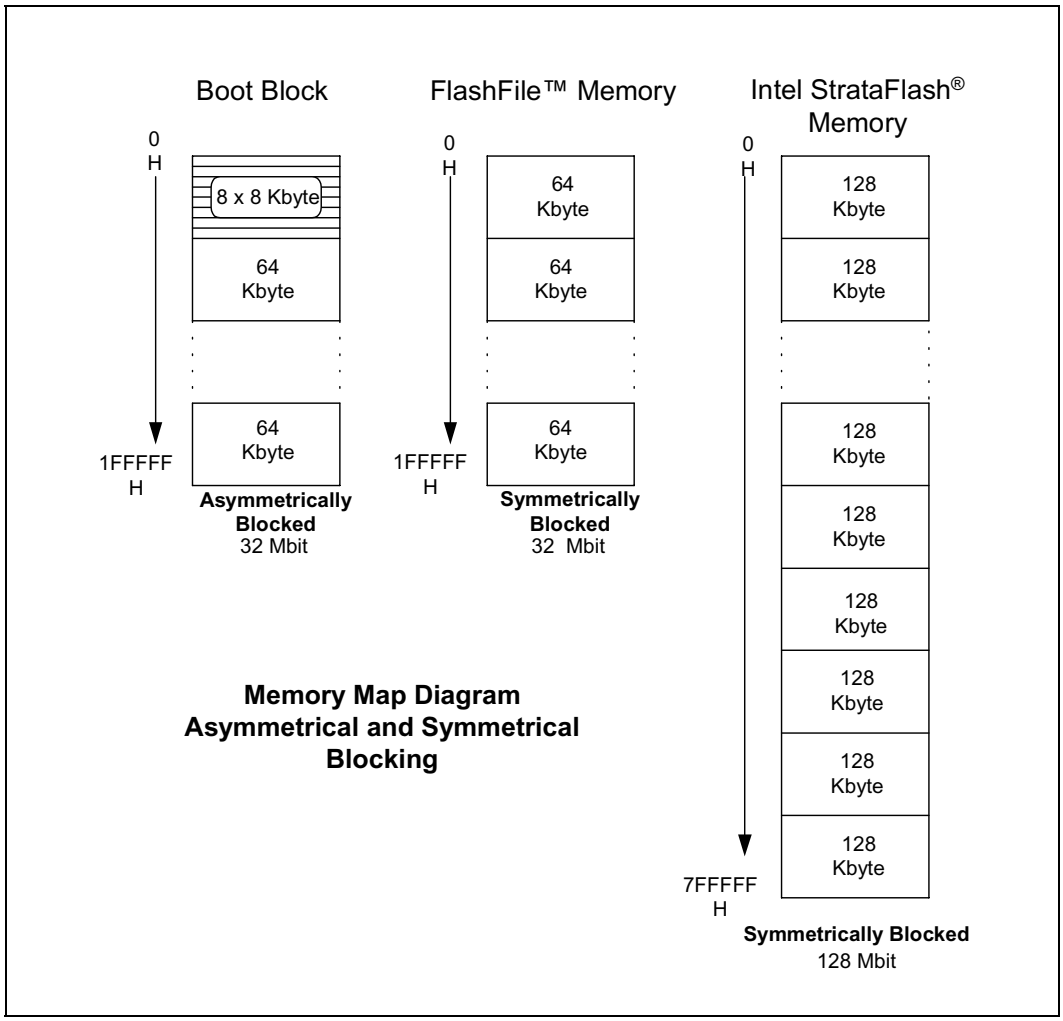
Figure 3. Single Bit vs. Intel StrataFlash® Memory



2.2 Memory Array Architecture

Intel Flash memory products are available in symmetrical and asymmetrical blocking architecture (see Figure 4 on page 8). The flexible blocking architecture enables system integration of code and data within a single flash device. The Boot Block flash memory family has *asymmetrically*-blocked memory array layouts to enable small parameter or boot code storage (like EEPROM), coupled with efficient larger blocks for code and data file storage. The FlashFile™ and Intel StrataFlash® memory families are *symmetrically*-blocked memory arrays, which enable the best code and data file management.

Figure 4. Memory Map Diagram

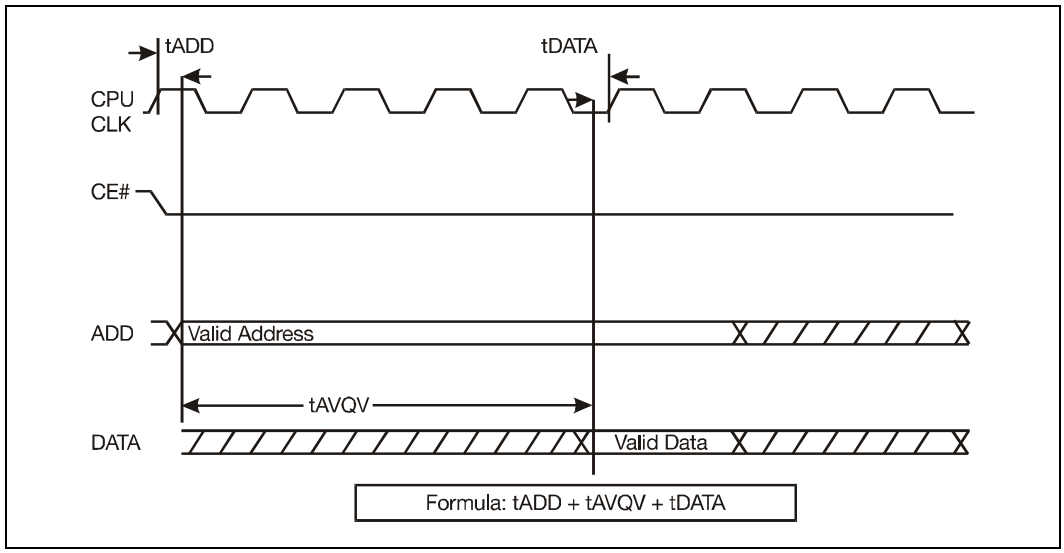


2.3 Operational Read Modes

The standard modes of operation for flash components are r*ead, program,* and *erase*. To enable the use of flash in different, higher-performance ways, Intel has enhanced these basic modes of operation by adding several other integrated features. Please note that not all modes or features are available on every product. Visit http://developer.intel.com/design/flash/datashts/index.htm for more complete product information.

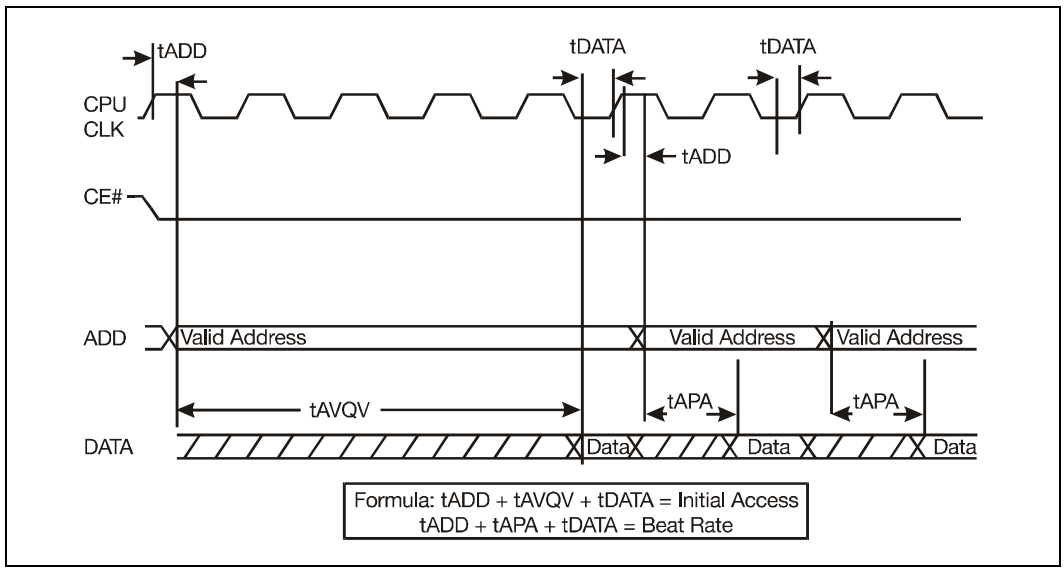
Intel provides three types of read operations: asynchronous word mode, asynchronous page mode and synchronous burst mode. The most common is an *asynchronous* word mode (see Figure 5 on page 9), where the access time for the data starts on an address transition, an OE# (output enable) falling edge, or a CE# (chip enable) falling edge. This type of access provides acceptable performance for most applications, and only requires a simple non-clocked system design. Our remaining two read modes are higher performance, and they require a CPU or ASIC to enable the modes on these devices.

Figure 5. Asynchronous Word Mode Read



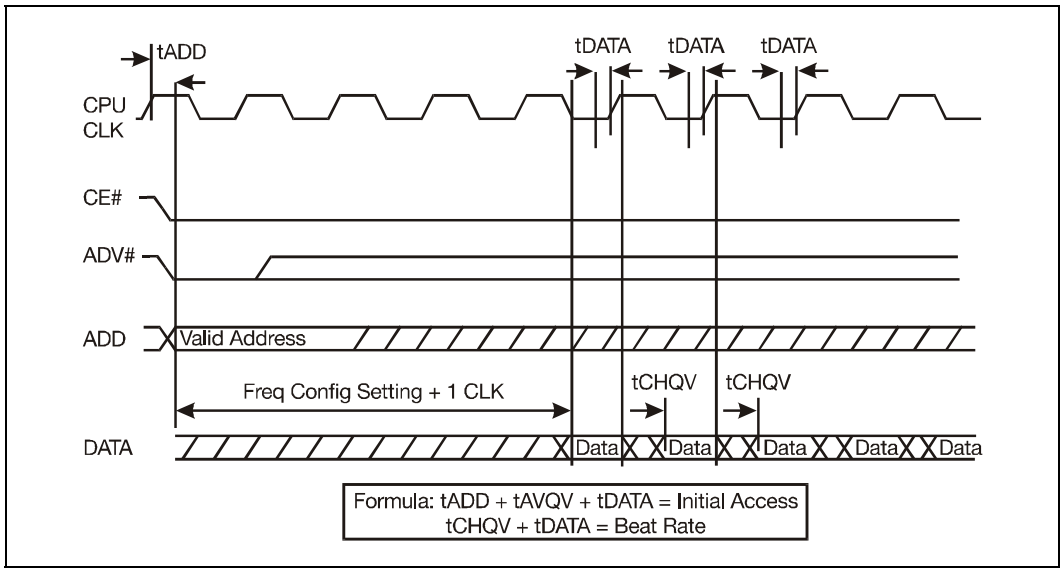
Our *asynchronous* page mode (see Figure 6) provides a high data transfer rate for non-clocked memory systems. In this mode, data is internally read and stored in a high-speed page buffer. This mode requires an initial access time similar to the asynchronous mode, but then the remaining data in the page can be accessed as fast as 20 ns each time the address lines are toggled within the page.

Figure 6. Asynchronous Page Mode Read



Lastly, our highest performance read mode is a synchronous burst interface (see Figure 7 on page 10). This mode supports up to a 66 MHz operation with no wait-state. This interface is achieved through three additional control pins: CLK# (clock input), WAIT# (CPU wait output), and ADV# (address valid input). In synchronous burst mode, the device latches the initial address, then outputs a sequence of data with respect to the input clock and read configuration setting. A programmable read configuration register (RCR) is supplied to provide for glueless hardware connections.

Figure 7. Synchronous Burst Read



2.4 Programming and Erasing

Programming on Intel Flash is most commonly done in a byte or word wide mode; however, several devices provide 32-byte write buffers. These buffers allow data to be queued in advance for up to 2 µs effective byte programming speeds. Erasure of the flash device is done through a Block Erase command, and the completion time is dependent upon the block size and technology. Functions, such as program-suspend, program-resume, erase-suspend and erase-resume, allow the device to pause and read data, then resume the previous operation. Intel's multi-partition architecture allows the system processor to read from one partition while completing a write/erase in the other partition. For example, this permits executing code *and* programming data from the same flash device at the same time.

2.5 Software Enabled Features

Intel Flash memory provides several software-enabled features that optimize code, increase system performance, and help to protect the integrity of the information stored on the device.

The Common Flash Interface (CFI) and status registers are features used for code optimization. The CFI query register contains non-alterable data about the component, such as block sizes, density, x8/x16, and electrical specifications. Think of this feature as a *databook-on-a-chip* that allows the software to adapt to several different devices by passing variables from the CFI register. Additionally, the status register is used to query the operating status of the device during programming, erase, and suspend modes. In some devices, the status register can also tell you if one of the blocks is locked.

The status register also helps the overall system performance of the device by performing a continuous query check on several bits to look for a successful programming or erase event to complete. This helps system performance by only using the required time to complete the operation vs. having the software implement a long timeout based on the maximum specification.

For synchronously read devices, the read configuration register (RCR) is the most important software-controlled register in the memory subsystem. Setting the RCR allows the user to get into burst mode, add CPU wait states, configure burst sequence/length, and even set hardware configuration for CLK# and WAIT# signal.

2.6 Data Protection

Protection of the nonvolatile data in a flash device has always been an important consideration. Several Intel Flash products feature dynamic hardware block-locking, so that critical code can be kept secure while non-locked blocks are programmed and erased. This locking scheme offers two levels of protection. The first allows software-only control of block locking (useful for frequently-changed data blocks), while the second requires hardware interaction before locking can be changed, protecting infrequently-changed code blocks. This locking capability is different by product family.

2.7 Security

Security is at the forefront of many applications, and several Intel Flash products are now equipped with two 64-bit OTP protection registers. These one-time programmable registers can be used to increase system security. Intel factories program a unique, unchangeable 64-bit number into the OTP, and the other 64-bit register can be programmed by the customer as desired. Once programmed, the customer segment can be locked to prevent further reprogramming. The OTP information can be used for manufacturing tractability and/or a small-encrypted security key for system authentication.

3.0 Why Intel Flash Memory?

When it comes to flash memory, Intel stands for experience, leadership, and technology. As the world's number one supplier of flash memory, Intel's combination of supply availability, leading edge product technologies, flexible packaging, value-added software, and superior customer support result in memory subsystem solutions unrivaled in the industry. It's clear that choosing a memory subsystem supplier has never been easier. That's because Intel is well-positioned to meet your memory needs for today and tomorrow.