深圳市宝安区华威显示厂
HUA WEI DISPLAY SYSTEM ELECTRONICS CO., LTD

Tel: +86-0755-29951125
Fax:+86-0755-27884399

# SPECIFICATIONS

# FOR

# LCD MODULE

Customer: _____

Model name: HW240320F-2D-0B-L1-T4

Description: LIQUID CRYSTAL DISPLAY MODULE

Date: 2008-12-03

CUSTOMER APPROVAL

| | |
|---|---|
| Customer Approval | ☐ Accept<br>☐ Reject<br>comment:<br><br>Approved by: _____ |

SUPPLIER APPROVAL

| APPROVED | CHECKED | ORGANIZED |
|---|---|---|
| 何俊光 | | 刘兰芬 |

1、OTHERS：

APPROVAL FOR SPECIFICATIONS ONLY

APPROVAL FOR SPECIFICATIONS AND SAMPLE

NOTE: VERSION OF SPECIFICATIONS: 00

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## 2、 OTHERS:

History of revision

| Revision | Contents | Date | Note |
|---|---|---|---|
| 00 | New Revision | 2008-12-03 | 1.0 |
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# 1. Introduction And General Specifications

Liquid crystal Displays (LCDS) have widely used in many applications such as industrial measurements, office mechanisms, and household electronic–equipment etc. LCM (LCD Module) integrates with LCD and driving circuit that is easily to be interfaced by user. This LCM contains a standard built-in dot –matrix font set.

## 1.1Applications of LCM

Telephone
Facsimile mechanism
Electronic Typewriter
Word processor
Electronic memo pads
Remote controller

## 1.2 Features of LCM

Compact, thin and light
Wide view angle
Low power consumption
High contrast image
Wide operating temperature
High reliability

## 1.2 General specification

| Parameter | Value | Unit |
|---|---|---|
| LCD Mode | TFT/Transmissive | - |
| Color Depth | 262K/65K | - |
| Display Resolution | 240*RGB*320 | pixels |
| Pixel Arrangement | RGB-stripe | - |
| Viewing Direction | 12 o’ clock | |
| Display Mode | Normally white | |
| LCD Controller/Driver | ILI9325 | - |
| IC Package Type | COG | - |
| MPU Interface | Standard 8080 system 8 bit/16bit parallel | - |
| Power Supply Voltage | 2.5~3.6 | V |
| Back-light | White LED*4 | pcs |

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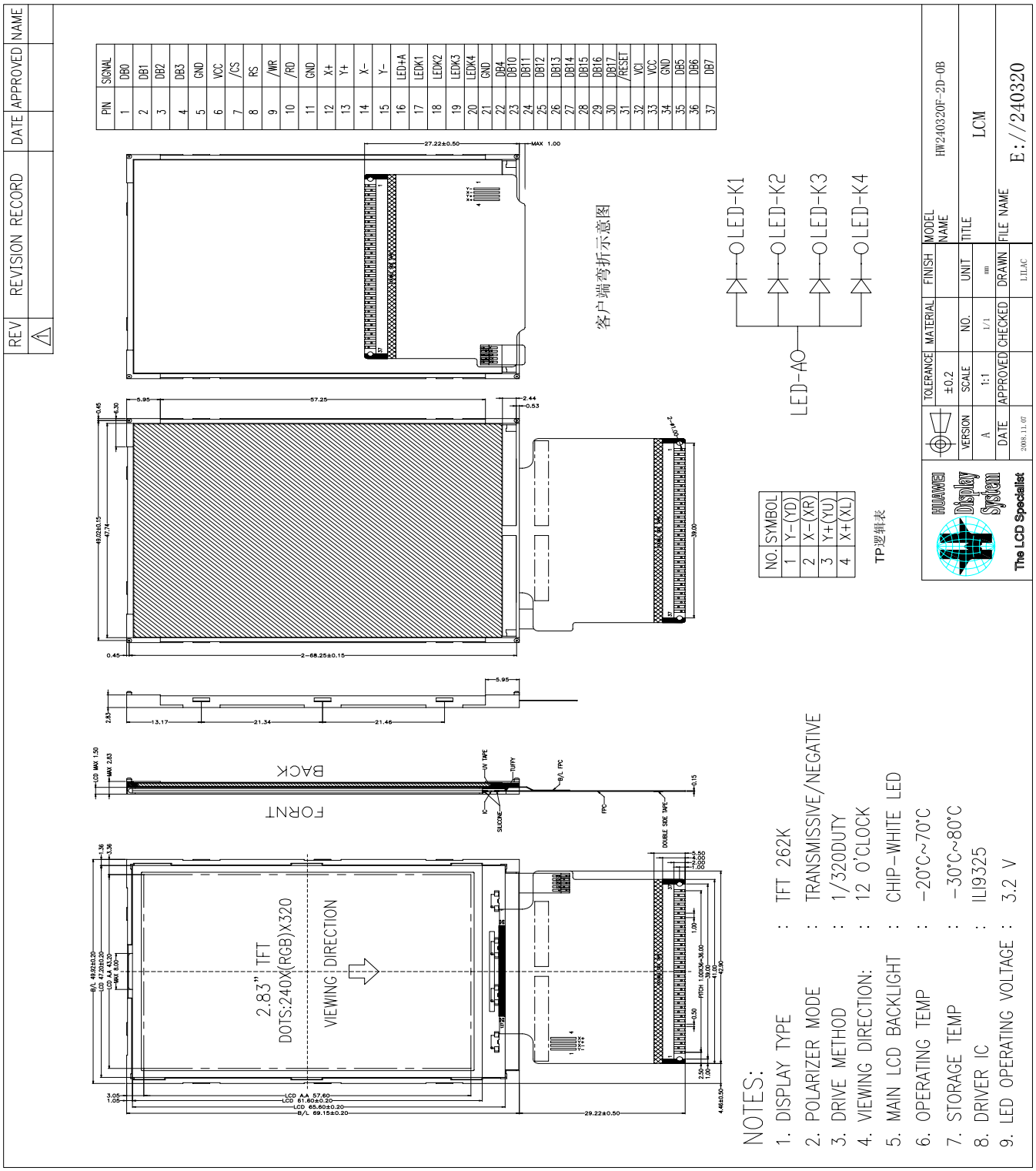
## 2. LCD&LCM Outline Drawing



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## 3. Interface pin Connections Circuit Block Diagram

| PIN NO. | SYMBOL | DESCRIPTION |
|---|---|---|
| 1-4 | DB0-DB3 | Data Bas Line |
| 5 | GND | Internal logic GND: GND=0V. |
| 6 | VCC | Internal logic power: VCC=2.5V~3.3V, VCC>IOVCC. |
| 7 | /CS | Color LCD chip select(active low) |
| 8 | RS | Register select input pin RS = "H": DB0 to DB7 are display data RS = "L": DB0 to DB7 are control data |
| 9 | /WR | Read/Write execution control R/W=" H ": read R/W=" L": write |
| 10 | /RD | Read/Write execution control When /RD is " L ", D0 to D7 are in an output status. |
| 11 | GND | Internal logic GND: GND=0V. |
| 12 | X+ | TP X+ |
| 13 | Y+ | TP Y+ |
| 14 | X- | TP X- |
| 15 | Y- | TP Y- |
| 16 | LEDA | LED 3V |
| 17 | KEDK1 | LED1 GND |
| 18 | LEDK2 | LED2 GND |
| 19 | LEDK3 | LED3 GND |
| 20 | LEDK4 | LED4 GND |
| 21 | GND | Internal logic GND: GND=0V. |
| 22 | DB4 | Data Bas Line |
| 23-30 | DB10-DB17 | Data Bas Line |
| 31 | /RESET | Reset pin. This is an active low signal. |
| 32 | VC1 | Power supply to the crystal power supply anglog circuit. Connect to an external power supply of 2.5V~3.3V. |
| 33 | VCC | Internal logic power: VCC=2.5V~3.3V, VCC>IOVCC. |
| 34 | GND | Internal logic GND: GND=0V. |
| 35-37 | DB5-DB7 | Data Bas Line |

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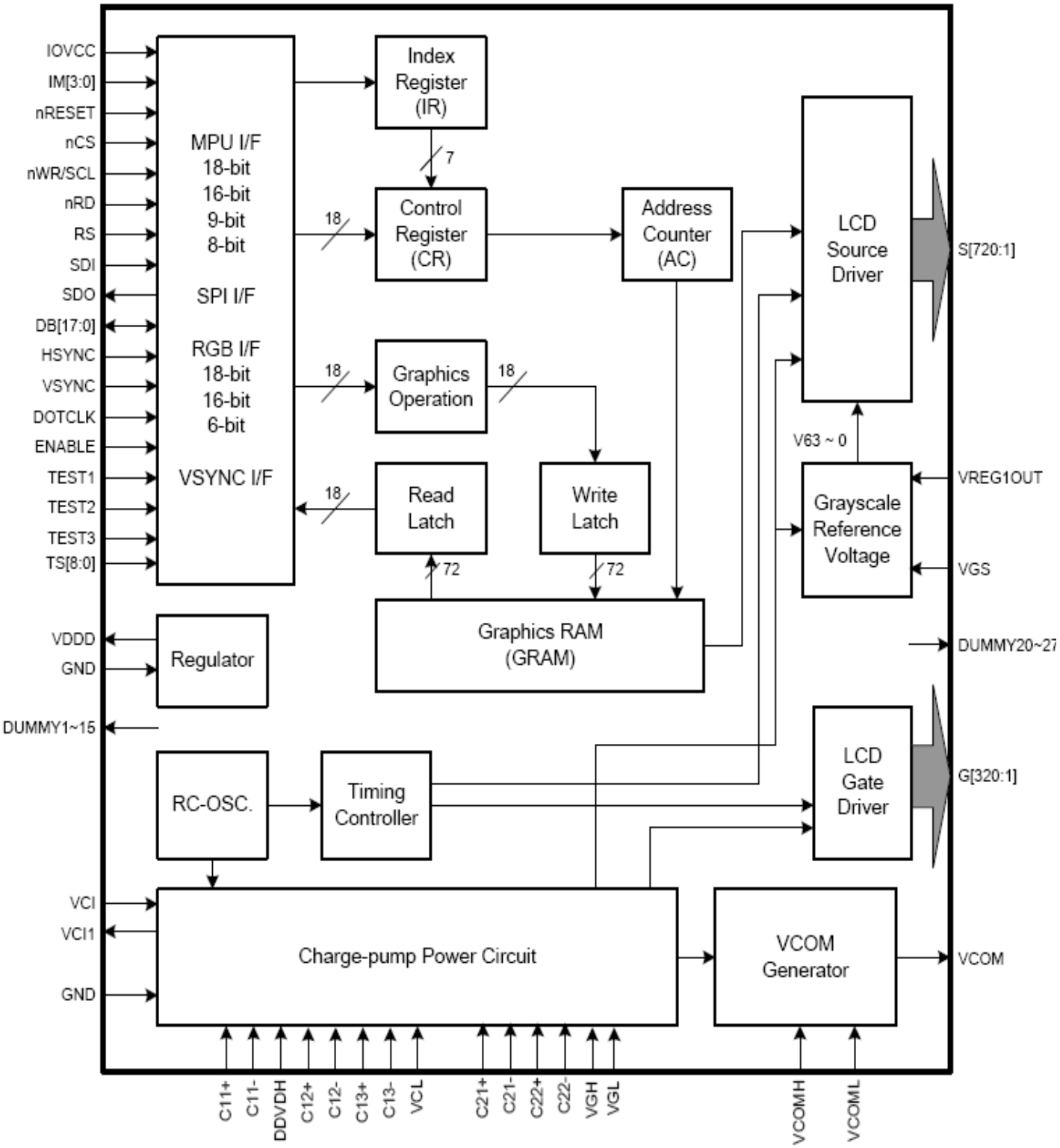
## 4. Block diagram



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# 5. Block description

## MPU System Interface

ILI9325 supports three system high-speed interfaces: i80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and serial peripheral interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

ILI9325 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9325 read the first data from the internal GRAM. Valid data are read out after the ILI9325 performs the second read operation.

Registers are written consecutively as the register execution time except starting oscillator takes 0 clock cycle.

| Registers selection by system interface (8-/9-/16-/18-bit bus width) | I80 | | |
|---|---|---|---|
| Function | RS | nWR | nRD |
| Write an index to IR register | 0 | 0 | 1 |
| Read an internal status | 0 | 1 | 0 |
| Write to control registers or the internal GRAM by WDR register. | 1 | 0 | 1 |
| Read from the internal GRAM by RDR register. | 1 | 1 | 0 |

| Registers selection by the SPI system interface | | |
|---|---|---|
| Function | R/W | RS |
| Write an index to IR register | 0 | 0 |
| Read an internal status | 1 | 0 |
| Write to control registers or the internal GRAM by WDR register. | 0 | 1 |
| Read from the internal GRAM by RDR register. | 1 | 1 |

## Parallel RGB Interface

ILI9325 supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB17-0) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the “External Display Interface” section. The ILI9325 allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

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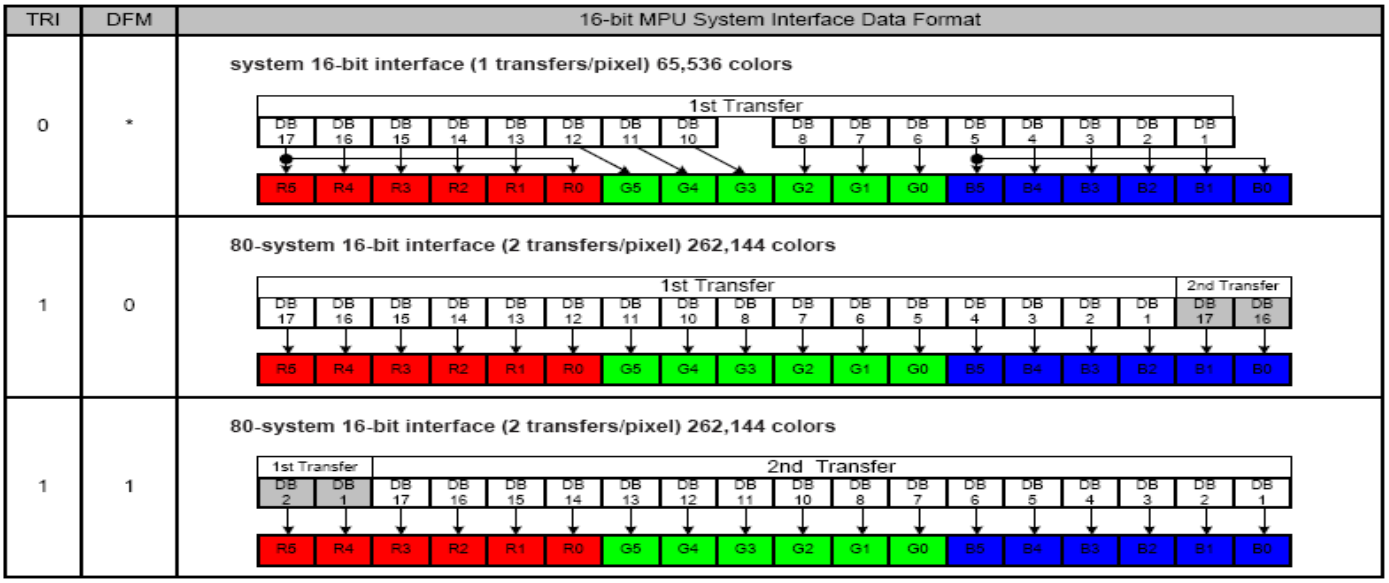
# 6. System interface

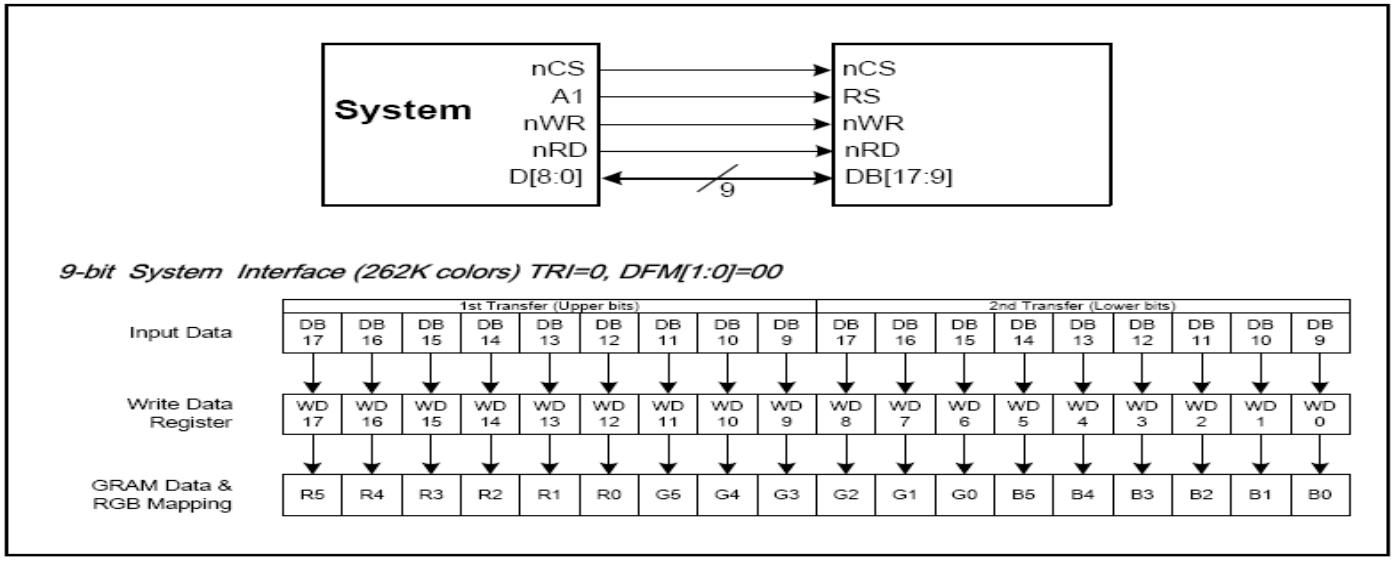
## 6.1 i80/16-bit system interface

The i80/16-bit system interface is selected by setting the IM[3:0] as "0010" levels. The 262K or 65K color can be display through the 16-bit MPU interface. When the 262K color is displayed, two transfers (1st transfer: 2 bits, 2nd transfer: 16 bits or 1st transfer: 16 bits, 2nd transfer: 2 bits) are necessary for the 16-bit CPU interface.




## 6.2 i80/9-bit system interface

The i80/9-bit system interface is selected by setting the IM[3:0] as "1011" and the DB17~DB9 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB[8:0] pins must be tied to GND.



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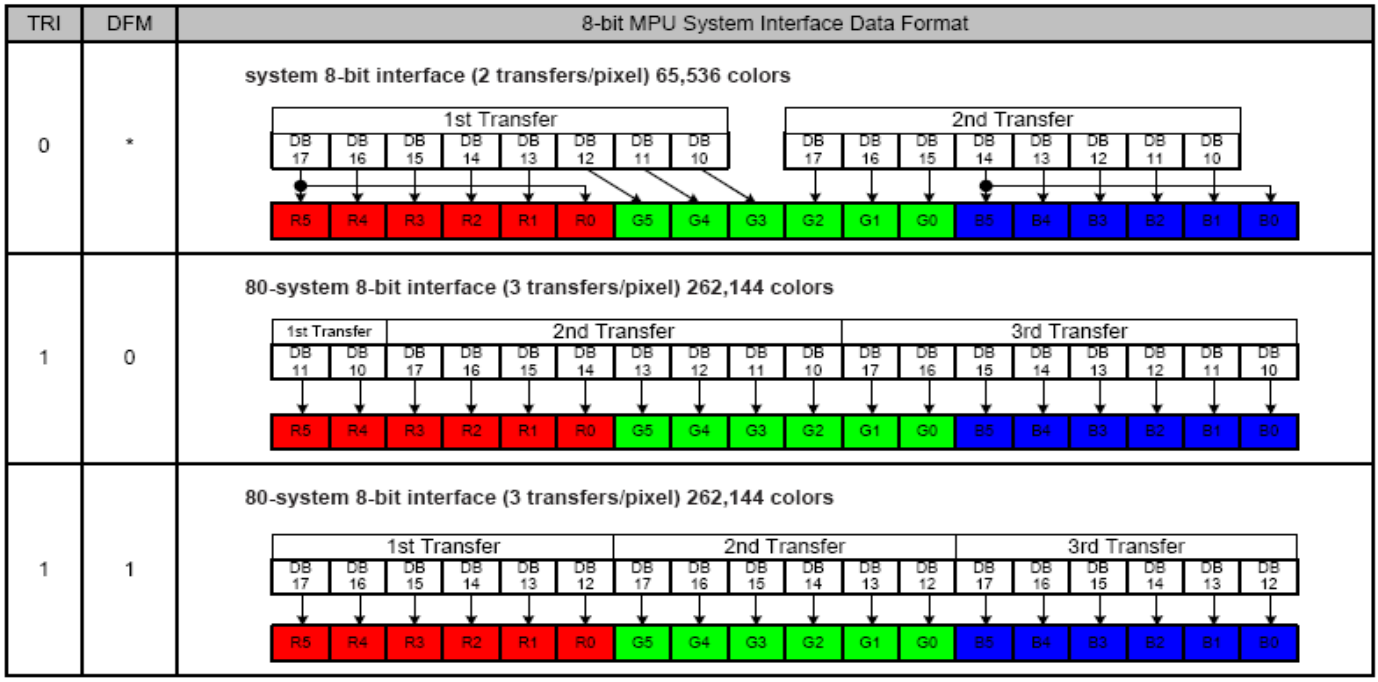
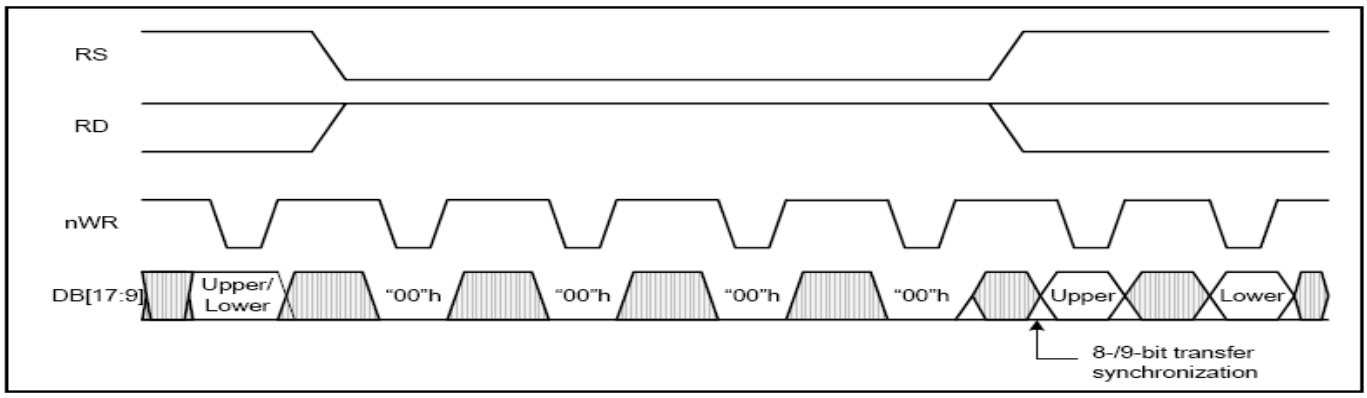
### 6.3 i80/8-bit system interface

The i80/8-bit system interface is selected by setting the IM[3:0] as "0011" and the DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to GND.




**Data transfer synchronization in 8/9-bit bus interface mode**

ILI9325 supports a data transfer synchronization function to reset upper and lower counters which count the transfers numbers of upper and lower byte in 8/9-bit interface mode. If a mismatch arises in the numbers of transfers between the upper and lower byte counters due to noise and so on, the "00"h register is written 4 times consecutively to reset the upper and lower counters so that data transfer will restart with a transfer of upper byte. This synchronization function can effectively prevent display error if the upper/lower counters are periodically reset.



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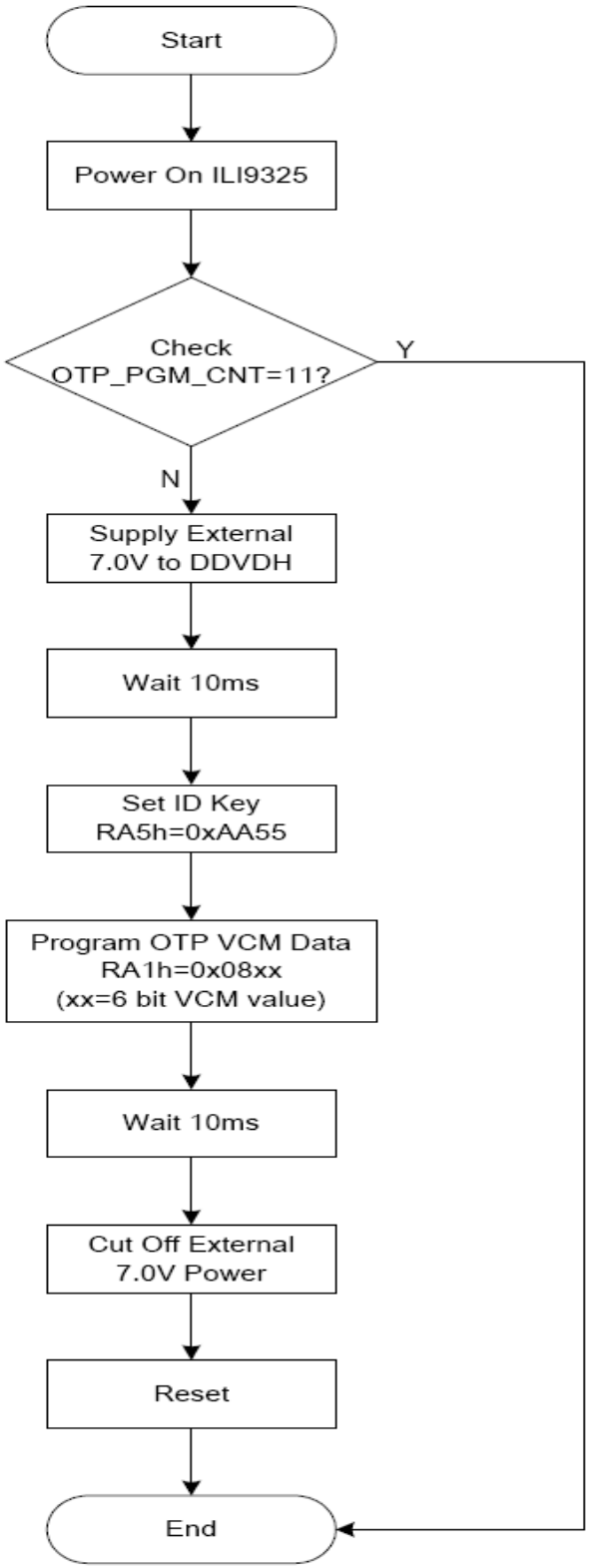
## 7. OTP programming flow



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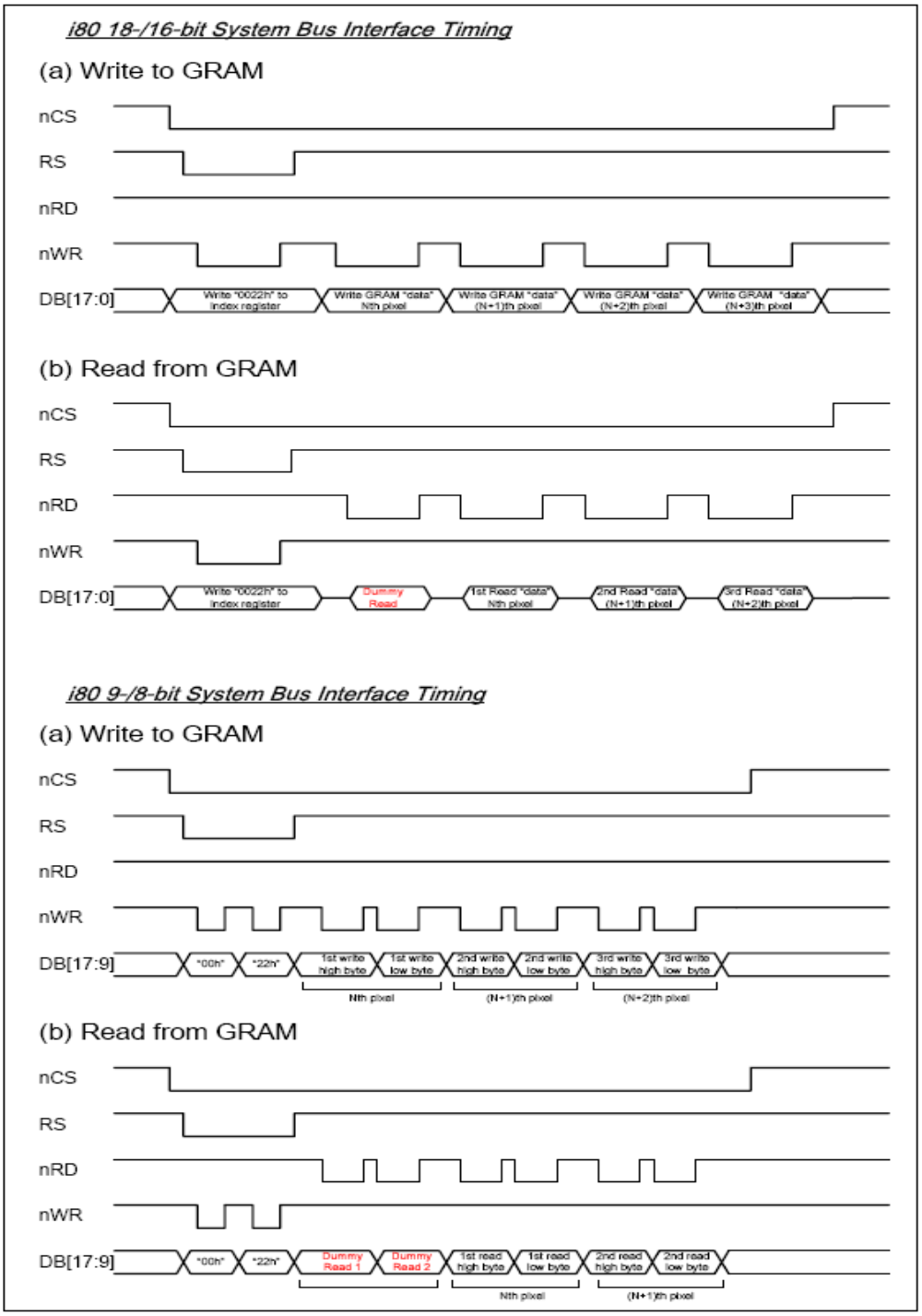
## 8. Gram address map & read / write

ILI9325 has an internal graphics RAM (GRAM) of 87,120 bytes to store the display data and one pixel is constructed of 18 bits. The GRAM can be accessed through the i80 system, SPI and RGB interfaces.



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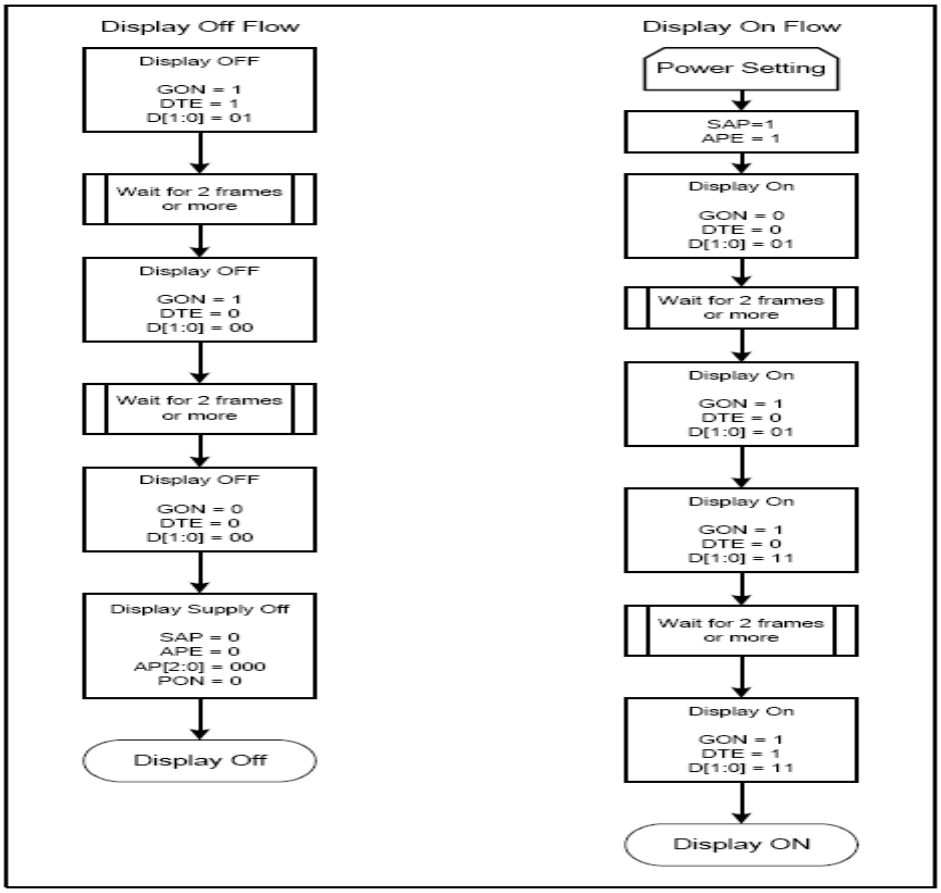
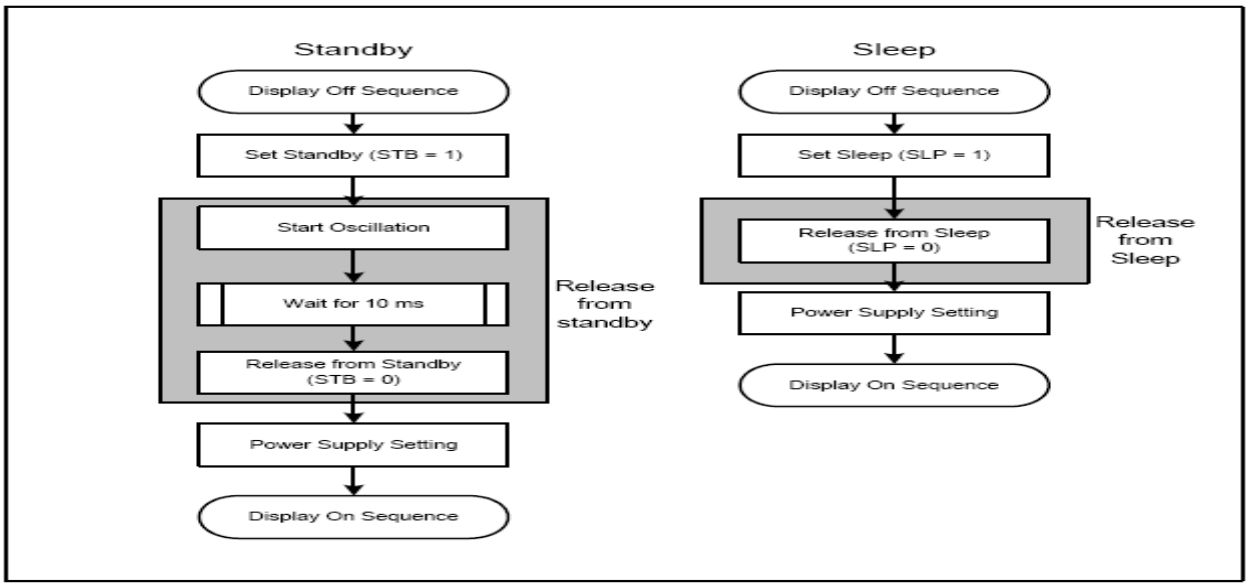
# 9. Application

## 9.1 Display ON/OFF sequence




## 9.2 Standby and sleep



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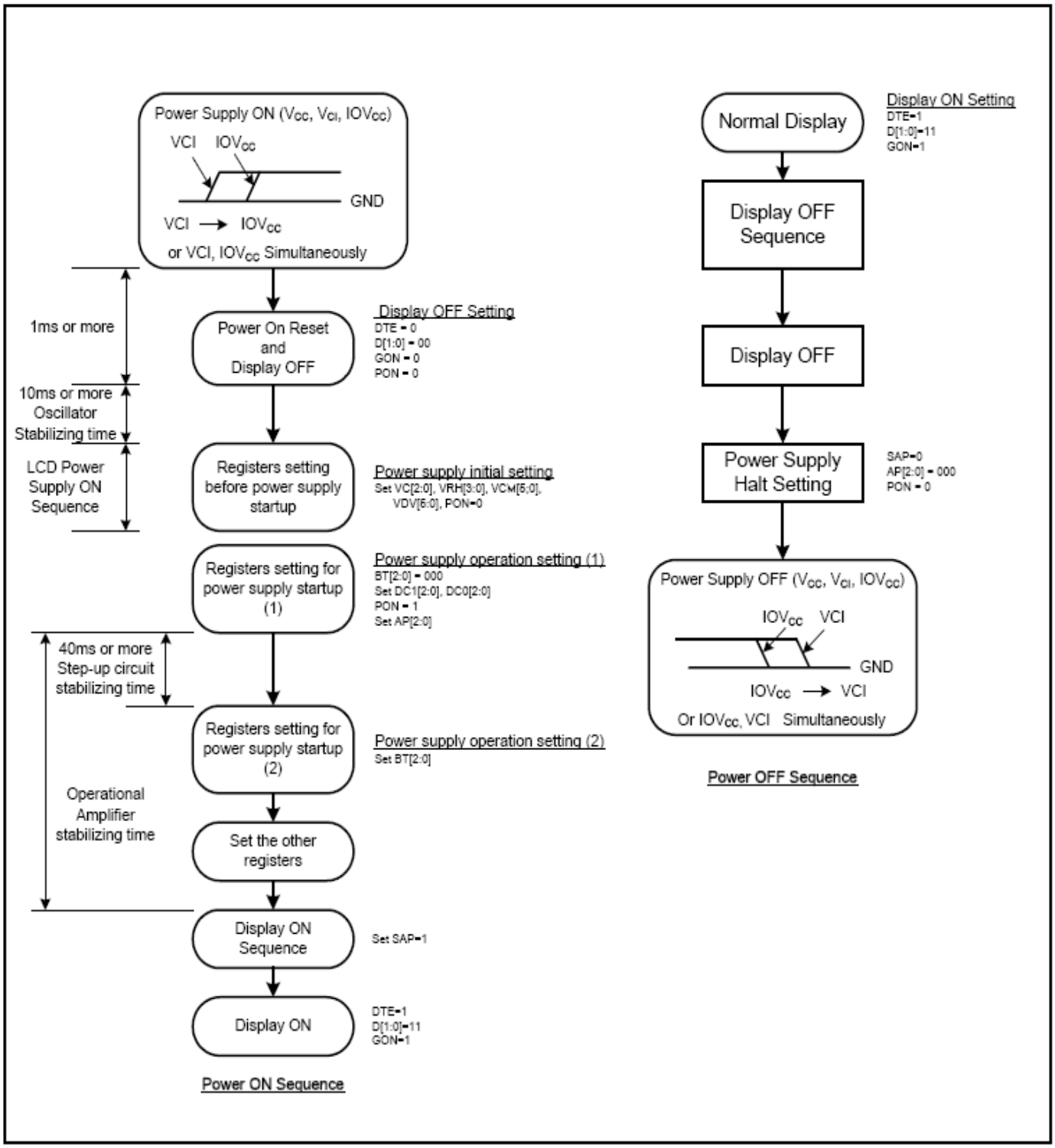
### 9.3 Power supply configuration

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on external resistance and capacitance.



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## 10. CMO panel

```
void ILI9325_CMO24_Initial(void)
{
  // VCI=2.8V
  //************* Reset LCD Driver ****************//
    LCD_nRESET = 1;
      delayms(1);   // Delay 1ms
    LCD_nRESET = 0;
      delayms(10); // Delay 10ms                  // This delay time is necessary
    LCD_nRESET = 1;
      delayms(50); // Delay 50 ms
  //************* Start Initial Sequence **********//
    LCD_CtrlWrite_ILI9325(0x00E3, 0x3008);     // Set internal timing
    LCD_CtrlWrite_ILI9325(0x00E7, 0x0012);     // Set internal timing
    LCD_CtrlWrite_ILI9325(0x00EF, 0x1231);     // Set internal timing
    LCD_CtrlWrite_ILI9325(0x0001, 0x0100);      // set SS and SM bit
    LCD_CtrlWrite_ILI9325(0x0002, 0x0700);      // set 1 line inversion
    LCD_CtrlWrite_ILI9325(0x0003, 0x1030);      // set GRAM write direction and BGR=1.
    LCD_CtrlWrite_ILI9325(0x0004, 0x0000);      // Resize register
    LCD_CtrlWrite_ILI9325(0x0008, 0x0207);      // set the back porch and front porch
    LCD_CtrlWrite_ILI9325(0x0009, 0x0000);      // set non-display area refresh cycle ISC[3:0]
    LCD_CtrlWrite_ILI9325(0x000A, 0x0000);      // FMARK function
    LCD_CtrlWrite_ILI9325(0x000C, 0x0000);      // RGB interface setting
    LCD_CtrlWrite_ILI9325(0x000D, 0x0000);      // Frame marker Position
    LCD_CtrlWrite_ILI9325(0x000F, 0x0000);       // RGB interface polarity
  //*************Power On sequence ****************//
    LCD_CtrlWrite_ILI9325(0x0010, 0x0000);         // SAP, BT[3:0], AP, DSTB, SLP, STB
    LCD_CtrlWrite_ILI9325(0x0011, 0x0007);         // DC1[2:0], DC0[2:0], VC[2:0]
    LCD_CtrlWrite_ILI9325(0x0012, 0x0000);         // VREG1OUT voltage
    LCD_CtrlWrite_ILI9325(0x0013, 0x0000);         // VDV[4:0] for VCOM amplitude
      delayms(200);                                // Dis-charge capacitor power voltage
    LCD_CtrlWrite_ILI9325(0x0010, 0x1490);         // SAP, BT[3:0], AP, DSTB, SLP, STB
    LCD_CtrlWrite_ILI9325(0x0011, 0x0227);         // Set DC1[2:0], DC0[2:0], VC[2:0]
      delayms(50);                                     // Delay 50ms
    LCD_CtrlWrite_ILI9325(0x0012, 0x001D);          // External reference voltage= Vci;
      delayms(50);                                     // Delay 50ms
    LCD_CtrlWrite_ILI9325(0x0013, 0x1A00);          // Set VDV[4:0] for VCOM amplitude
    LCD_CtrlWrite_ILI9325(0x0029, 0x000B);          // SetVCM[5:0] for VCOMH
    LCD_CtrlWrite_ILI9325(0x002B, 0x000D);           // Set Frame Rate
      delayms(50);                                    // Delay 50ms
    LCD_CtrlWrite_ILI9325(0x0020, 0x0000);          // GRAM horizontal Address
    LCD_CtrlWrite_ILI9325(0x0021, 0x0000);          // GRAM Vertical Address
  // ----------- Adjust the Gamma    Curve ----------//
    LCD_CtrlWrite_ILI9325(0x0030, 0x0007);
    LCD_CtrlWrite_ILI9325(0x0031, 0x0206);
    LCD_CtrlWrite_ILI9325(0x0032, 0x0506);
    LCD_CtrlWrite_ILI9325(0x0035, 0x0704);
    LCD_CtrlWrite_ILI9325(0x0036, 0x1203);
    LCD_CtrlWrite_ILI9325(0x0037, 0x0007);
    LCD_CtrlWrite_ILI9325(0x0038, 0x0000);
    LCD_CtrlWrite_ILI9325(0x0039, 0x0706);
    LCD_CtrlWrite_ILI9325(0x003C, 0x0701);
    LCD_CtrlWrite_ILI9325(0x003D, 0x000F);
  //------------------ Set GRAM area ---------------//
    LCD_CtrlWrite_ILI9325(0x0050, 0x0000);        // Horizontal GRAM Start Address
    LCD_CtrlWrite_ILI9325(0x0051, 0x00EF);        // Horizontal GRAM End Address
    LCD_CtrlWrite_ILI9325(0x0052, 0x0000);        // Vertical GRAM Start Address
    LCD_CtrlWrite_ILI9325(0x0053, 0x013F);        // Vertical GRAM Start Address
    LCD_CtrlWrite_ILI9325(0x0060, 0xA700);        // Gate Scan Line
```

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```
    LCD_CtrlWrite_ILI9325(0x0061, 0x0001);      // NDL,VLE, REV
    LCD_CtrlWrite_ILI9325(0x006A, 0x0000);      // set scrolling line
  //---------- Partial Display Control ---------//
    LCD_CtrlWrite_ILI9325(0x0080, 0x0000);
    LCD_CtrlWrite_ILI9325(0x0081, 0x0000);
    LCD_CtrlWrite_ILI9325(0x0082, 0x0000);
    LCD_CtrlWrite_ILI9325(0x0083, 0x0000);
    LCD_CtrlWrite_ILI9325(0x0084, 0x0000);
    LCD_CtrlWrite_ILI9325(0x0085, 0x0000);
  //---------- Panel Control ----------//
    LCD_CtrlWrite_ILI9325(0x0090, 0x0010);
    LCD_CtrlWrite_ILI9325(0x0092, 0x0600);
    LCD_CtrlWrite_ILI9325(0x0093, 0x0003);
    LCD_CtrlWrite_ILI9325(0x0095, 0x0110);
    LCD_CtrlWrite_ILI9325(0x0097, 0x0000);
    LCD_CtrlWrite_ILI9325(0x0098, 0x0000);

    LCD_CtrlWrite_ILI9325(0x0007, 0x0133);      // 262K color and display ON
}

void LCD_EnterSleep_ILI9325(void)
{
  LCD_CtrlWrite_ILI9325(0x0007, 0x0131);        // Set D1=0, D0=1
    delayms(10);
  LCD_CtrlWrite_ILI9325(0x0007, 0x0130);        // Set D1=0, D0=0
    delayms(10);
  LCD_CtrlWrite_ILI9325(0x0007, 0x0000);        // display OFF
  //************* Power OFF sequence **************//
  LCD_CtrlWrite_ILI9325(0x0010, 0x0000);          // SAP, BT[3:0], APE, AP, DSTB, SLP
  LCD_CtrlWrite_ILI9325(0x0011, 0x0000);          // DC1[2:0], DC0[2:0], VC[2:0]
  LCD_CtrlWrite_ILI9325(0x0012, 0x0000);          // VREG1OUT voltage
  LCD_CtrlWrite_ILI9325(0x0013, 0x0000);          // VDV[4:0] for VCOM amplitude
    delayms(200);                                 // Dis-charge capacitor power voltage
  LCD_CtrlWrite_ILI9325(0x0010, 0x0002);          // SAP, BT[3:0], APE, AP, DSTB, SLP
}


void LCD_ExitSleep_ILI9325(void)
{
//*************Power On sequence ******************//
  LCD_CtrlWrite_ILI9325(0x0010, 0x0000);        // SAP, BT[3:0], AP, DSTB, SLP
  LCD_CtrlWrite_ILI9325(0x0011, 0x0000);        // DC1[2:0], DC0[2:0], VC[2:0]
  LCD_CtrlWrite_ILI9325(0x0012, 0x0000);        // VREG1OUT voltage
  LCD_CtrlWrite_ILI9325(0x0013, 0x0000);        // VDV[4:0] for VCOM amplitude
    delayms(200);                               // Dis-charge capacitor power voltage
  LCD_CtrlWrite_ILI9325(0x0010, 0x1490);        // SAP, BT[3:0], AP, DSTB, SLP, STB
  LCD_CtrlWrite_ILI9325(0x0011, 0x0227);        // Set DC1[2:0], DC0[2:0], VC[2:0]
      delayms(50);                              // Delay 50ms
  LCD_CtrlWrite_ILI9325(0x0012, 0x001D);        // External reference voltage =Vci;
      delayms(50);                              // Delay 50ms
  LCD_CtrlWrite_ILI9325(0x0013, 0x1A00);        // Set VDV[4:0] for VCOM amplitude
  LCD_CtrlWrite_ILI9325(0x0029, 0x000B);        // Set VCM[5:0] for VCOMH
    delayms(50);                                // Delay 50ms
  LCD_CtrlWrite_ILI9325(0x0007, 0x0133);        // 262K color and display ON
}
```

## 11. Notice packing method

Pack the products so that they may not touch each other.

Put the inner cartons containing module into outer carton.

Attach the display label on the visible location on the outer carton.