SAMSUNG ELECTRONICS

S6D0154

Rev. 1.00

MOBILE DISPLAY DRIVER IC

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IMPORTANT NOTICE!!

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.
2. Always test and inspect products under the environment with no penetration of light.

Revision History

Ver.	Date	History
1.00	2007-10-08	- Added note.2 in Table 2.S6D0154 Pad Dimensions - Added Figure 13.MDDI Receiver, Driver Electrical Diagram, Figure 14.Host enable/disable time and Client enable/disable time diagram and Table 21. Receiver AC Characteristics - Modified Figure 19. Power Up Sequence Timing Diagram and Figure 20. Power Down Sequence Timing Diagram Blank Display → Non Display, White Display → Blank Display - Divided “MTP Initialization, Erase and program” into “a. Using VCI for MTP” and “b. Using VCI1 for MTP” - Modified Table 10.Interface Pad Configuration When MDDI is used, CSB & RW_WRB : VDD3 → VDD3/VSS - Modified note.1 in Figure 43.Power-Up Pattern Diagram & An Example Of Source/VCOM Waveforms - Modified unused bits in 9.3.34. MTP Data Write (R82h) “0” → don’t care - Added note in Figure 134.Application Circuit Example - Added 19.3. EXTERNAL COMPONENT - Correct some misspellings
0.20	2007-08-28	- Added 4.2. Bump PAD Information - Modified form of Table 2.S6D0154 Pad Dimensions - Added explanation to description of VCI_MDDI in Table 3.Pads for power supplies. - Modified pad descriptions of DB[17:0], S_CSB, S_RS, S_WRB, GPIO[5:0] and S_DB[8:0] in Table 5. Signal pads for Interface Logic - Added 5.3. INTERFACE PAD CONFIGURATION - Modified SAP3-0 parameter table in R10h command 0001/0010 → Setting Disable - Deleted NOTE of AB_VCI1 parameter in R11h command - Added additional description of FCV_EN parameter in R40h command - Corrected misspellings in R42h/R43h command Initial value of SUB_SEL : 42h → 4Ah register address : 43h → 4Ah initial state : 42h → 4Ah - Added protection bit description of MTP_DOUT parameter in R82h command - Modified 10.RESET FUNCTION SUB_SEL = 00000000 → 01001010 (4Ah) SUB_WR = 00000000 → 00100010 (22h) TEST_KEY = 10001100 → 00000000 (00h) - Modified Figure 40.Power-Up Pattern Diagram & An Example Of Source/VCOM Waveforms and Figure 41.Setup Flow of Generated Power Supply - Added Section C. TFT-type Sub panel control signal speed in 13.15.2. STN type sub panel timing - Modified Figure 127.D-STAND-BY/STAND-BY SEQUENCE and Figure 128.DEEP STAND-BY EXIT FLOW - Modified Figure 129.Oscillation Circuit - Modified Table 17.RGB Data Interface Characteristics tHE : HBP → 255 - Deleted Ircv-act and Ircv-hib in Table 19.Data/Strobe Rx DC Characteristics - Deleted Idrv-act and Idrv-tri in Table 20.Driver Electrical DC Characteristics - Modified 6.6. External Power On/Off Sequence - Correct some misspellings in 8. PLUG & PLAY FUNCTION SPECIFICATION PNP_EN = Low → High - Correct some misspellings in MDT parameter description 16-bit (68/80-system), MDT1=1 → MDT0=1 - Added additional description of 13.12. MDDI OPERATION Table - Modified Table 36.Display State and Interface - Mofified Figure 33.Flow of MTP Load / Read deleted TEST_KEY - Modified Figure 24.Interlace drive and output waveform (Two Line Mixed Inversion) - Modified Figure 103.Main / Sub panel selection procedure - Modified Figure 87.Differential connection between host and client - Modified description in 13.3. MDDI Data & STB - Modified Figure 93.Link shutdown packet structure - Correct some misspellings in 13.9. GPIO CONTROL 3 GPIOs → 6 GPIOs - Modified description in 13.13. SUB PANEL CONTROL - Added Note in Table 29.Relationship between EPL, ENABLE and RAM access and Table 36.Display State and Interface - Added Note of VCIR parameter in 9.3.15. VCI Recycling (R15h) - Correct some misspellings in 9.3.19. Software Reset (R28h) zero → high - Modified Figure 17.Power Up Sequence Timing Diagram - Modified DM parameter table in 9.3.10. External Display Interface Control (R0Ch) - Modified bus assignment of GPIO parameter in MTP Data Read (R82H) - Added Istby, Idstby, IVDD3 and IVCI in Table 13.DC Characteristics For LCD Driver Outputs - Added values of TBD in SAP parameter table of 9.3.11. Power Control 1 (R10h)

		- Modified Table 12.DC Characteristics Fosc : 320 → 323 - Modified MTP_MODE and MTP_EX parameters description in 9.3.33. MTP Control (R81h) - Modified Figure 34. and Figure 36. added Execute Initialization & Erase Flow in Program Flow - Modified MTP_DOUT parameter description in 9.3.34. MTP Data Write (R82h) - Correct some misspellings - Changed representation on the whole
0.10	2007-02-16	- Modified Various Interface (p.7) added MDDI support sentence - Modified BLOCK DIAGRAM (p.8) VCI → VDD3, SS → RL, GS → TB - Modified Chip Configuration (p.9) VCOMR *2 pad → VCOMR pad - Modified MDDI pad description (p.22,25) floating → VSS - Added CONTACT pad description (p.26) - Modified FLM and CL1 pad descriptions (p.26) - Added MDDI description (p.27) - Modified Table 18, 19 and 20. (p.30, p.32, p.33) - Modified Index register range (p.37) ID6-0 → ID7-0 - Modified Version Management (R00h) description (p.37) - Added note (p.39, p.41) [NOTE] When SM = 1, NL setting is disable. - Changed parameter name (p.48) TEMON → FLM_MON - Added Figure 12. Two Line Mixed Inversion (p.44) - Modified FP and BP (p.50) FP → BP - Modified Start Oscillation(R0Fh) (p.56) - Deleted AB2A parameter (p.57) VCOMH → VCOMH/VCOML - Added AB_VCI1 parameter (p.58) - GVD6-0,VCM6-0,VML6-0 table full range description (p.62~66) - Modified VCOMG description (p.64) - Modified Note3. (p.65) - Added FLM Function(R29h) (p.72) - Modified Figure 18. Vertical Scroll Display (p.77) - Modified SUB_IM1-0 table (p.81) 00,10 → setting disable - Modified MTP_SEL parameter description (p.84) - Added Note. (p.85) - Added MTP_DOUT register (p.85) - Added Product Name/Version Write(R83h) (p.89) - Modified Figure 21, 22, 23 and 24. (p.86, p.87) - Changed reset value of SAP and MTP_SEL parameter (p.90) SAP3-0=0000 → SAP3-0=0010, MTP_SEL=1 → MTP_SEL=0 - Modified Figure 27. (p.92) - Modified Figure 54. (p.105) - Modified Sub Panel Control Timing (p.134~p.138) deleted 18/16 bit Sub Panel Interface - Modified Figure 106. (p.143) VINP1/VINN1, VINP6/VINN6 : 3R → 9R - Deleted contents related with DIV (p.163) - Modified Table 49. (p.165) - Modified Table 50. DC Characteristics (p.166) VGH : ILOAD=0.2mA → 0.1mA VGL : ILOAD=0.2mA → 0.1mA - Corrected parameter that is not used from “don’t care” to “0” - Moved GPIO3-0 from R0Eh to R82h - Added APPLICAION CIRCUIT, AC CHARACTERISTICS, RESET TIMING, EXTERNAL POWER ON/OFF SEQUENCE, MDDI IO DC/AC CHARACTERISTICS - Correct some misspellings

Contents

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1. Introduction

1.1. Purpose of this document

This document is to provide an electrical and mechanical reference specification of S6D0154 driver IC developed by Samsung. This would be a reference design guide for display panel module makers so that the display module subassembly can be designed properly.

1.2. Product options

S6D0154 is a single-chip CMOS LCD controller/driver for color TFT-LCD displays supporting the panel resolution of 320 gates and 240xRGB columns. It contains a 260k-bit (240 x 320 x 18-bit) display graphic RAM and a full set of control functions. S6D0154 comes with a multiple options based on customer's need, where some of functions are slightly different. The description of each option is described in Table 1. For example, S6D0154-X01 version supports various types of peripheral interface such as 80-series MCU interface (8-/9-/16-/18-bit data), 68-Series MCU interface (8-/9-/16-/18-bits data), and serial interface.

Table 1. List of S6D0154 options.

Options	Remarks

2. Features

- **240-RGB x 320-dot Resolution, 720ch Source Driver & 320ch Gate Driver**
- **Various color-display control functions**
  - 262,144 colors can be displayed at the same time (including gamma adjust)
  - 65,536 colors, 8 colors can be displayed
- **MPU/SPI/RGB Interfaces**
  - 18-/16-/9-/8-bit high-speed parallel bus interfaces including MDT (Multiple Data Transfer) mode.
  - Serial peripheral interface(SPI)
  - 18-/16-/6-bit RGB interfaces for motion picture display.
  - MDDI (Mobile Display Digital Interface)
- **Various Graphic Operations**
  - Window-Addressing Function to display motion picture independently of still image display
  - Image Rotating / Mirroring Function
- **Built-in GRAM : 240 x 18 x 320 = 1,382,400 bits**
- **Alternating functions for TFT-LCD common-electrode power**
- **Low-power operation supports**
  - Power-save functions (standby mode, deep-standby mode)
  - Partial display in any position
  - Voltage step-up circuit up to 7 times for generating driving voltage
  - Charge-recycling function for the switching performance of step-up circuits and operational amplifiers
- **An Internal oscillator and external hardware reset**
- **Internal power supply circuit**
  - Voltage Step-up circuit: five to seven times, positive-polarity inversion
- **Operating voltage**
  - 1.65V–3.3V for I/O supply voltage range for VDD3
  - 2.5V–3.3V for Analog supply voltage range for VCI
- **Voltage supplies generated internally**
  - 2.5V to 5.0V Source output voltage range for GVDD to AVSS
  - 4.5V to 6.0V (See Note 1) Power supply for driver circuit range for AVDD to AVSS
  - Max 6.0V Common electrode output voltage range for VCOM
  - Min 11.25V to 16.5V (See Note 2) Positive Gate output voltage range for VGH to AVSS
  - -13.75 V to -6.75V (See Note 2) Negative Gate output voltage range for VGL to AVSS

Note.

1. AVDD Min: When VCI1 = 2.25V, AVDD Max: When VCI1=3.0V
2. |VGH| & |VGL| Min : When VCI1 = 2.25V, |VGL| Max : When VCI1=2.75V, |VGH - VGL| Max : 30.0V
3. |VGH| max. should be lower than or equal to 16.5V in normal operating condition, regardless of VCI1 & BT settings.

3. Display Module Block Diagram

3.1. Signal flow of the display module and its relationship

Figure 1 shows the block diagram of a mobile display panel module and related interface signals required by set makers and module makers. Level I interface signals are usually required by a set maker who would then request the display module such a function, and Level II interface signals are required by a display module maker for its own purpose.

There are also Level III signals which is for the internal use only for the driver IC itself. Level III signals are not intended to be released to the customers since it is designed for a specific manufacturing purpose, and it may alter the functions of IC if it is misused.

This reference specification only provide a guideline to Level I and II interface signals since some of specifications related to Level I and II need a margin on IC side and would not be necessarily the same as the one in Level I and II specification even though both uses the same interface signals. This is mainly due to the parasitic and design requirements within the flexible PCB used by a display module maker. IC specification will offer related information among Level I/II on how each interface signal relates each other.

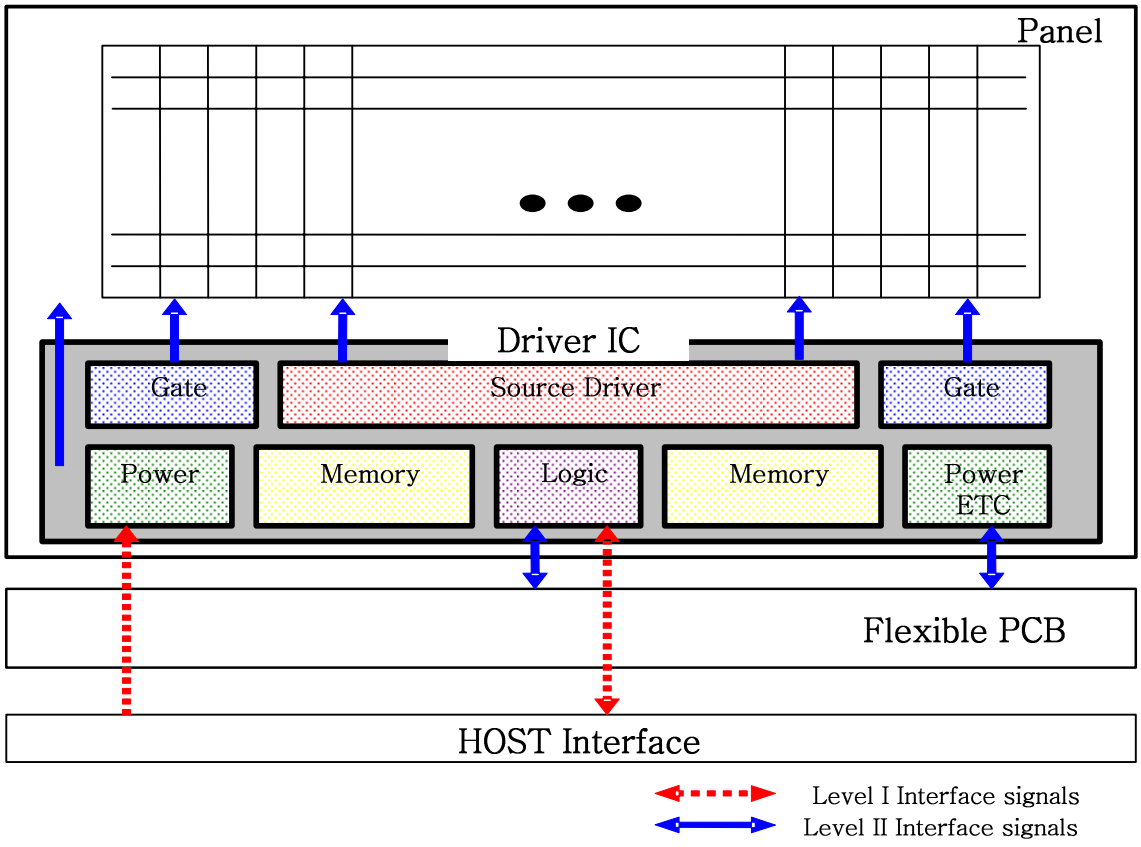


Figure 1. The interface signal flow of a mobile display panel module

3.2. Function Block Diagram and Signal Pads of S6D0154

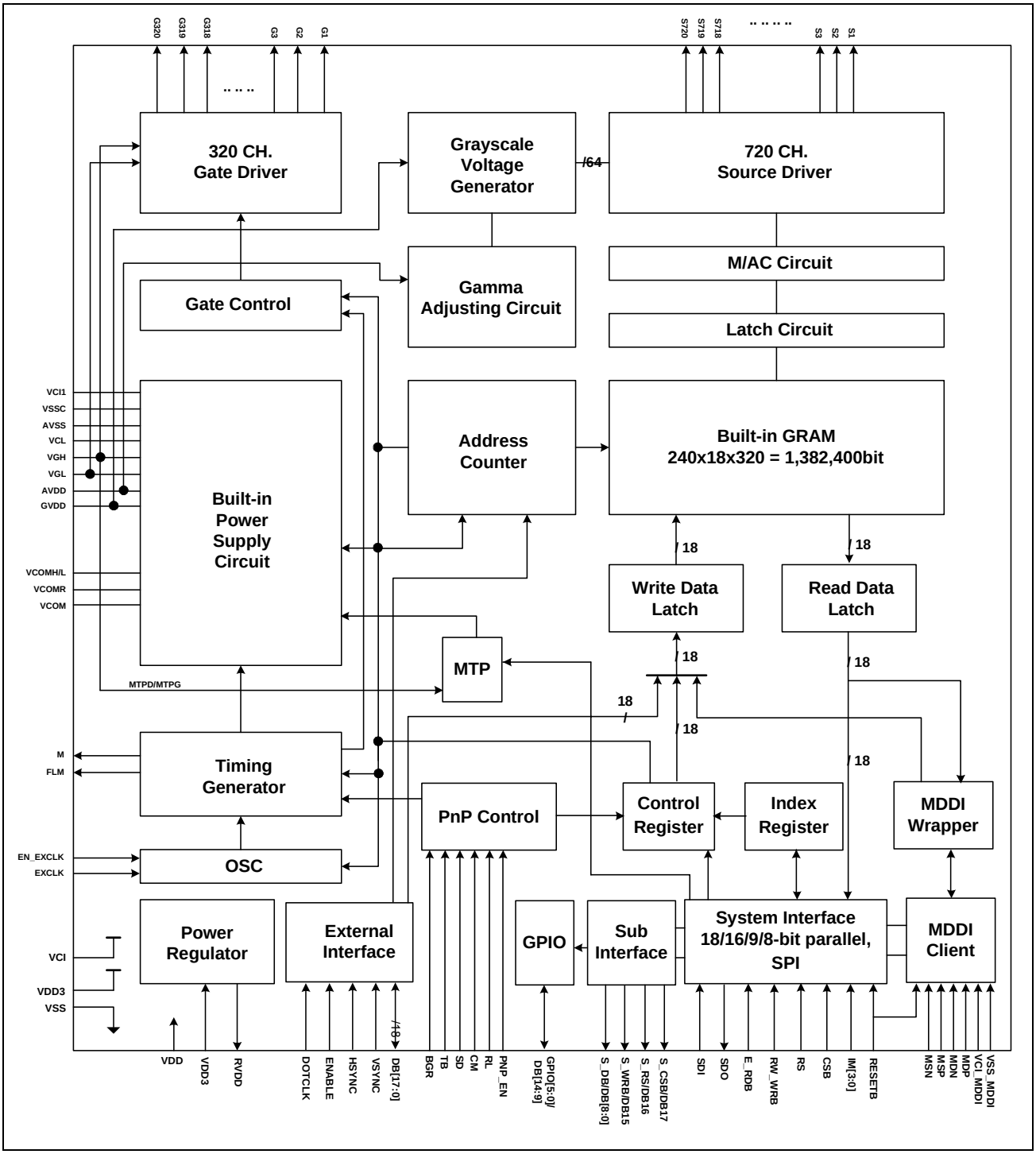


Figure 2. The functional block diagram and signal pads of S6D0154.

4. Chip Information

4.1. PAD Configuration

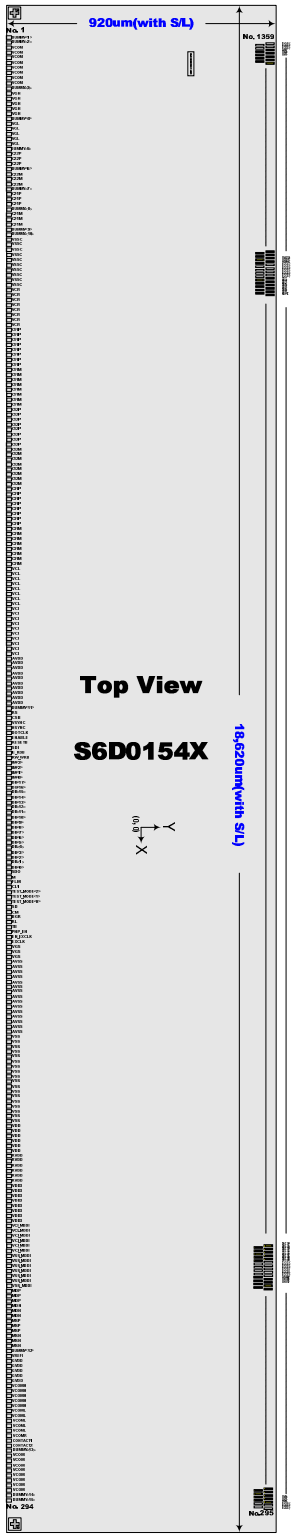
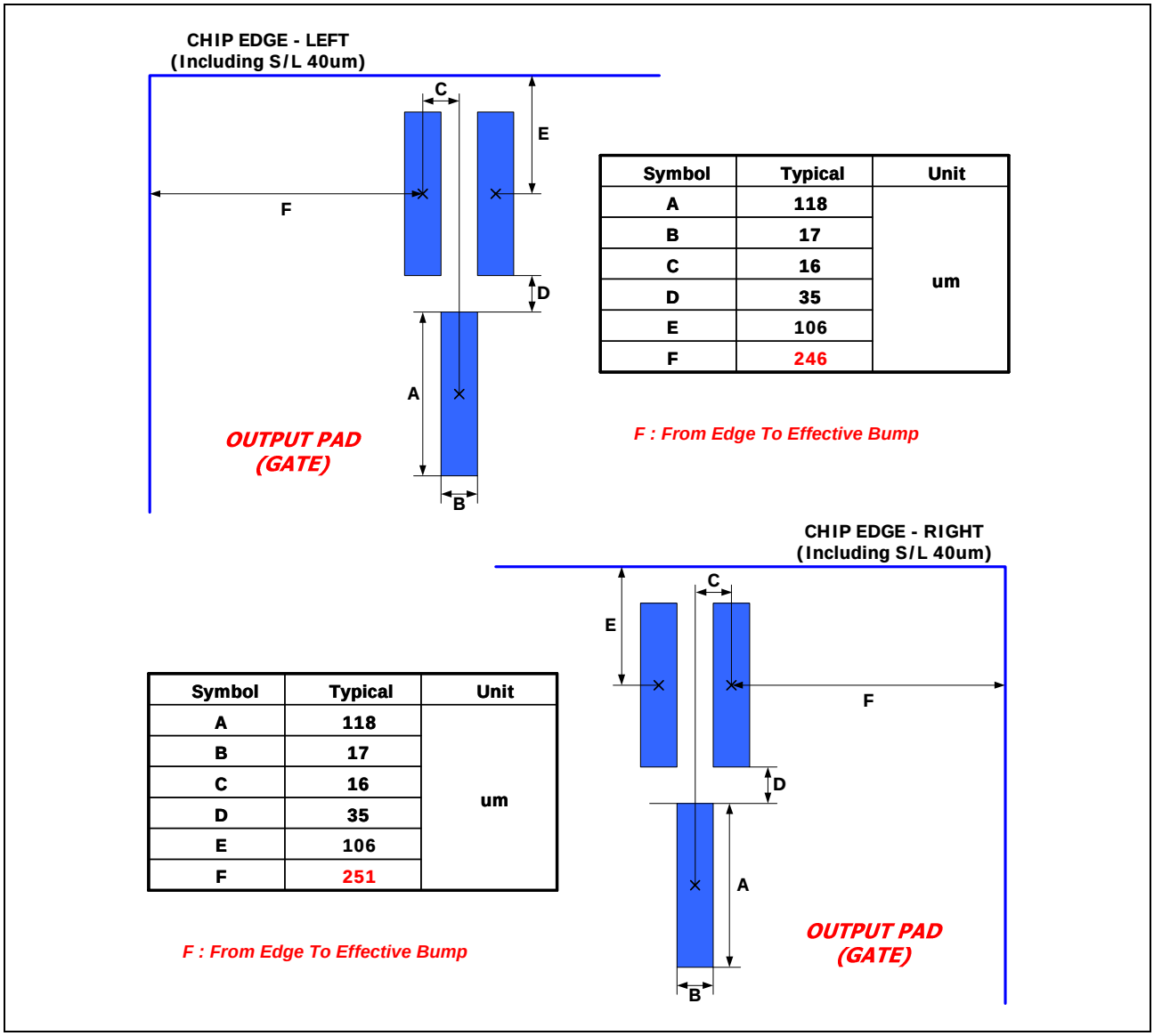


Figure 3. Chip Layout

4.2. Bump PAD Information



Symbol	Typical	Unit
A	118	um
B	17	
C	16	
D	35	
E	106	
F	246	

F : From Edge To Effective Bump

Symbol	Typical	Unit
A	118	um
B	17	
C	16	
D	35	
E	106	
F	251	

F : From Edge To Effective Bump

Figure 4. Pad Configuration – Output

Table 2. S6D0154 Pad Dimensions

Items	Pad name.	Size		Unit
		X	Y	
Chip Size[1)]	-	18,620	920	um
Bumped Pad Size	Input Pads (60um / 85um pitch)	40±2	56±2	
	Output Pads (16um pitch)	17±2	118±2	
Bumped Pad Height	In Wafer	15(typ.) ±3		
	In Chip	Under 2		

Note.

1. Scribe lane is included in this chip size (Scribe lane: 80um)
2. wafer thickness :
   - S6D0154●●●-●●●8 : 300±10 um
   - S6D0154●●●-●●●9 : 280±10 um
   - S6D0154●●●-●●●Y : 470±10 um

4.3. ALIGN KEY CONFIGURATION AND COORDINATES

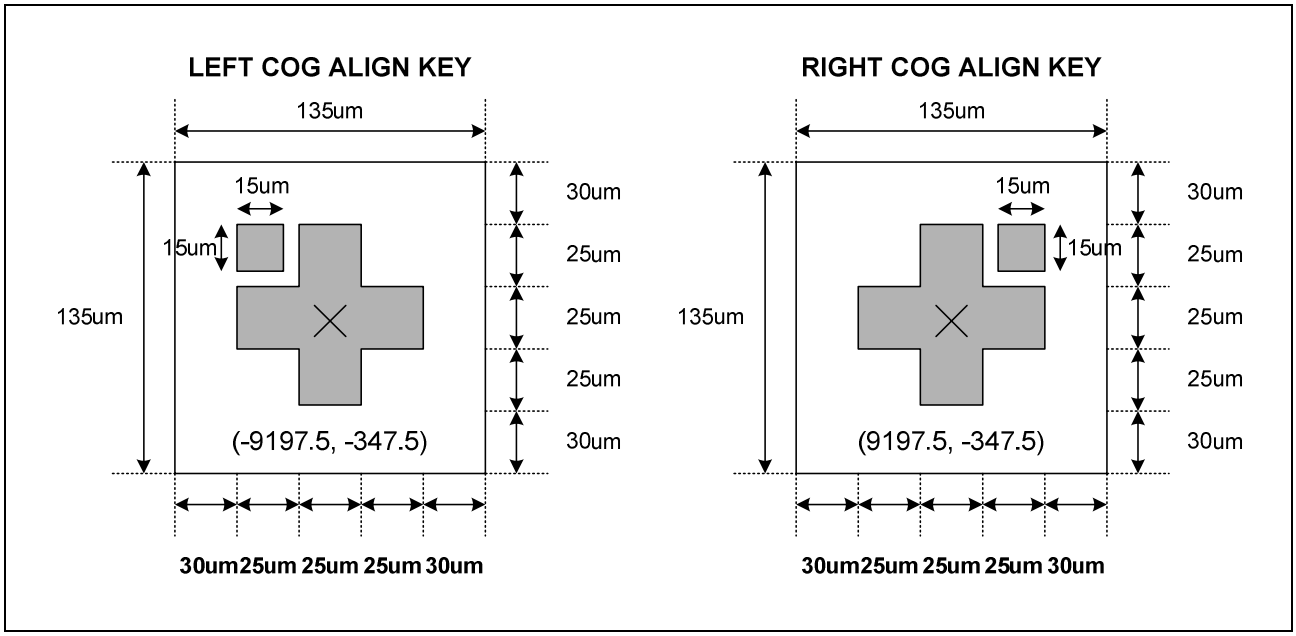


Figure 5. COG Align Keys

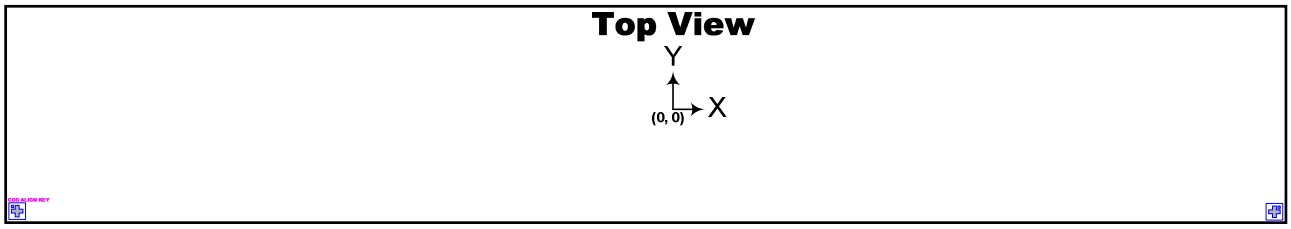


Figure 6. Align Key reference(only COG align key exist).

5. IC Pad Description

5.1. Pads for Power Supplies

Table 3. Pads for power supplies.

Symbol	I/O	Description
RVDD	O	Voltage regulator output for VDD. Connect this to VDD pad for supplying power. Connect a capacitor for stabilization.
VDD	I	Power supply for memory and internal logic circuit. Connect this pad to RVDD pad Do not apply any external power to this pad over 1.5V.
VDD3	P	Power supply for I/O block.
VCI	P	Power supply for analog and voltage booster block.
VCI_MDDI	I	Power supply for MDDI I/O block. Must be connected to VCI level when not in use.
AVSS	P	GND for analog circuits
VSSC	P	GND for booster circuits.
VSS	P	GND for logic circuits.
VSS_MDDI	I	GND for MDDI I/O
AVDD	O	Internally generated voltage output pad for source driver block. Output voltage of 1st booster circuit (=2 x VCI1) Input voltage to 2nd booster circuit. This pad needs to an external bypass capacitor..
VCI1	O	Reference input voltage for 1st booster circuit. Connect a capacitor for stabilization. Note. VCI1 cannot exceed 3V
VGH	O	Positive power output of the 2nd booster circuit. Gate “ON” level voltage. Connect a capacitor for storage function.
VGL	O	Negative power output of the 2nd booster circuit. Gate “OFF” level voltage. Connect a capacitor for storage function.
VCL	O	3rd booster output voltage. Power supply for generating VCOML block. Connect a capacitor for storage function.
VGS	I	Reference voltage input for grayscale voltage generator. Connect an external resistor or to system ground.
VREFI	I/O	Reference voltage for generating GVDD voltage.
GVDD	O	Reference voltage input for grayscale voltage generator. Reference voltage input for VCOMH / VCOML voltage generator. An internal register can be used to adjust the GVDD voltage. Connect a capacitor for stabilization.
VCOMH	O	High level output voltage of VCOM. An internal register can be used to adjust the VCOMH voltage. Connect a capacitor for stabilization.
VCOML	O	Low level output voltage of VCOM. An internal register can be used to adjust the difference voltage between VCOMH and VCOML. Connect a capacitor for stabilization.

Table 4. Power supply pad description (continued)

Symbol	I/O	Description
VCOM	O	Power supply pad for the TFT- display common electrode. The alternating cycle can be set by the “M” pad. Charge recycling method is used with VCI voltage. Connect this pad to the TFT-display common electrode
VCOMR	I/O	Reference voltage input pad for VCOMH. When VCOMH voltage is adjusted externally, halt the internal adjuster of VCOMH by setting the register and insert a variable resistor between GVDD and VSS. When VCOMH is not adjusted externally, leave this pad open and adjust VCOMH by setting the internal register.
C11P, C11M C12P, C12M	-	Connect the charge-pumping capacitor for generating AVDD level.
C21P, C21M C22P, C22M	-	Connect the charge-pumping capacitor for generating VGH, VGL level.
C31P, C31M	-	Connect the charge-pumping capacitor for generating VCL level.

5.2. Signal pads for Logic interface

Table 5. Signal pads for Interface Logic

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>IM[3:0] / ID</td><td>I</td><td>Selects the interface mode.
<table>
<tr><th>IM[3:0]</th><th>Description</th></tr>
<tr><td>0000</td><td>68-Series 16-bit MPU interface</td></tr>
<tr><td>0001</td><td>68-Series 8-bit MPU interface</td></tr>
<tr><td>0010</td><td>80-Series 16-bit MPU interface</td></tr>
<tr><td>0011</td><td>80-Series 8-bit MPU interface</td></tr>
<tr><td>010x</td><td>Serial peripheral interface (SPI) IM[0] = ID</td></tr>
<tr><td>011x</td><td>Reserved</td></tr>
<tr><td>1000</td><td>68-Series 18-bit MPU interface</td></tr>
<tr><td>1001</td><td>68-Series 9-bit MPU interface</td></tr>
<tr><td>1010</td><td>80-Series 18-bit MPU interface</td></tr>
<tr><td>1011</td><td>80-Series 9-bit MPU interface</td></tr>
<tr><td>110x</td><td>HSSI (MDDI)</td></tr>
<tr><td>111x</td><td>Reserved</td></tr>
</table>
Note. “X” denotes Don’t care.</td></tr>
<tr><td>RESETB</td><td>I</td><td>Reset pad. Initializes the IC when it is low. Must be reset after power-on.</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip Select
- Low: IC is selected and can be accessed.
- High: IC is not selected and cannot be accessed.
Must be connected to VDD3 level when not in use.</td></tr>
<tr><td>RS</td><td>I</td><td>Register Select.
- Low : Index / status register
- High : Control register
Must be connected to VDD3 or VSS level when SPI mode.</td></tr>
<tr><td>RW_WRB / SCL</td><td>I</td><td>In 68-Series mode, this is used to select operation, read or write operation. (RW)
In 80-Series mode, this is used as a write strobe signal (WRB).
In SPI mode, it is used as a synchronous clock (SCL).</td></tr>
<tr><td>E_RDB</td><td>I</td><td>In 68-Series mode, this is used as write/read enable strobe (E).
In 80-Series mode, this is used as a read strobe signal. (RDB).
Must be connected to VDD3 or VSS level when SPI mode.</td></tr>
<tr><td>DB[17:0] [Note]</td><td>I/O</td><td>Data Bus.
<table>
<tr><th colspan="2">Interface Mode</th><th colspan="2">Description</th></tr>
<tr><td>IM[3:0]</td><td></td><td>Index</td><td>Data</td></tr>
<tr><td>0000</td><td>68-Series16-bit MPU interface</td><td>DB[8:1]</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>0001</td><td>68-Series 8-bit MPU interface</td><td>DB[17:10]</td><td>DB[17:10]</td></tr>
<tr><td>0010</td><td>80-Series 16-bit MPU interface</td><td>DB[8:1]</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>0011</td><td>80-Series 8-bit MPU interface</td><td>DB[17:10]</td><td>DB[17:10]</td></tr>
<tr><td>010x</td><td>Serial peripheral interface (SPI)</td><td>-</td><td>-</td></tr>
<tr><td>011x</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>1000</td><td>68-Series 18-bit MPU interface</td><td>DB[8:1]</td><td>DB[17:0]</td></tr>
<tr><td>1001</td><td>68-Series 9-bit MPU interface</td><td>DB[17:10]</td><td>DB[17:9]</td></tr>
<tr><td>1010</td><td>80-Series 18-bit MPU interface</td><td>DB[8:1]</td><td>DB[17:0]</td></tr>
<tr><td>1011</td><td>80-Series 9-bit MPU interface</td><td>DB[17:10]</td><td>DB[17:9]</td></tr>
<tr><td>11xx</td><td>Reserved</td><td>-</td><td>-</td></tr>
</table>
Must be connected to VDD3 or VSS level when not used.
<table>
<tr><th colspan="2">Interface Mode</th><th colspan="3">Description</th></tr>
<tr><td>IM[3:0]</td><td></td><td>PAD NAME</td><td>Without Sub-panel</td><td>With Sub-panel</td></tr>
<tr><td rowspan="4">4’b110x</td><td rowspan="4">HSSI (MDDI)</td><td>DB[17]</td><td>not used</td><td>S_CSB</td></tr>
<tr><td>DB[16]</td><td>not used</td><td>S_RS</td></tr>
<tr><td>DB[15]</td><td>not used</td><td>S_WRB</td></tr>
<tr><td>DB[14]</td><td>GPIO<5></td><td>GPIO<5></td></tr>
</table></td></tr>
</table>

		<table><tr><td></td><td></td><td>DB[13]</td><td>GPIO<4></td><td>GPIO<4></td></tr><tr><td></td><td></td><td>DB[12]</td><td>GPIO<3></td><td>GPIO<3></td></tr><tr><td></td><td></td><td>DB[11]</td><td>GPIO<2></td><td>GPIO<2></td></tr><tr><td></td><td></td><td>DB[10]</td><td>GPIO<1></td><td>GPIO<1></td></tr><tr><td></td><td></td><td>DB[9]</td><td>GPIO<0></td><td>GPIO<0></td></tr><tr><td></td><td></td><td>DB[8:0]</td><td>not used</td><td>S_SB[8:0]</td></tr></table>If Sub-panel is not used in MDDI mode, DB[17:15] and DB[8:0] pads should be unconnected. And unused GPIO<5:0> must be connected to VDD3 or VSS level.
SDI	I	Serial input data. Must be connected to VDD3 or VSS level when not in use.
SDO	O	Serial output data. Leave this pad open when not in use.
MDP/MDN	I/O	Differential Data input/output pads for MDDI interface. When the forward link activates, MDP/MDN receive data from the host. When the reverse link activates, MDP/MDN transmit data to the host. If MDDI is not used, this pad should be unconnected.
MSP/MSN	I/O	Differential Strobe input/output pads for MDDI interface. These pads always receive strobe data regardless of link direction. If MDDI is not used, this pad should be unconnected.
S_CSB (DB[17])	O	Chip select for Sub Panel Driver IC Low: Sub Panel Driver IC is selected and can be accessed. High: Sub Panel Driver IC is not selected and can not be accessed. If Sub-panel is not used in MDDI mode, this pad should be unconnected.
S_RS (DB[16])	O	Register select for Sub Panel Driver IC Low : Index/status, High : Control If Sub-panel is not used in MDDI mode, this pad should be unconnected.
S_WRB (DB[15])	O	Write Strobe signal for Sub Panel Driver IC Only 80-Series 18/16-bit mode is enabled, so Data is fetched at the rising edge. If Sub-panel is not used in MDDI mode, this pad should be unconnected.
GPIO[5:0] (DB[14:9])	I/O	General purpose input/output Must be connected to VDD3 or VSS level when not in use
S_DB[8:0] (DB[8:0])	O	For Sub Panel, this Signal can be used to transfer DB[8:0] data to Sub Panel Driver IC If Sub-panel is not in use in MDDI mode, this pad should be unconnected.
PNP_EN	I	Serial interface selection input pad High : Plug & play display mode Low : Plug & play disable
RL	I	When PNP_EN=High, Source output direction decision pad. RL = High : S1 → S720 scan mode RL = Low : S720 → S1 scan mode Must be connected to VSS level, when PNP_EN=Low.
CM	I	When PNP_EN=High, enable pad for 8-color display mode. CM = High : 8-color display mode CM = Low : 260k-color display mode Must be connected to VSS level, when PNP_EN=Low.
SD	I	Display decision pad. When PNP_EN=High SD = High : Shut down (power off & Standby sequence) SD = Low : Display on sequence. Must be connected to VSS level, when PNP_EN=Low.
TB	I	When PNP_EN=High, Determines the order of gate driver output array. TB = High : G1 → G320 scan mode TB = Low : G320 → G1 scan mode Must be connected at VSS level, when PNP_EN=Low.
BGR	I	When PNP_EN=High, <R><G><B> output order decision pad. BGR = High : <B><G><R> color is assigned from S1. BGR = Low : <R><G><B> color is assigned from S1. Must be connected to VSS level, when PNP_EN=Low.

Note. When used as system interface.

Table 6. RGB interface pad description (Continued)

Symbol	I/O	Description
ENABLE	I	Data enable signal of RGB interface. When ENABLE is in active state, data on RGB bus is valid. But when this is not in active state, data on RGB bus is invalid. (For details, refer to the description of EPL register) Must be connected to VDD3 or VSS level when not used.
VSYNC	I	Synchronous signal of frame. (Active Low Pad) Must be connected to VDD3 or VSS level when not used.
HSYNC	I	Synchronization signal of a horizontal line. (Active Low Pad) Must be connected to VDD3 or VSS level when not used.
DOTCLK	I	Data Clock of RGB interface. Must be connected to VDD3 or VSS level when not used.
DB[17:0] [NOTE]	I	Used as an input data bus for RGB I/F. - 6-bit interface: DB[17:12] - 16-bit interface: {DB[17:13], & DB[11:1]} - 18-bit interface: DB[17:0] Must be connected to VDD3 or VSS level when not used.

Note. When used as RGB I/F

Table 7. Display pad description

Symbol	I/O	Description
S1 – S720	O	Source driver output pads. The SS bit can change the shift direction of the source signal. For example, if SS = 0, gray data of S1 is read from RAM address 0000h. If SS = 1, contents of RAM address 0000h is out from S528. S1, S4, S7, ... S(3n-2) : display Red (R) (SS = 0) S2, S5, S8, ... S(3n-1) : display Green (G) (SS = 0) S3, S6, S9, ... S(3n) : display Blue (B) (SS = 0)
G1 – G320	O	Gate driver output pads. The output of driving circuit is whether VGH or VGL VGH : gate-ON level VGL : gate-OFF level

Table 8. Miscellaneous pad description

Symbol	I/O	Description
M	O	Output pads used only for a test purpose at IC-side. In normal operation, leave this unconnected.
FLM	O	Tearing effect output pad to synchronize MCU to frame writing, activated by S/W command. When this is not activated, this pad should be low. If not in use, leave this unconnected.
CL1	O	Output pads used only for a test purpose at IC-side. In normal operation, leave this unconnected.
EN_EXCLK	I	Enable external clock input Connect this pad to VSS level if the pad is not in use.
EXCLK	I	External clock input pad. Connect this pad to VSS level if the pad is not in use.
CONTACT	-	Contact resistance measurement pad. In normal operation, leave this unconnected. These pads are at VSS level. When measuring an ohmic resistance of the contact, do not apply any power.

Table 9. Test pad description

Symbol	I/O	Description
TEST_MODE[2:0]	I	Input pads used only for a test purpose at IC-side. In normal operation, connect this pad to VSS.

5.3. INTERFACE PAD CONFIGURATION

Table 10. Interface Pad Configuration

PAD NAME	68 System				80 System				RGB			MDDI	
	18bit	16bit	9bit	8bit	18bit	16bit	9bit	8bit	18bit	16bit	6bit	Normal	Sub-panel
IM[0]	VSS	VSS	VDD3	VDD3	VSS	VSS	VDD3	VDD3	ID *[Note1]			VDD3/VSS	VDD3/VSS
IM[1]	VSS	VSS	VSS	VSS	VDD3	VDD3	VDD3	VDD3	VSS	VSS	VSS	VSS	VSS
IM[2]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD3	VDD3	VDD3	VDD3	VDD3
IM[3]	VDD3	VSS	VDD3	VSS	VDD3	VSS	VDD3	VSS	VSS	VSS	VSS	VDD3	VDD3
VCI_MDDI	VCI	VCI	VCI	VCI	VCI	VCI	VCI	VCI	VCI	VCI	VCI	VCI	VCI
VSS_MDDI	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
MDP	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	MDP	MDP
MDN	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	MDN	MDN
MSP	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	MSP	MSP
MSN	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	MSN	MSN
DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	*[Note2]	*[Note3]
DB[12]	DB[12]	DB[12]	DB[12]	DB[12]	DB[12]	DB[12]	DB[12]	DB[12]	DB[12]	VDD3/VSS	DB[12]		
DB[11:10]	DB[11:10]	DB[11:10]	DB[11:10]	DB[11:10]	DB[11:10]	DB[11:10]	DB[11:10]	DB[11:10]	DB[11:10]	DB[11:10]	VDD3/VSS		
DB[9]	DB[9]	VDD3/VSS	DB[9]	VDD3/VSS	DB[9]	VDD3/VSS	DB[9]	VDD3/VSS	DB[9]	DB[9]	VDD3/VSS		
DB[8:1]	DB[8:1]	DB[8:1]	VDD3/VSS	VDD3/VSS	DB[8:1]	DB[8:1]	VDD3/VSS	VDD3/VSS	DB[8:1]	DB[8:1]	VDD3/VSS		
DB[0]	DB[0]	VDD3/VSS	VDD3/VSS	VDD3/VSS	DB[0]	VDD3/VSS	VDD3/VSS	VDD3/VSS	DB[0]	VDD3/VSS	VDD3/VSS		
SDI	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	SDI	SDI	SDI	VDD3/VSS	VDD3/VSS
SDO	floating	floating	floating	floating	floating	floating	floating	floating	SDO *[Note4]			floating	floating
CSB	CSB	CSB	CSB	CSB	CSB	CSB	CSB	CSB	CSB	CSB	CSB	VDD3/VSS	VDD3/VSS
RW_WRB/SCL	RW	RW	RW	RW	WRB	WRB	WRB	WRB	SCL	SCL	SCL	VDD3/VSS	VDD3/VSS
E_RDB	E	E	E	E	RDB	RDB	RDB	RDB	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
RS	RS	RS	RS	RS	RS	RS	RS	RS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
RESETB	RESETB	RESETB	RESETB	RESETB	RESETB	RESETB	RESETB	RESETB	RESETB	RESETB	RESETB	RESETB	RESETB
VSYNC	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VSYNC	VSYNC	VSYNC	VDD3/VSS	VDD3/VSS
HSYNC	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	HSYNC	HSYNC	HSYNC	VDD3/VSS	VDD3/VSS
DOTCLK	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	DOTCLK	DOTCLK	DOTCLK	VDD3/VSS	VDD3/VSS
ENABLE	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	ENABLE	ENABLE	ENABLE	VDD3/VSS	VDD3/VSS
TEST_MODE<0>	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
TEST_MODE<1>	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
TEST_MODE<2>	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
PNP_EN*[Note5]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS

Without Sub-panel		Note
PAD NAME	MDDI	
DB[17]	floating	Output
DB[16]	floating	
DB[15]	floating	
DB[14]	GPIO<5>	Input *[Note6]
DB[13]	GPIO<4>	
DB[12]	GPIO<3>	
DB[11]	GPIO<2>	
DB[10]	GPIO<1>	
DB[9]	GPIO<0>	
DB[8:1]	floating	Output *[Note7]
DB[0]	floating	

With Sub-panel		Note
PAD NAME	MDDI	
DB[17]	S_CSB	Output
DB[16]	S_RS	
DB[15]	S_WRB	
DB[14]	GPIO<5>	Input *[Note6]
DB[13]	GPIO<4>	
DB[12]	GPIO<3>	
DB[11]	GPIO<2>	
DB[10]	GPIO<1>	
DB[9]	GPIO<0>	
DB[8:1]	S_DB[8:1]	Output *[Note7]
DB[0]	S_DB[0]	

Note.

1. IM[0] = ID, Refer to Datasheet Page 106, or PAD Description.
2. Refer to Without Sub-panel Chart.
3. Refer to With Sub-panel Chart.
4. Leave this pad open when not used.
5. When PNP_EN = Low, PNP mode H/W pad must be fix at VSS level.
6. GPIO(General Purpose I/O), Must be fix at VDD3 or VSS when not used.
7. When sub panel is 9-bit I/F, DB[8:0] is used. When sub panel is 8-bit I/F, DB[8:1] is used and DB[0] must be floating.

6. Electrical Specifications

This chapter describes the DC and AC electrical specification of the IC.

6.1. Absolute Maximum Ratings

Table 11. Absolute Maximum Rating

Item	Symbol	Rating	Unit
Supply voltage for logic block	VDD - VSS	-0.3 to +3.3	V
Supply voltage for I/O block	VDD3 - VSS	-0.3 to +5.0	V
Supply voltage for step-up circuit	VCI - VSS	-0.3 to +5.0	V
LCD Supply Voltage range	AVDD – VSS	-0.3 to +6.5	V
	VGH - VSS	-0.3 to +22.0	V
	VSS – VGL	-0.3 to +22.0	V
	VSS - VCL	-0.3 to +5.0	V
	|VGH – VGL|	-0.3 to +33	V
Input Voltage range	Vin	- 0.3 to VDD3 + 0.5	V
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-55 to +110	°C

Note.

1. Absolute maximum rating is the limit value. When the IC is exposed operating environment beyond this range, the IC is not guaranteed for the normal operations and may be damaged permanently, not be able to be recovered.
2. Operating temperature means the possible range of device-operating temperature. It does not mean that the performance of the driver IC would be guaranteed over this temperature range.
3. Absolute maximum rating is guaranteed only when our company's package used.

6.2. DC Characteristics

6.2.1. Basic Characteristics

Table 12. DC Characteristics

(VSS = 0V)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Operating voltage	VDD3		1.65	-	3.3	V	*1
LCD driving voltage	VGH		11.25	-	16.50	V	*2
	VGL		-13.75	-	-6.75	V	*2
	VCL		-3	-	-2.25	V	*3
	AVDD		4.5	-	6.0	V	*3
	GVDD		2.5	-	5.0	V	
Input high voltage	V_{IH}		0.7*VDD3	-	VDD3	V	*4
Input low voltage	V_{IL}		0	-	0.3*VDD3	V	*4
Output high voltage	V_{OH}	I_{OH} = -0.5mA	0.8*VDD3	-	VDD3	V	*5
Output low voltage	V_{OL}	I_{OL} = 0.5mA	0.0	-	0.2*VDD3	V	*5
Input leakage current	I_{IL}	VIN = VSS or VDD3	-1.0		1.0	uA	*4
Output leakage current	I_{OL}	VIN = VSS or VDD3	-3.0		3.0	uA	*5
Operating frequency	Fosc	Frame freq. = 60 Hz Display line = 320	0.9*TYP	323	1.1*TYP	kHz	*6
Internal reference power supply voltage	VCI		2.5	-	3.3	V	
1st step-up input voltage	VCI1		1.35	-	3	V	
1st step-up output efficiency	η_{AVDD}	ILOAD = 4 mA	90	95	-	%	
2nd step-up output efficiency	η_{VGH}	ILOAD = 0.1 mA	90	95	-	%	
3rd step-up output efficiency	η_{VGL}	ILOAD = 0.1 mA	90	95	-	%	
4th step-up output efficiency	η_{VCL}	ILOAD = 0.3 mA	90	95	-	%	

Note.

1. VSS = 0V.
2. |VGH| & |VGL| Min : When VCI1 = 2.25V, |VGL| Max : When VCI1=2.75V, |VGH - VGL| Max : 30.0V
   cf> |VGH| max. should be lower than or equal to 16.5V in normal operating condition, regardless of VCI1 & BT settings.
3. AVDD & |VCL| Min: When VCI1 = 2.25V, AVDD & |VCL| Max: When VCI1=3.0V
4. Applied pads; CSB, E_RDB, RW_WRB, RS, DB[17:0], RESETB, HSYNC, VSYNC, DOTCLK, ENABLE, SDI, EXCLK
5. Applied pads; DB[17:0], M, FLM, CL1, SDO
6. Target frame frequency : 60 Hz, Display line = 320, Back porch = 8, Front porch = 8, RTN2-0 = “000”
   cf> Fosc can be observed indirectly by measuring CL1 pad.(fosc / 16)

Table 13. DC Characteristics For LCD Driver Outputs

(VDD = 1.5V, VDD3 = 3.0V, VSS = 0V)

Characteristic	Symbol	Condition	MIN	TYP	MAX	Unit	Note
LCD Gate Driver Output "On" Resistance	Ronvgh	I(sink)=100uA	-	-	3	kΩ	-
	Ronvgl	I(source)=100uA	-	-	3	kΩ	-
LCD Source Driver Output "On" Resistance	Ronp	I(sink)=100uA	-	-	20	kΩ	-
	Ronn	I(source)=100uA	-	-	20	kΩ	-
LCD Binary Driver Output "On" Resistance	Ronpb	I(sink)=100uA	-	-	300	kΩ	-
	Ronnb	I(source)=100uA	-	-	300	kΩ	-
Output Voltage Deviation (Mean Value)	ΔV_O	$4.2V \leq V_{SO}$	-	-	±55	mV	*1
		$0.8V < V_{SO} < 4.2V$	-	-	±25	mV	*1
		$V_{SO} \leq 0.8V$	-	-	±55	mV	*1
LCD Source Driver Delay	tSD	AVDD = 5.0V GVDD = 4.5V SAP = "0100"	-	-	20.9	us	*2
Current Consumption during Normal Operation	IVDD3	No load, Ta = 25 °C, VDD3=VCI=3V Frame(f)=60Hz	-	-	150	uA	-
	IVCI		-	-	8	mA	-
Current Consumption during Standby Mode	Istby_VDD3	VDD3= VCI = 3.0V Ta = 25°C	-	-	25.0	uA	*3
	Istby_VCI		-	-	5.0	uA	
Current Consumption during Deep Standby Mode	Idstby_VDD3	VDD3= VCI = 3.0V Ta = 25°C	-	-	5.0	uA	*3
	Idstby_VCI		-	-	5.0	uA	

Note.

1. VSO the output voltage of analog output pins S1 to S720
2. tSD : LCD Source driver delay
3. Target frame frequency = 60 Hz, Display line = 320, Back porch = 8, Front porch = 8, RTN3-0 = "0000" VC3-0 = "1011", DC11/DC10/DC21/DC20/DC31/DC30 = "000000", BT2-0 = "000", GVD5-0 = "111111" VCM5-0 = "111111", VML5-0 = "111111"

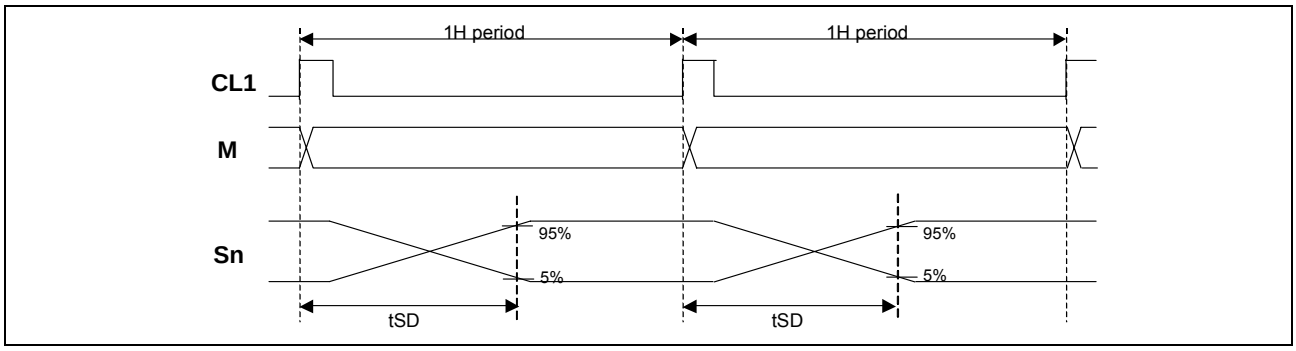


Figure 7. LCD source driver delay

6.3. AC characteristics

Table 14. Parallel Write Interface Characteristics (68 Mode)

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, TA = -40 to +85 °C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	tCYCW68	100	-	ns
	Read	tCYCR68	500	-	
Pulse rise / fall time		tR, tF	-	15	
Pulse width low	Write	tWLW68	33	-	
	Read	tWLR68	250	-	
Pulse width high	Write	tWHW68	33	-	
	Read	tWHR68	250	-	
RS,RW to CSB, E setup time		tAS68	10	-	
RS,RW to CSB, E hold time		tAH68	2	-	
CSB to E time		tCW68	15	-	
Write data setup time		tWDS68	60	-	
Write data hold time		tWDH68	15	-	
Read data delay time		tRDD68	-	200	
Read data hold time		tRDH68	5	-	

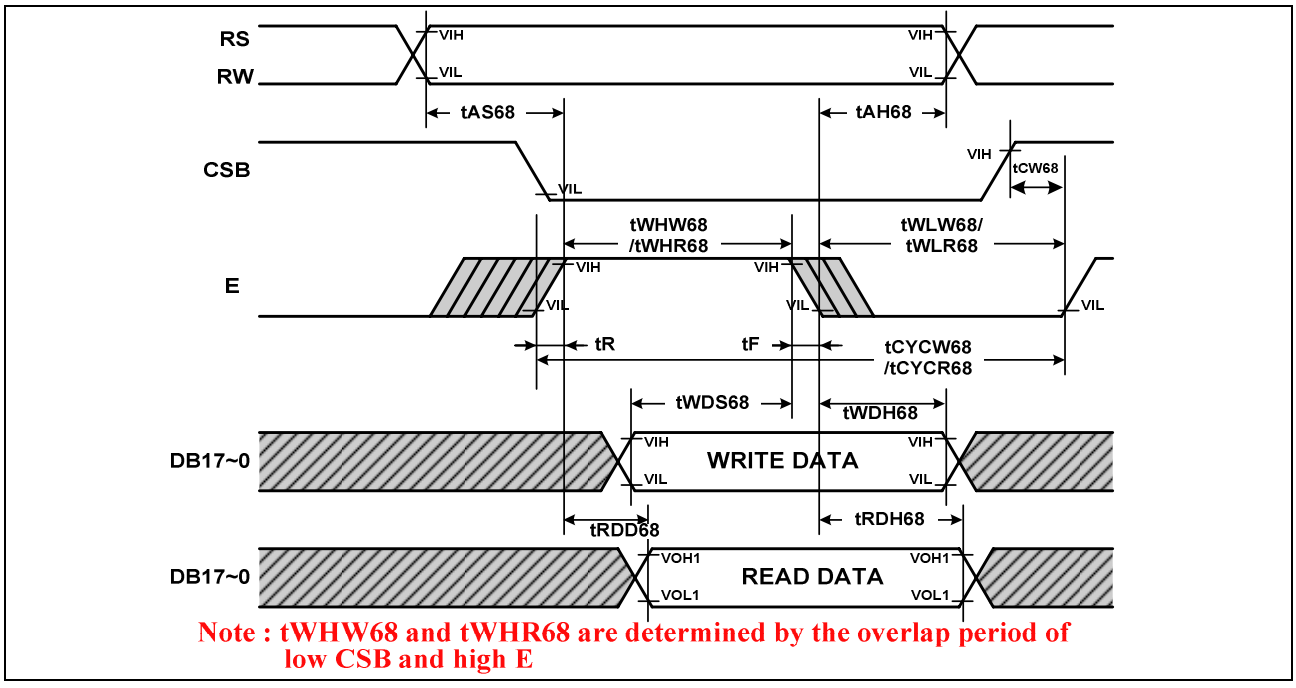


Figure 8. AC Characteristics (68 Mode)

Table 15. Parallel Write Interface Characteristics (80 Mode)

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, TA = -40 to +85 °C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	tCYCW80	100	-	ns
	Read	tCYCR80	500	-	
Pulse rise / fall time		tR, tF	-	15	
Pulse width low	Write	tWLW80	33	-	
	Read	tWLR80	250	-	
Pulse width high	Write	tWHW80	33	-	
	Read	tWHR80	250	-	
RS to CSB, WRB(RDB) setup time		tAS80	10	-	
RS to CSB, WRB(RDB) hold time		tAH80	2	-	
CSB to WRB(RDB) time		tCW80	15	-	
Write data setup time		tWDS80	20	-	
Write data hold time		tWDH80	10	-	
Read data delay time		tRDD80	-	200	
Read data hold time		tRDH80	10	-	

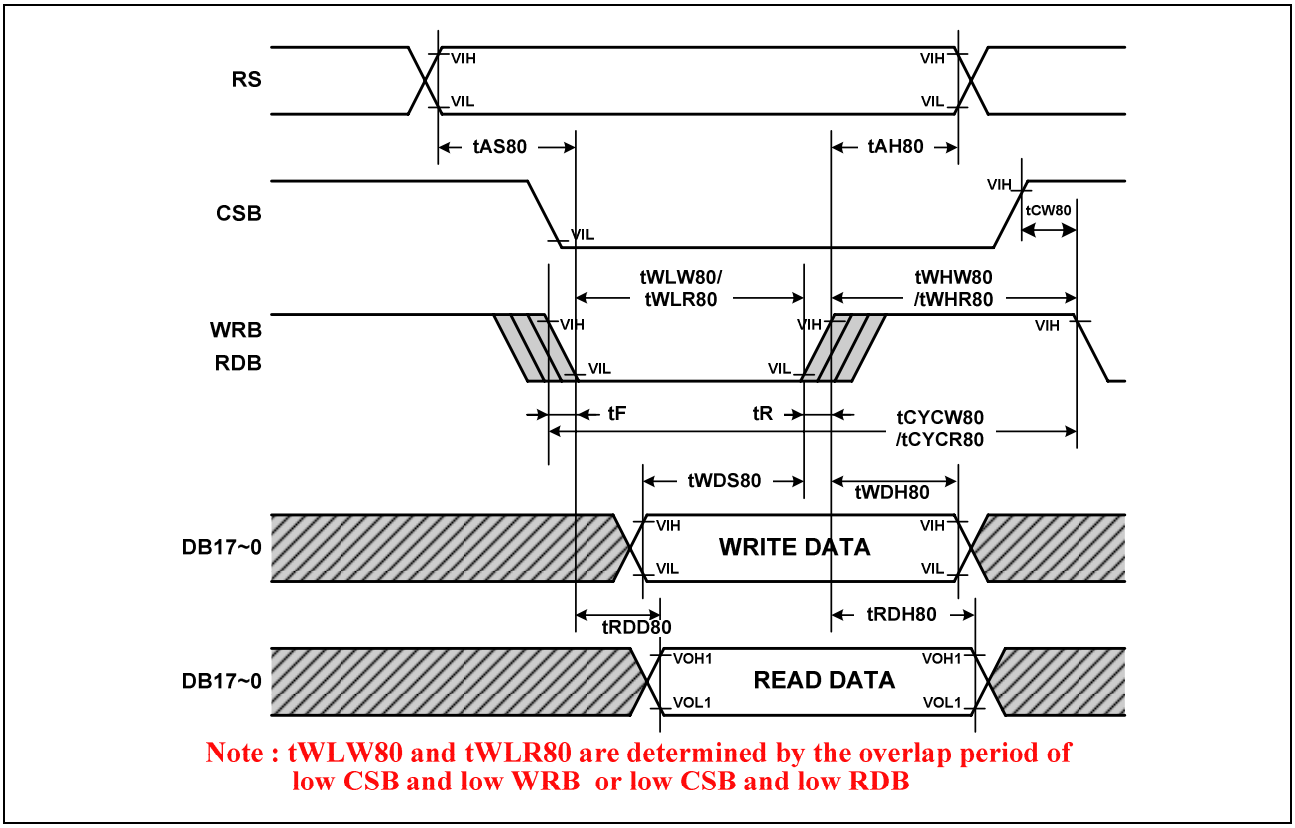


Figure 9. AC Characteristics (80 Mode)

Table 16. Clock Synchronized Serial Write Mode Characteristics

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, TA = -40 to +85 °C)

Characteristic	Symbol	specification		Unit
		Min.	Max.	
Serial clock write cycle time	tscyc	130	-	ns
Serial clock read cycle time	tscyc	250	-	ns
Serial clock rise / fall time	tR, tF	-	15	ns
Pulse width high for write	tSCHW	50	-	ns
Pulse width high for read	tSCHR	110	-	ns
Pulse width low for write	tSCLW	50	-	ns
Pulse width low for read	tSCLR	110	-	ns
Chip Select setup time	tCSS	20	-	ns
Chip Select hold time	tCSH	60	-	ns
Serial input data setup time	tSIDS	30	-	ns
Serial input data hold time	tSIDH	30	-	ns
Serial output data delay time	tSODD	-	130	ns
Serial output data hold time	tSODH	5	-	ns

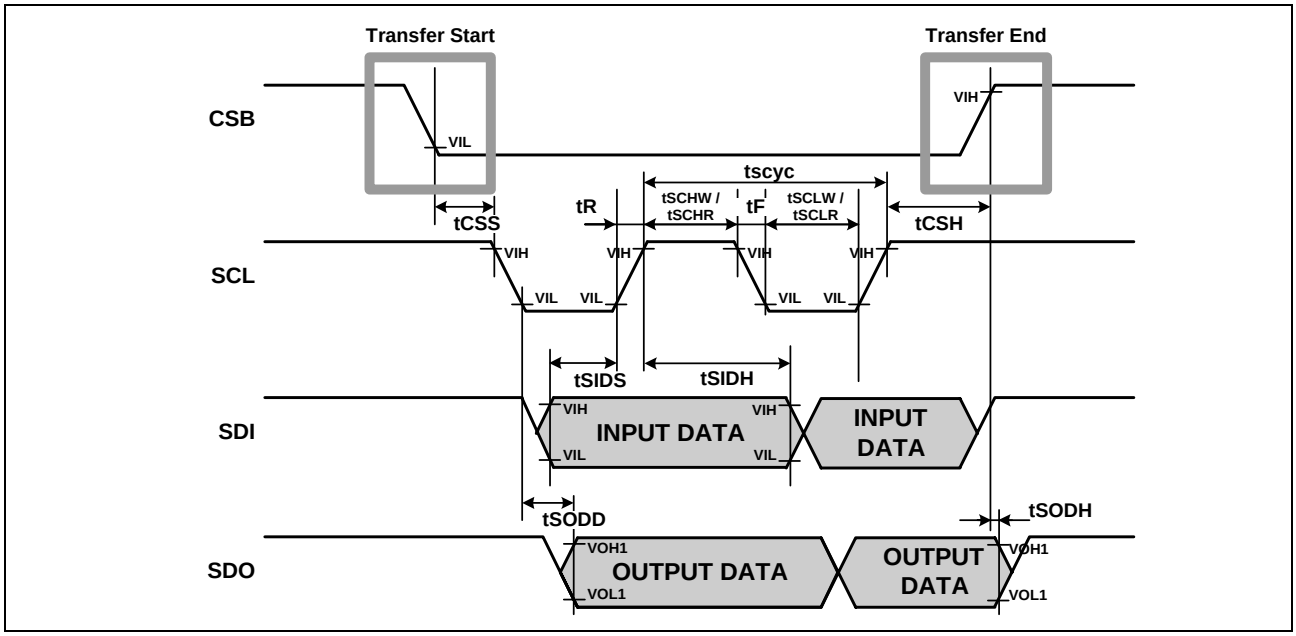
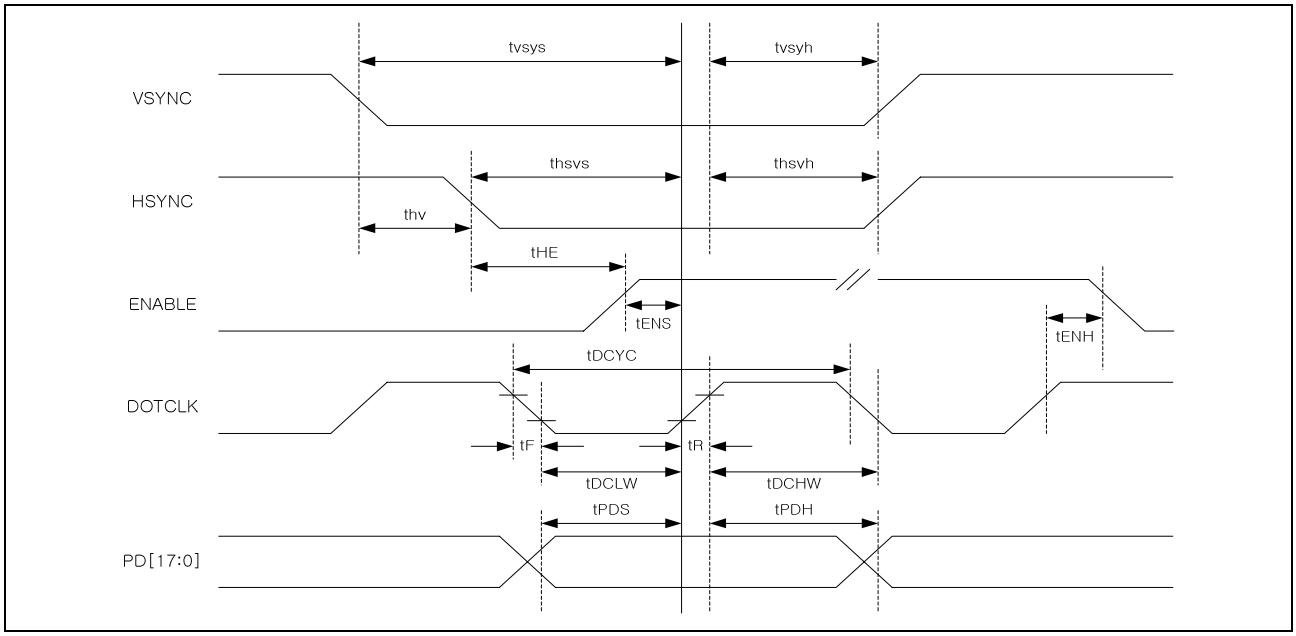


Figure 10. AC Characteristics (SPI Mode)

Table 17. RGB Data Interface Characteristics

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, TA = -40 to +85 °C)

Characteristic	Symbol	18/16bit RGB interface		6bit RGB interface		Unit
		Min.	Max.	Min.	Max.	
DOTCLK cycle time	tDCYC	100	-	100	-	ns
DOTCLK rise / fall time	tR, tF	-	15	-	15	
DOTCLK Pulse width high	tDCHW	40	-	40	-	
DOTCLK Pulse width low	tDCLW	40	-	40	-	
Vertical Sync Setup Time	tvsys	30	-	30	-	
Vertical Sync Hold Time	tvsyh	30	-	30	-	
Horizontal Sync Setup Time	thsys	30		30		
Horizontal Sync Hold Time	thsyh	30		30		
ENABLE setup time	tENS	30	-	30	-	
ENABLE hold time	tENH	20	-	20	-	
PD data setup time	tPDS	30	-	30	-	
PD data hold time	tPDH	20	-	20	-	
HSYNC-ENABLE Time	tHE	1	255	1	255	tDCYC
VSYNC-HSYNC Time	thv	1	239	1	719	



(When VSPL=0, HSPL=0, DPL=0, EPL=1)

Figure 11. Figure 90 : AC Characteristics (RGB Interface Mode)

Note. When RGB interface mode, PD [17:0] corresponds to DB [17:0]

6.4. Reset Input Timing

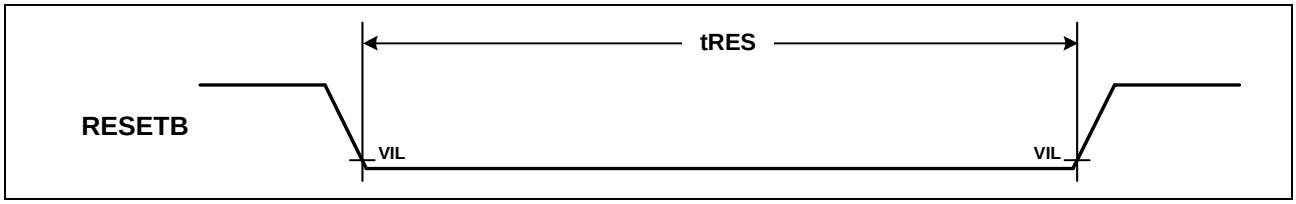


Figure 12. AC characteristics (RESET timing)

Note. Reset low pulse width shorter than 10us do not make reset. It means undesired short pulse such as glitch, bouncing noise or electrostatic discharge do not cause irregular system reset. Please refer to the table below.

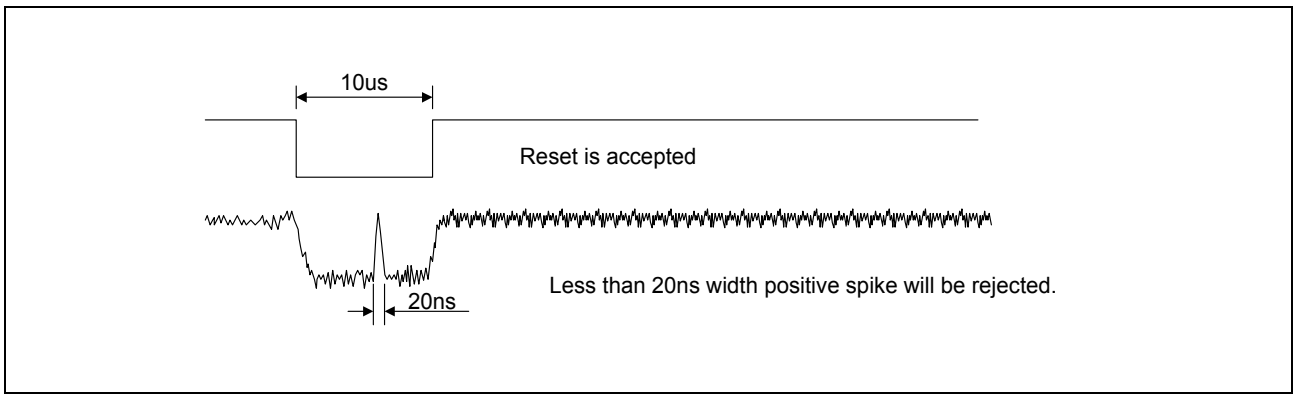
Parameter	Description	Min	Max	Unit
tRES	Reset low pulse width	10	-	us

Table 18. Reset Operation regarding tRES Pulse Width

tRES Pulse	Action
Shorter than 5 us	No reset
Longer than 10 us	Reset
Between 5 us and 10 us	Not determined

1. User may or may not use RESETB pin. In order to use it, user should satisfy the conditions described in the above tables. But when not wants to use RESETB, user may fix this pin to VDD3 level because internally generated POR (Power-On-Reset) is used.

2. Spike Rejection also applies during a valid reset pulse as shown below:



6.5. MDDI IO DC/AC CHARACTERISTICS

Table 19. Data/Strobe Rx DC Characteristics

Parameter	Description	MIN	TYP	MAX	Unit	Note
V_{IT+}	Receiver differential input high threshold voltage. Above this differential voltage the input signal shall be interpreted as a logic-one level.			50	mV	
V_{IT-}	Receiver differential input low threshold voltage. Below this differential voltage the input signal shall be interpreted as a logic-zero level.	-50			mV	
V_{IT+}	Receiver differential input high threshold voltage (offset for hibernation wake-up). Above this differential voltage the input signal shall be interpreted as a logic-one level.		125	175	mV	
V_{IT-}	Receiver differential input low threshold voltage (offset for hibernation wake-up). Below this differential voltage the input signal shall be interpreted as logic-zero level.	75	125		mV	
$V_{Input-Range}$	Allowable receiver input voltage range with respect to client ground.	0		1.65	V	
R_{term}	Parallel termination resistance value	98	100	102	Ω	

Table 20. Driver Electrical DC Characteristics

Parameter	Description	MIN	TYP	MAX	Unit	Note
$I_{diffabs}$	Absolute driver differential output current range (Currnt through the termination resistor)	2.5		4.5	mA	R_{term}= 100 Ω
$V_{out-rng-int}$	Single-ended driver output voltage range with respect to ground, internal mode	0.35		1.60	V	Under all conditions, including double-drive

Note. Please refer to VESA specification Ver 1.0

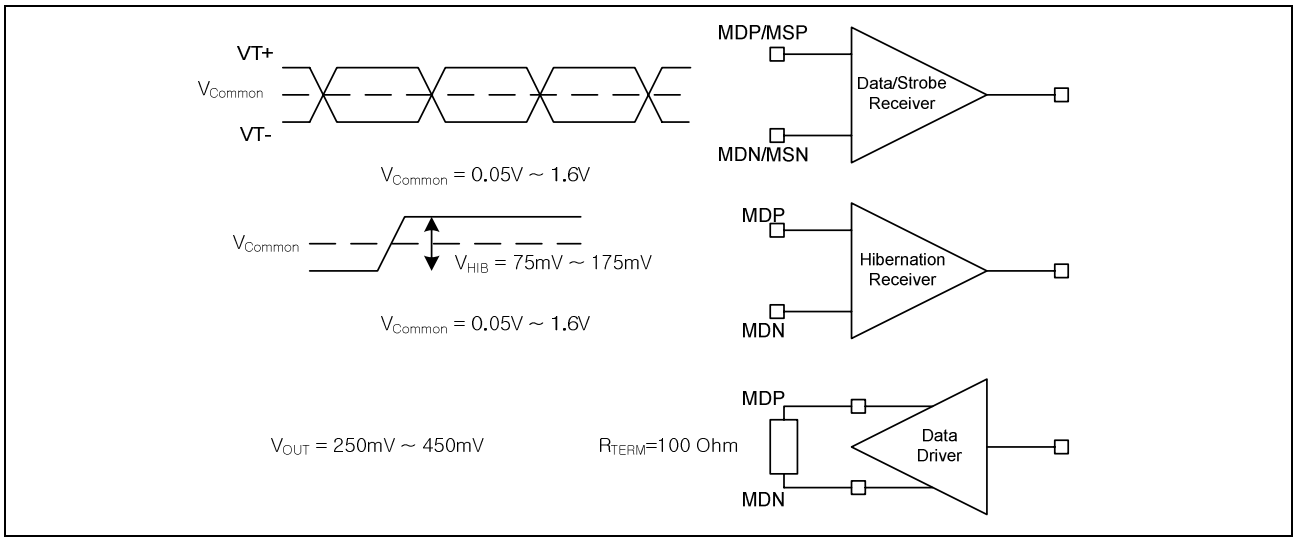


Figure 13. MDDI Receiver, Driver Electrical Diagram

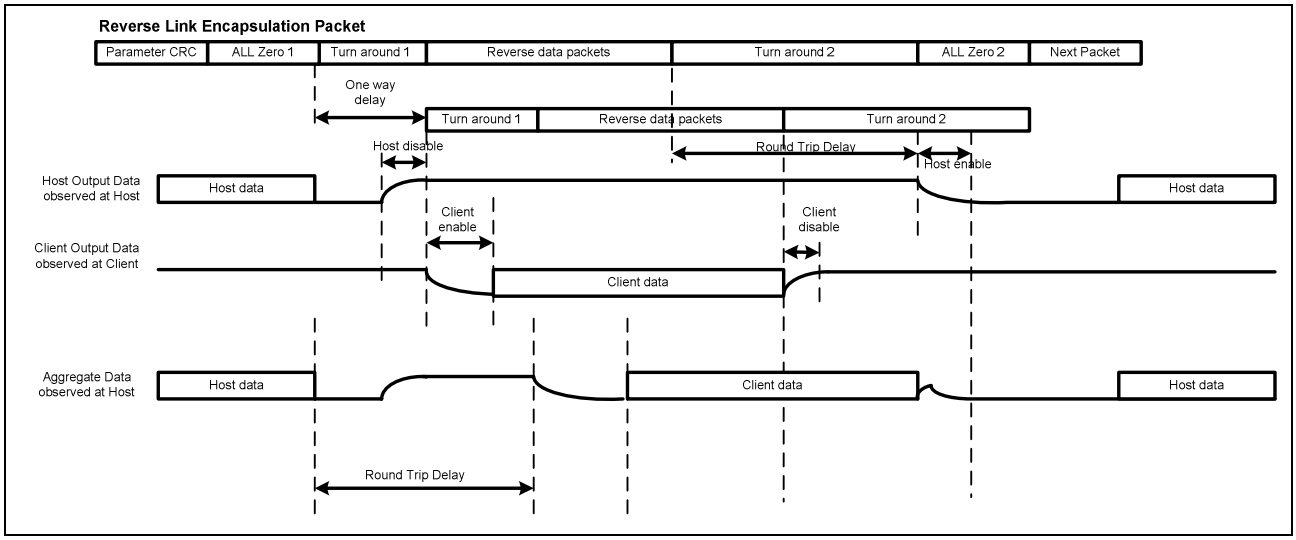


Figure 14. Host enable/disable time and Client enable/disable time diagram

Table 21. Receiver AC Characteristics

Parameter	Description	MIN	TYP	MAX	Unit
t_{BIT}	Forward link data bit rate	0		8	ns
$T_{host\text{-}enable}$	Host output enable time	0		$24*t_{BIT}$	ns
$T_{host\text{-}disable}$	Host output disable time, entire length of the Turn-Around 1 field	0		$24*t_{BIT}$	ns
$T_{client\text{-}enable}$	Client output enable time, entire length of the Turn-Around 1 field	0		$24*t_{BIT}$	ns
$T_{client\text{-}disable}$	Client output disable time, measured from the end of the last bit of the Turn-Around 2 field	0		$24*t_{BIT}$	ns

Note.

1. t_{BIT}= 1 / Link_Data_Rate, where Link_Data_Rate is the bit rate of a single data pair
   (For example, if the average forward link bit rate is 125Mbps, then t_{BIT}= 1 / 125Mbps = 8ns)
2. These specifications are from VESA specification Ver 1.0.

6.6. External Power On/Off Sequence

6.6.1. External Power On Sequence

VDD3 must be applied earlier than VCI or at least applied simultaneously with VCI. When regulator cap is 1uF, RESETB must be applied after VCI have been applied. The applied time gap between VCI and RESETB is minimum 1ms. As regulator cap becomes larger, this time gap must be increased. Otherwise function is not guaranteed.

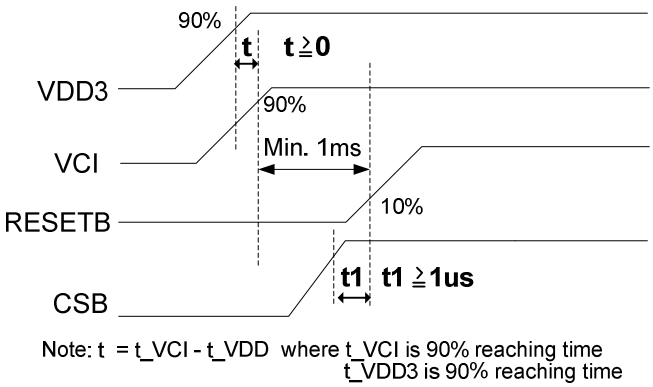


Figure 15. External power on sequence

6.6.2. External Power Off Sequence

VDD3 must be powered down later than VCI or at least powered down simultaneously with VCI. VCI must be powered down after RESETB have been powered down. The time gap of powered down between RESETB and VCI is minimum 1ms. Otherwise function is not guaranteed.

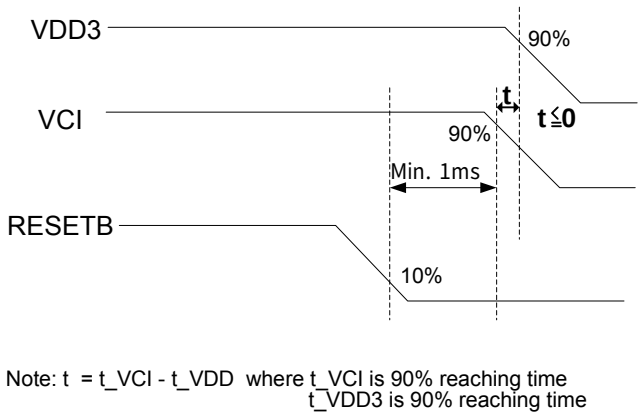


Figure 16. External power off sequence

7. FUNCTIONAL DESCRIPTION

7.1. SYSTEM INTERFACE

The IC has nine high-speed system interfaces: a 80-Series 18-/16-/9-/8-bit bus, a 68-Series 18-/16-/9-/8-bit and SPI(Serial Peripheral Interface).

The IC has three 18-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR stores index information for control register and GRAM. WDR temporarily stores data to be written into control register and GRAM. RDR temporarily stores data read from GRAM. Data written into the GRAM from MPU is initially written to WDR and then written to the GRAM automatically. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are valid.

Execution time for instruction, except oscillation start, is 0-clock cycle so that instructions can be written in succession.

Table 22. Register Selection (18-/16-/9-/8- Parallel Interface)

SYSTEM	RW_WRB	E_RDB	RS	Operations
68	0	1	0	Write index to IR
	1	1	0	Read internal status
	0	1	1	Write to control register and GRAM through WDR
	1	1	1	Read from GRAM through RDR
80	0	1	0	Write index to IR
	1	0	0	Read internal status
	0	1	1	Write to control register and GRAM through WDR
	1	0	1	Read from GRAM through RDR

Table 23. CSB signal (GRAM update control)

CSB	Operation
0	Data is written to GRAM, GRAM address is updated
1	Data is not written to GRAM, GRAM address is not updated

Table 24. Register Selection (Serial Peripheral Interface)

R/W bit	RS bit	Operation
0	0	Write index to IR
1	0	Read internal status
0	1	Write data to control register and GRAM through WDR
1	1	Read data from GRAM through RDR

7.2. RGB INTERFACE

The IC has RGB interface for the reproduction of motion picture display. When the RGB interface is used, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for the display operation. The data for display (DB [17:0]) can be written according to the values of ENABLE and DOTCLK. This allows a flicker-free update of screen.

7.3. HIGH SPEED SERIAL INTERFACE (MDDI)

For the detailed information, see the section “Introduction to MDDI”

7.4. GRAPHICS RAM

The graphics RAM (GRAM) has 18-bits/pixel and stores the bit-pattern data of 240-RGB x 320 pixels.

The IC has an address counter for GRAM access. The address counter (AC) assigns addresses to the GRAM. When an address set instruction is performed, the address from system interface is sent to this AC. After writing into GRAM, AC is automatically increased (or decremented) by 1. When read data from GRAM, AC is not updated. Window Address Function allows data to be written only into the Window specified by designated control registers.

7.5. PANEL INTERFACE CONTROLLER

The Panel Interface Controller generates timing signals for TFT-LCD Driver and control signals for the operation of internal circuits such as source driver array and GRAM. GRAM read operations done by this Panel Interface Controller and GRAM write operations done through system interface are performed independently to avoid the interference between them.

7.6. GRAYSCALE VOLTAGE GENERATOR

The grayscale voltage circuit block generates a certain voltage level that is specified by the grayscale -adjusting resistor for LCD driver circuit. By use of the generator, 262,144 colors can be displayed. For details, see the ϒ-adjusting resistor section.

7.7. OSCILLATION CIRCUIT (OSC)

The IC can provide R-C oscillator without an external resistor. The appropriate oscillation frequency for controlling operating voltage, display size, and frame frequency, can be obtained by adjusting the register setting value[R0Fh]. Clock pulse can also be supplied externally. Since R-C oscillator is suspended during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

7.8. SOURCE DRIVER ARRAY

The liquid crystal display source driver array consists of 720 drivers (S1 to S720).
Display pattern data is latched when 720-bit data is ready. Then the latched data enables the source drivers to output the expected voltage level. The SS bit can change the shift direction of 720-bit data by selecting an appropriate direction for the panel configuration.

7.9. GATE DRIVER ARRAY

The liquid crystal display gate driver array consists of 220 gate drivers (G1 to G320).
The VGH or VGL level is controlled by the signal from the gate control circuit. G1 and G320 are IC test pads for itself.

7.10. GRAM ADDRESS MAP

The image data stored in GRAM corresponds to real pixel on display as shown below.

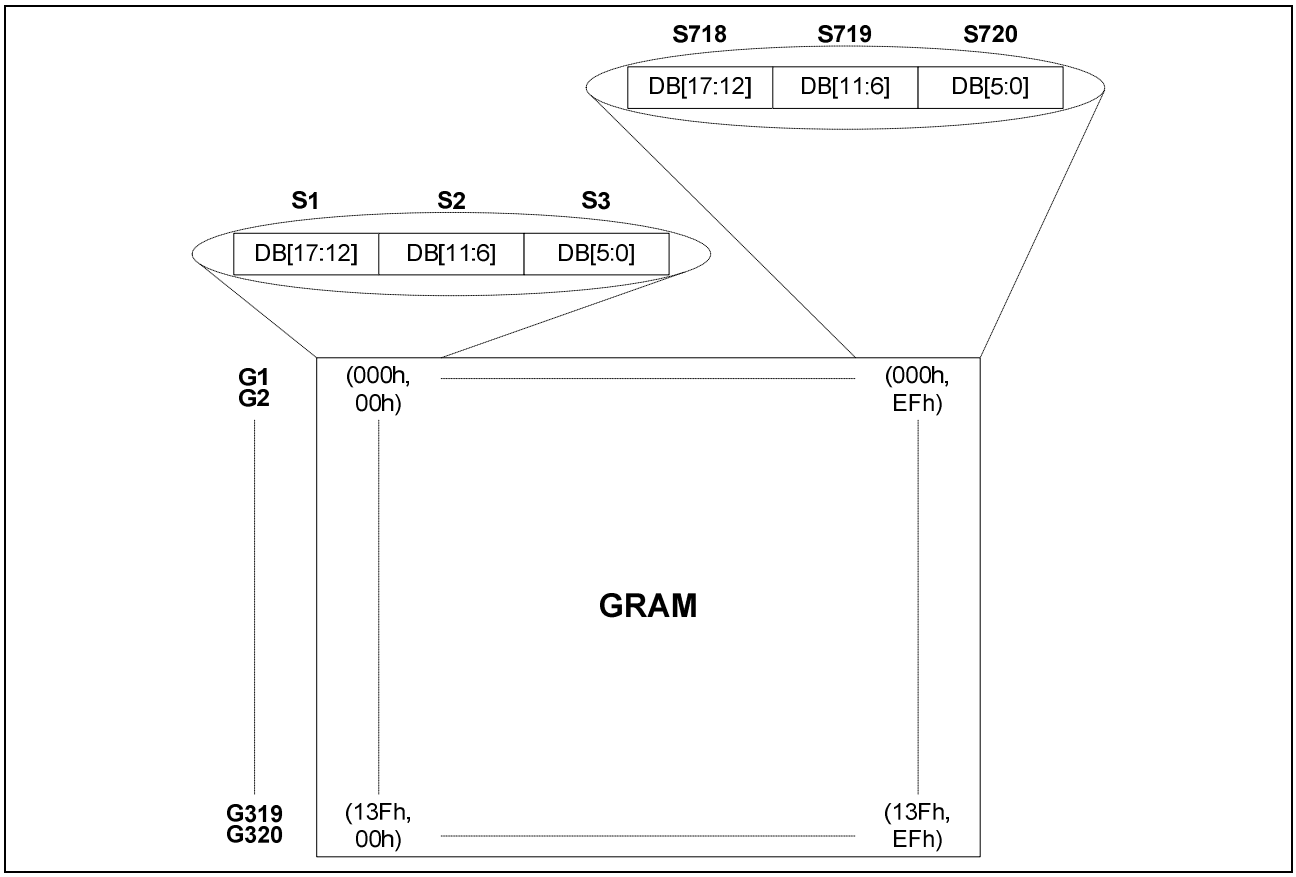


Figure 17. GRAM Address and Display Image

Note. The display condition of this figure is like this. SS = 0, BGR = 0, GS = 0.

8. PLUG & PLAY FUNCTION SPECIFICATION

When PNP_EN=High, the IC enters the Plug & Play Mode. During this mode, IC follows the internal power up/down flow. Table 24 shows AC Timing characteristics and Figure 16 shows horizontal/vertical/pixel clock timings.

8.1. AC TIMING REQUIREMENTS

Table 25. Plug & Play Function AC Charteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Vertical Sync Frequency (Refresh)	fv		60		Hz
Horizontal Sync Frequency (Line)	f_H		19.56		KHz
DOTCLK Frequency	f_{DOTCLK}		5.48	10.0	MHz
DOTCLK period	t_{DOTCLK}		183		nSec
Hsync pulse width low	t_{HSW}	-	10	-	t_{DOTCLK}
Horizontal Back Porch	t_{HBP}	-	20	-	t_{DOTCLK}
Horizontal Front Porch	t_{HFP}	-	10	-	t_{DOTCLK}
Horizontal Data Start Point	t_{HSW} + t_{HBP}	-	30	-	t_{DOTCLK}
Horizontal Blanking Period	t_{HSW} + t_{HBP} + t_{HFP}	-	40	-	t_{DOTCLK}
Horizontal Display Area	HDISP	-	240	-	t_{DOTCLK}
Horizontal Cycle	H_{cycle}	-	280	-	t_{DOTCLK}
Vsync pulse width low	t_{VSW}	-	2	-	Line
Vsync Back Porch	t_{VBP}	-	2	-	Line
Vsync Front Porch	t_{VFP}	-	2	-	Line
Vertical Data Start Point	t_{VSW} + t_{VBP}	-	4	-	Line
Vertical Blanking Period	t_{VSW} + t_{VBP} + t_{VFP}	-	6	-	Line
Vertical Display Area	VDISP	-	320	-	Line
Vertical Cycle	V_{cycle}	-	326	-	Line
Vertical Sync Setup Time	Tvsys	20			nSec
Vertical Sync Hold Time	Tvsyh	20			nSec
Horizontal Sync Setup Time	Thsys	20			nSec
Horizontal Sync Hold Time	Thsyh	20			nSec
Phase difference of Sync signal Falling Edge	Thv	1		239	t_{DOTCLK}
DOTCLK Low Period	tCKL		75		nSec
DOTCLK High Period	tCKH		75		nSec
Data Setup Time	tds	20			nSec
Data Hold Time	tdh	20			nSec

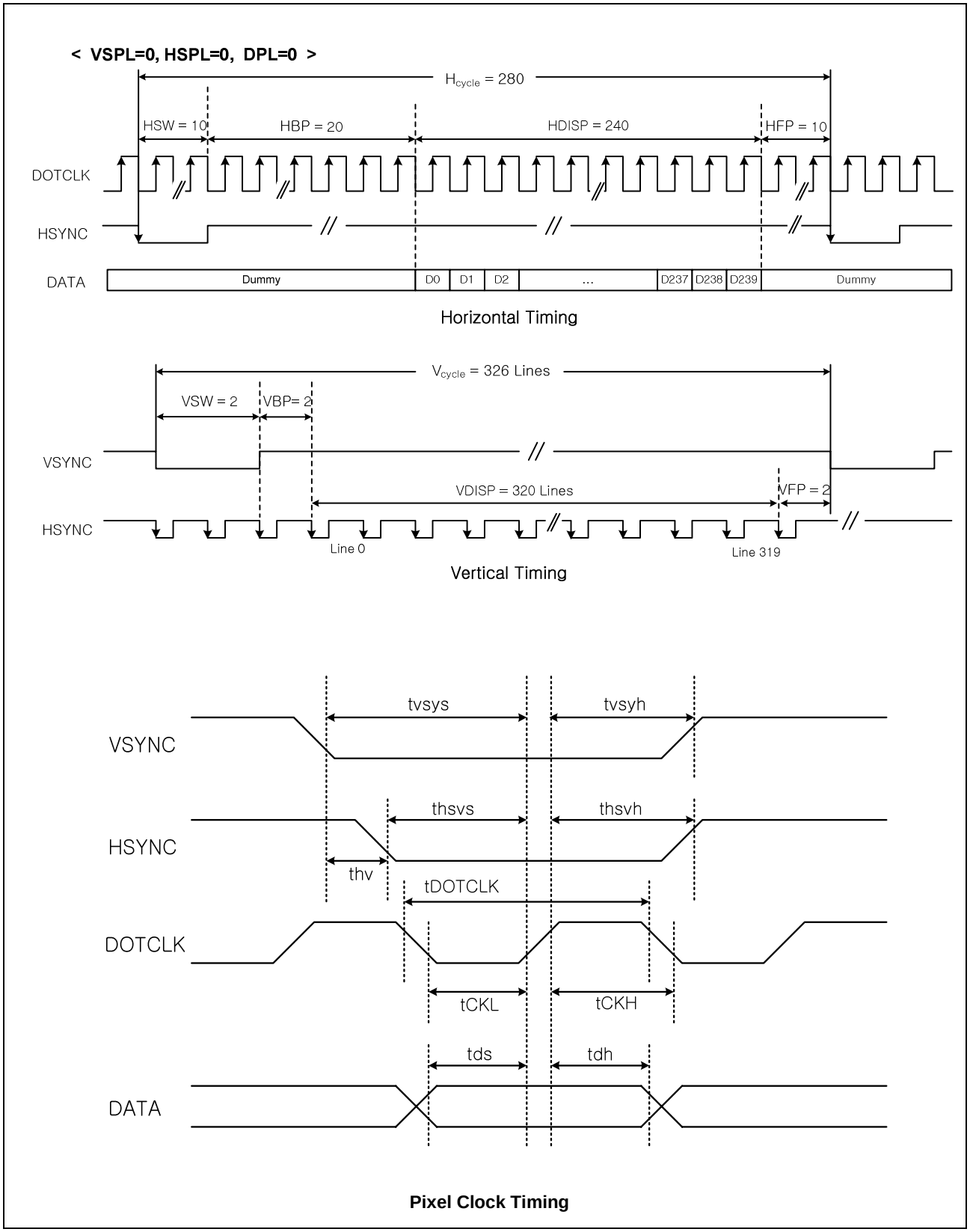


Figure 18. Plug & Play Timing Diagram

8.2. POWER- UP SEQUENCE

The power-up sequence is controlled by VDD3, VCI, SD, DOTCLK, HSYNC and VSYNC as shown in Figure 19.

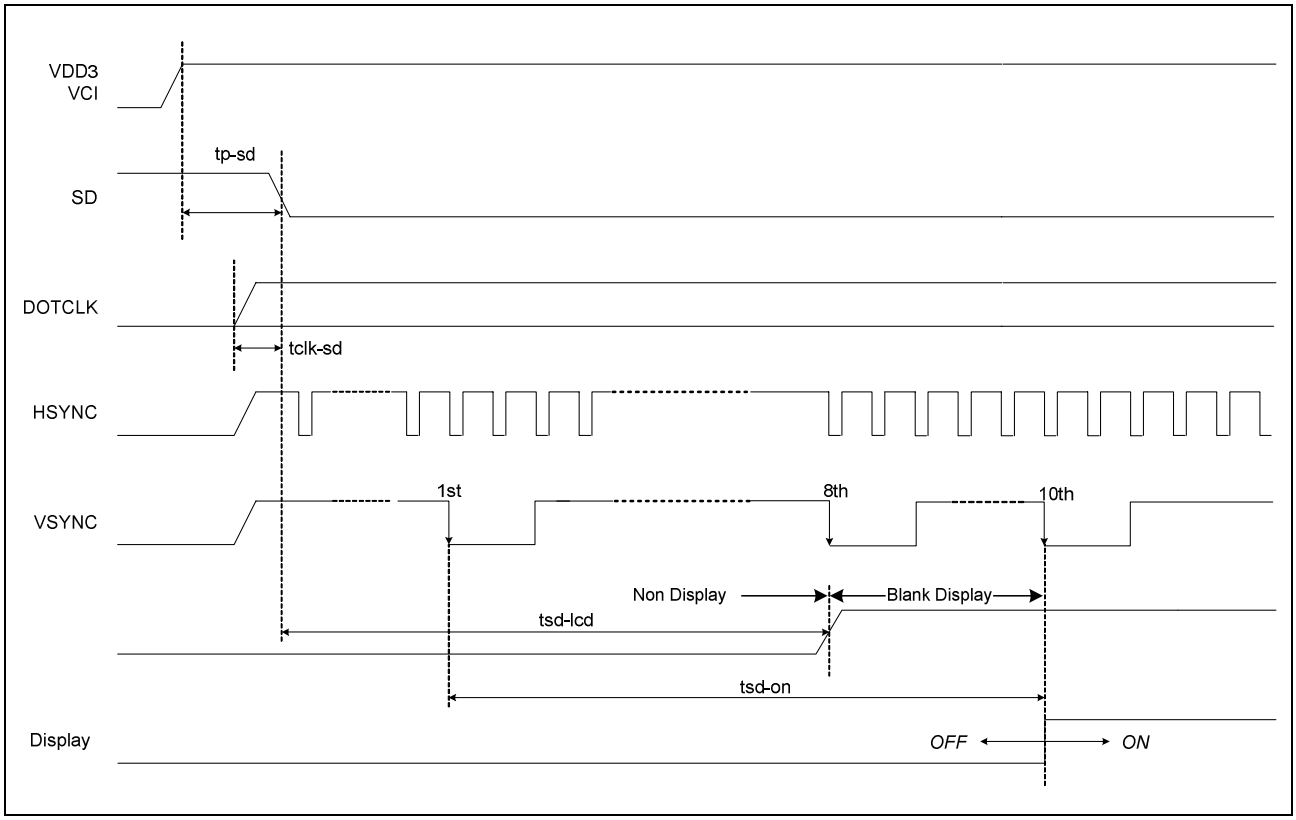


Figure 19. Power Up Sequence Timing Diagram

Table 26. Power Up AC Charateristics

Characteristics	Symbol	Min	Typ	Max	Unit
VDD/VCI on to falling edge of SD	tp-sd	1	-	-	μsec
DOTCLK input to the falling edge of SD	tclk-sd	1	-	-	μsec
Falling edge of SD to LCD power on	tsd-lcd	-	-	128	msec
Falling edge of SD to display start 1H=280t_{DOTCLK}, 1frame=326H, DOTCLK=5.48MHz	tsd-on	-	166	-	msec
		-	10	-	frame

Note. It is necessary to provide DOTCLK before the falling edge of SD.

Display will be on at 10th falling edge of VSYNC after the falling edge of SD.

8.3. POWER DOWN SEQUENCE

The power-down (and display off) sequence controlled by VDD3, VCI, SD, DOTCLK, HSYNC and VSYNC as shown in Figure 20.

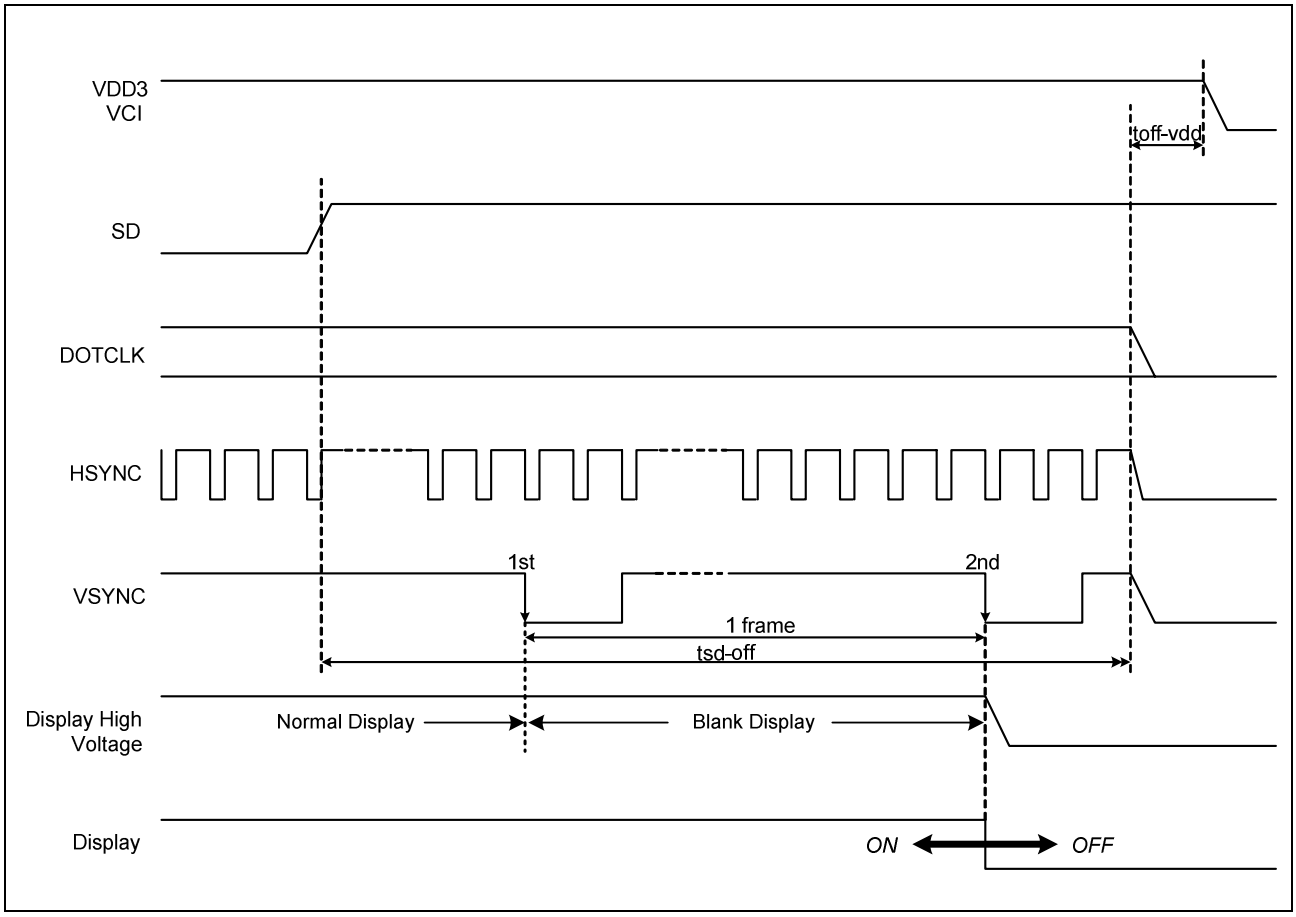


Figure 20. Power Down Sequence Timing Diagram

Table 27. Power Down AC Charateristics

Characteristics	Symbol	Min	Typ	Max	Unit
Rising edge of SD to display off 1H=280t_{DOTCLK}, 1frame=326H, DOTCLK=5.48MHz	tsd-off	33.4	-	-	msec
		2	-	-	frame
Input-signal-off to VDD/VCI off	toff-vdd	1	-	-	μsec

Note. Display will be off at the 2nd falling edge of VSYNC after the rising edge of SD.

9. Instruction Sets

9.1. Introduction

The IC uses 18-bit bus architecture. To execute an instruction to the IC, the control information from the external 18/16/9/8-bit data is stored in Index Register (IR) and Control Register (CR) as described later.

The internal operation of the IC is determined by the set of data sent from MCU. These data, which consists of the register selection signal (RS), the write/read signals (E/RWB for 68-Series, WRB/RDB for 80-Series), and the internal 16-bit data bus signals (IB15 to IB0), generate instructions.

There are eight categories of instructions that

- Specifies the index
- Reads the status
- Controls the display
- Controls power management
- Processes the graphics data
- Sets internal GRAM addresses
- Transfers data to and from the internal GRAM
- Sets grayscale level for the internal grayscale palette table

Normally, instructions writing data are used the most frequently. So, the automatic update of internal GRAM address after each data write can lighten the microcomputer’s load. Because instructions are executed in 0 cycles, they can be written in succession.

The 16-bit instruction assignment varies with interface mode specified by IM. And the assignment for each interface mode is shown in SYSTEM INTERFACE section described later.

9.2. Instruction Set

Table 28. Instruction set I

Reg.No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	Register Name / Description
IR	W	0	X	X	X	X	X	X	X	X	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	**Index /** Sets the index register value
SR	R	0	X	X	X	X	X	X	X	L8	L7	L6	L5	L4	L3	L2	L1	L0	**Status read /** Reads the internal status of the S6D0154
R00h	R	1	VER7	VER6	VER5	VER4	VER3	VER2	VER1	VER0	VER27	VER26	VER25	VER24	VER23	VER22	VER21	VER20	**Version Management (R00H)/** VER7-0: Product Name VER27-0: Product Version
R01h	W	1	VSPL (0)	HSPL (0)	DPL (0)	EPL (0)	0	SM (0)	GS (0)	SS (0)	0	0	NL5 (1)	NL4 (0)	NL3 (1)	NL2 (0)	NL1 (0)	NL0 (0)	**Driver output control(R01H) /** VSPL: set polarity of VSYNC pad. HSPL: set polarity of HSYNC pad. DPL: set polarity of DOTCLK pad. EPL: set polarity of ENABLE pad. SM: gate driver division drive control GS: gate driver shift direction SS: source driver shift direction. NL4-0: number of driving lines.
R02h	W	1	0	0	0	0	0	0	INV1 (0)	INV0 (1)	0	0	0	0	0	0	0	FLD (0)	**LCD-Driving-waveform control (R02H)/** INV1-0 : Line/Frame inversion setting FLD : Interlace Mode Control
R03h	W	1	0	0	0	BGR (0)	0	0	MDT1 (0)	MDT0 (0)	0	0	ID1 (1)	ID0 (1)	AM (0)	0	0	0	**Entry mode(R03H) /** BGR: RGB swap control MDT1-0: Multiple Data Transfer ID1-0: address counter Increment / Decrement control AM: horizontal / vertical RAM update
R07h	W	1	0	0	0	FLM _MON (0)	0	0	0	0	0	0	0	GON (0)	CL (0)	REV (0)	D1 (0)	D0 (0)	**Display control (R07H) /** FLM_MON : Enable Frame Flag Output(FLM) GON: gate on/off control CL: 8-color display mode enable REV: display area inversion drive D1-0: source output control
R08h	W	1	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)	**Blank period control 1 (R08H)/** FP3-0: Front porch setting BP3-0: Back porch setting
R0Bh	W	1	NO3 (0)	NO2 (0)	NO1 (0)	NO0 (1)	SDT3 (0)	SDT2 (0)	SDT1 (0)	SDT0 (1)	0	0	0	0	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)	**Frame cycle control (R0BH)/** NO3-0: specify the amount of non-overlap SDT3-0: set amount of source delay RTN3-0: set the 1-H period
R0Ch	W	1	0	0	0	0	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)	**External interface control(R0CH) /** RM: specify the interface for RAM access DM1-0: specify display operation mode RIM1-0: specify RGB-I/F mode
R0Fh	W	1	0	0	0	FOSC4 (0)	FOSC3 (0)	FOSC2 (1)	FOSC1 (0)	FOSC0 (1)	0	0	0	0	0	0	0	OSC ON (1)	**Start oscillation(R0FH) /** FOSC4-0:Adjust frequency of oscillator OSCON : oscillator ON
R10h	W	1	0	0	0	0	SAP3 (0)	SAP2 (0)	SAP1 (1)	SAP0 (0)	0	0	0	0	0	0	DSTB (0)	STB (0)	**Power control 1 (R10H) /** SAP3-0:adjust amount of current for source driver amp DSTB: deep standby mode control STB: standby mode control
R11h	W	1	0	0	0	APON (0)	PON3 (0)	PON2 (0)	PON1 (0)	PON (0)	0	AB _VCI1 (0)	AON (0)	VCI1_E N (0)	VC3 (0)	VC2 (0)	VC1 (0)	VC0 (0)	**Power control 2 (R12H)/** APON: auto power on control PON3 : VCL booster control PON2 : VGL booster control PON1: VGH booster circuit control AB_VCI1: Set VCI1 output equal to VCI PON: AVDD booster circuit control AON: operation start bit for the amplifier. VCI1_EN: VCI1 amplifier control VC3-0:set VCI1 voltage
R12h	W	1	0	BT2 (0)	BT1 (0)	BT0 (0)	0	0	DC11 (0)	DC10 (0)	0	0	DC21 (0)	DC20 (0)	0	0	DC31 (0)	DC30 (0)	**Power control 3 (R11H)/** BT2-0:Adjust scale factor DC11-0:Adjust the frequency in stepup1 DC21-0: Adjust the frequency in stepup2 DC31-0: Adjust the frequency in stepup3
R13h	W	1	0	0	0	DCR_ EX (0)	0	DCR2 (0)	DCR1 (0)	DCR0 (0)	0	GVD6 (0)	GVD5 (0)	GVD4 (0)	GVD3 (0)	GVD2 (0)	GVD1 (0)	GVD0 (0)	**Power control 4 (R13H)/** DCR_EX: Input signal selection. DCR2-0: Set clock cycle for step-up circuit. GVD6-0:set GVDD voltage
R14h	W	1	VCOM G (1)	VCM6 (0)	VCM5 (0)	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)	VCMR (0)	VML6 (0)	VML5 (0)	VML4 (0)	VML3 (0)	VML2 (0)	VML1 (0)	VML0 (0)	**Power control 5 (R14H)/** VCOMG : VCOML -> GND VCMR: VCOMH control VCM6-0:set the VCOMH voltage VML6-0:set the VCOM Amplitude
R15h	W	1	0	0	0	0	0	0	0	0	0	VCIR2 (0)	VCIR1 (0)	VCIR0 (0)	0	0	0	0	**VCI Recycling (R15H)/** VCIR2-0: VCI Recycling period setting
R20h	W	1	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)	**RAM address register (R20H)/** AD7-AD0
R21h	W	1	0	0	0	0	0	0	0	AD16 (0)	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)	**RAM address register (R21H)/** AD15-AD8
R22h	W	1	WD17-0 : Pad assignment varies according to the interface method																**Write data to GRAM (R22H)/** WD17-0:Input data for GRAM
	R	1	RD17-0 : Pad assignment varies according to the interface method																**Read data from GRAM (R22H)/** RD17-0:Read data from GRAM
R28h	W	1	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0	**Software RESET(R28H)** 00CEh : Software RESET
R29h	W	1	0	FLM _INT1 (0)	FLM _INT0 (0)	0	0	0	0	FLM _POS8 (0)	FLM _POS7 (0)	FLM _POS6 (0)	FLM _POS5 (0)	FLM _POS4 (0)	FLM _POS3 (0)	FLM _POS2 (0)	FLM _POS1 (0)	FLM _POS0 (0)	**FLM FunctionT(R29H)** FLM_INT1-0: FLM Output Interval FLM_POS8-0: FLM Output Position
R30h	W	1	0	0	0	0	0	0	0	0	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)	**Gate Scan Position (R30H)/** SCN4-0 : scan starting position of gate
R31h	W	1	0	0	0	0	0	0	0	SEA8 (1)	SEA7 (0)	SEA6 (0)	SEA5 (1)	SEA4 (1)	SEA3 (1)	SEA2 (1)	SEA1 (1)	SEA0 (1)	**Vertical scroll control 1 (R31H,R32H)/** SEA7-0 : Scroll End Address SSA7-0 : Scroll Start Address
R32h	W	1	0	0	0	0	0	0	0	SSA8 (0)	SSA7 (0)	SSA6 (0)	SSA5 (0)	SSA4 (0)	SSA3 (0)	SSA2 (0)	SSA1 (0)	SSA0 (0)	
R33h	W	1	0	0	0	0	0	0	0	SST8 (0)	SST7 (0)	SST6 (0)	SST5 (0)	SST4 (0)	SST3 (0)	SST2 (0)	SST1 (0)	SST0 (0)	**Vertical scroll control 2(R33H)/** SST7-0 : Scroll Start and Step
R34h	W	1	0	0	0	0	0	0	0	SE18 (1)	SE17 (0)	SE16 (0)	SE15 (1)	SE14 (1)	SE13 (1)	SE12 (1)	SE11 (1)	SE10 (1)	**Partial screen driving position (R34H,R35H)/** SS17-10: screen start position SE17-10: screen end position
R35h	W	1	0	0	0	0	0	0	0	SS18 (0)	SS17 (0)	SS16 (0)	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)	
R36h	W	1	0	0	0	0	0	0	0	HEA8 (0)	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)	**Horizontal window address (R36H,R37H)/** HEA7-0: Horizontal window address end position HSA7-0: Horizontal window address start position
R37h			0	0	0	0	0	0	0	HSA8 (0)	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)	
R38h	W	1	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (0)	VEA6 (0)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)	**Vertical window Address (R38H,R39H)/** VEA7-0: Vertical window address end position VSA7-0: Vertical window address start position
R39h	W	1	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)	
R40h	W	1	0	0	0	0	0	0	0	0	FCV _EN (0)	0	MPU _MODE (0)	STN _EN (0)	SUB _IM1 (0)	SUB _IM0 (0)	0	VWAKE _EN (0)	**Sub Panel Control (R40H)/** FCV_EN: Format conversation MPU_MODE: set mpu mode STN_EN : set the panel SUB_IM : interface mode VWAKE_EN: Client Initiated Wake-up
R41h	W	1	WKL8 (0)	WKL7 (0)	WKL6 (0)	WKL5 (0)	WKL4 (0)	WKL3 (0)	WKL2 (0)	WKL1 (0)	WKL0 (0)	0	WKF3 (0)	WKF2 (0)	WKF1 (0)	WKF0 (0)	0	0	**MDDI link wake-up start position (R41H)/** **WKF3-0** : The frame that data is written **WKL8-0** : The line that data is written
R42h	W	1	0	0	0	0	0	0	0	0	SUB_SEL								**Sub panel selection index (R42H)** SUB_SEL: select main/sub panel

Reg.No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	Register Name / Description
R43h	W	1	0	0	0	0	0	0	0	0	SUB_WR								**Sub panel data write index (R43H)** SUB_WR: GRAM write data sub frame
R44h	W	1	0	0	0	0	0	0	0	0	0	0	GPIO5 (0)	GPIO4 (0)	GPIO3 (0)	GPIO2 (0)	GPIO1 (0)	GPIO0 (0)	**GPIO value(R44H)** GPIO 5-0
R45h	W	1	0	0	0	0	0	0	0	0	0	0	GPIO _CON5 (0)	GPIO _CON4 (0)	GPIO _CON3 (0)	GPIO _CON2 (0)	GPIO _CON1 (0)	GPIO _CON0 (0)	**GPIO in/output control(R45H)** GPIO 5-0
R46h	W	1	0	0	0	0	0	0	0	0	0	0	GPCLR 5 (0)	GPCLR 4 (0)	GPCLR 3 (0)	GPCLR 2 (0)	GPCLR 1 (0)	GPCLR 0 (0)	**GPIO Clear(R46H)** GPCLR 5-0
R47h	W	1	0	0	0	0	0	0	0	0	0	0	GPIO _EN5 (0)	GPIO _EN4 (0)	GPIO _EN3 (0)	GPIO _EN2 (0)	GPIO _EN1 (0)	GPIO _EN0 (0)	**GPIO interrupt enable(R47H)** GPIO_EN 5-0
R48h	W	1	0	0	0	0	0	0	0	0	0	0	GPPOL 5 (1)	GPPOL 4 (1)	GPPOL 3 (1)	GPPOL 2 (1)	GPPOL 1 (1)	GPPOL 0 (1)	**GPIO polarity selection (R48H)** GPPOL 5-0
R50h	W	1	0	0	0	0	PKP 13 (0)	PKP 12 (0)	PKP 11 (0)	PKP 10 (0)	0	0	0	0	PKP 03 (0)	PKP 02 (0)	PKP 01 (0)	PKP 00 (0)	**Gamma control 1 (R50H)/** Adjust Gamma voltage
R51h	W	1	0	0	0	0	PKP 33 (0)	PKP 32 (0)	PKP 31 (0)	PKP 30 (0)	0	0	0	0	PKP 23 (0)	PKP 22 (0)	PKP 21 (0)	PKP 20 (0)	**Gamma control 2 (R51H)/** Adjust Gamma voltage
R52h	W	1	0	0	0	0	PKP 53 (0)	PKP 52 (0)	PKP 51 (0)	PKP 50 (0)	0	0	0	0	PKP 43 (0)	PKP 42 (0)	PKP 41 (0)	PKP 40 (0)	**Gamma control 3 (R52H)/** Adjust Gamma voltage
R53h	W	1	0	0	0	0	PRP 13 (0)	PRP 12 (0)	PRP 11 (0)	PRP 10 (0)	0	0	0	0	PRP 03 (0)	PRP 02 (0)	PRP 01 (0)	PRP 00 (0)	**Gamma control 4 (R53H)/** Adjust Gamma voltage
R54h	W	1	0	0	0	0	PKN 13 (0)	PKN 12 (0)	PKN 11 (0)	PKN 10 (0)	0	0	0	0	PKN 03 (0)	PKN 02 (0)	PKN 01 (0)	PKN 00 (0)	**Gamma control 5 (R54H)/** Adjust Gamma voltage
R55h	W	1	0	0	0	0	PKN 33 (0)	PKN 32 (0)	PKN 31 (0)	PKN 30 (0)	0	0	0	0	PKN 23 (0)	PKN 22 (0)	PKN 21 (0)	PKN 20 (0)	**Gamma control 6 (R55H)/** Adjust Gamma voltage
R56h	W	1	0	0	0	0	PKN 53 (0)	PKN 52 (0)	PKN 51 (0)	PKN 50 (0)	0	0	0	0	PKN 43 (0)	PKN 42 (0)	PKN 41 (0)	PKN 40 (0)	**Gamma control 7 (R56H)/** Adjust Gamma voltage
R57h	W	1	0	0	0	0	PRN 13 (0)	PRN 12 (0)	PRN 11 (0)	PRN 10 (0)	0	0	0	0	PRN 03 (0)	PRN 02 (0)	PRN 01 (0)	PRN 00 (0)	**Gamma control 8 (R57H)/** Adjust Gamma voltage
R58h	W	1	0	0	0	VRP 14 (0)	VRP 13 (0)	VRP 12 (0)	VRP 11 (0)	VRP 10 (0)	0	0	0	VRP 04 (0)	VRP 03 (0)	VRP 02 (0)	VRP 01 (0)	VRP 00 (0)	**Gamma control 9 (R58H)/** Adjust Amplitude voltage
R59h	W	1	0	0	0	VRN 14 (0)	VRN 13 (0)	VRN 12 (0)	VRN 11 (0)	VRN 10 (0)	0	0	0	VRN 04 (0)	VRN 03 (0)	VRN 02 (0)	VRN 01 (0)	VRN 00 (0)	**Gamma control 10 (R59H)/** Adjust Amplitude voltage

Table 29. Instruction table 2

Reg.No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	Register Name / Description
R80h	W	1	0	0	0	0	0	0	0	0	TEST_ KEY7 (0)	TEST_ KEY6 (0)	TEST_ KEY5 (0)	TEST_ KEY4 (0)	TEST_ KEY3 (0)	TEST_ KEY2 (0)	TEST_ KEY1 (0)	TEST_ KEY0 (0)	**MTP Test Key (R80H)** Test Key to update MTP Value.
R81h	W	1	MTP_ MODE (0)	MTP_E X (0)	0	MTP_ SEL (0)	0	0	0	MTP_ ERB (1)	0	0	0	MTP_ WRB (1)	0	0	0	MTP_ LOAD (0)	**MTP Control Registers (R81H)**
R82h	W	1	0	0	0	0	GPI3 (0)	GPI2 (0)	GPI1 (0)	GPI0 (0)	0	0	0	MTP _DIN4 (0)	MTP _DIN3 (0)	MTP _DIN2 (0)	MTP _DIN1 (0)	MTP _DIN0 (0)	**MTP Data Write (R82H)** GPI3-0: GPI Input
	R	1	X	X	X	X	X	X	GPI3	GPI2	GPI1	GPI0	MTP _DOUT 5	MTP _DOUT 4	MTP _DOUT 3	MTP _DOUT 2	MTP _DOUT 1	MTP _DOUT 0	**MTP Data Read (R82H)**
R83h	W	1	P_ NAME7	P_ NAME6	P_ NAME5	P_ NAME4	P_ NAME3	P_ NAME2	P_ NAME1	P_ NAME0	P_ VER7	P_ VER6	P_ VER5	P_ VER4	P_ VER3	P_ VER2	P_ VER1	P_ VER0	**Product Name/Version Write (R83H)**

9.3. Description of Instructions

9.3.1. Index Register (IR)

The index instruction specifies the RAM control indexes (R00h to R83h). It sets the register number in the range of 00000000 to 11111111 in binary form.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

9.3.2. Status Read

The status read instruction reads out the internal status of the IC.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	0	0	0	0	0	0	0	L8	L7	L6	L5	L4	L3	L2	L1	L0

L8–0: Indicate the driving raster-row position in scan address of GRAM where the liquid crystal display is being driven.

9.3.3. Version Management (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	VER 7	VER 6	VER 5	VER 4	VER 3	VER 2	VER 1	VER 0	VER 27	VER 26	VER 25	VER 24	VER 23	VER 22	VER 21	VER 20

When PNP_EN = 1, Bit 8 to 15 shows a product name. Bit 0 to 7 shows a product version

When PNP_EN = 0, Read device code “0154h”.

9.3.4. Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VSPL	HSPL	DPL	EPL	0	SM	GS	SS	0	0	NL5	NL4	NL3	NL2	NL1	NL0

VSPL: reverses the polarity of the VSYNC signal.

VSPL= “0”: VSYNC is low active.

VSPL= “1”: VSYNC is high active.

HSPL: reverses the polarity of the HSYNC signal.

HSPL= “0”: HSYNC is low active.

HSPL= “1”: HSYNC is high active.

DPL: reverses the polarity of the DOTCLK signal.

DPL= “0”: Display data is fetched at DOTCLK’s rising edge.

DPL= “1”: Display data is fetched at DOTCLK’s falling edge.

EPL: Set the polarity of ENABLE pin while using RGB interface.

EPL = “0”: ENABLE =”Low” / write data of DB17-0

ENABLE =”High” / do not write data of DB17-0

EPL = “1”: ENABLE =”High” / write data of DB17-0

ENABLE =”Low” / do not write data of DB17-0

Table 30. Relationship between EPL, ENABLE and RAM access

EPL	ENABLE	RAM write	RAM address
0	0	Valid	Updated
0	1	Invalid	Held
1	0	Invalid	Held
1	1	Valid	Updated

Note. When RGB mode 2 is used, EPL must be Low.

SM: Select the division drive method of the gate driver. When SM = 0, even/odd division is selected; SM = 1, upper/lower division drive is selected by NL5-0(Upper NL5-0/2 and Lower NL5-0/2). Various connections between TFT panel and the IC can be supported with the combination of SM and GS bit.

Note. When SM = 1, NL setting is disable.

GS: Set the order of Gate Clock generation. When GS = 0, G1 is output first and G320 is finally output. When GS = 1, G320 is output first and G1 is finally output (NL = 6'b101000). But in case of NL = 6'b001100, when GS = 0, G1 is output first and G96 is finally output, and when GS = 1, G96 is output first and G1 is finally output

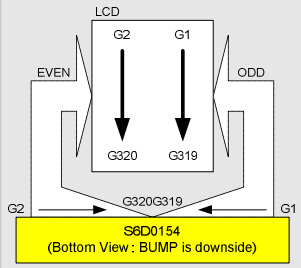
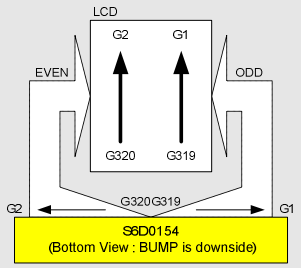
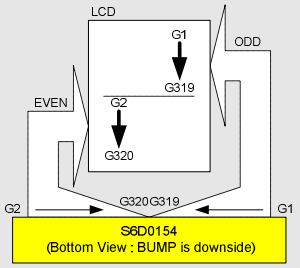
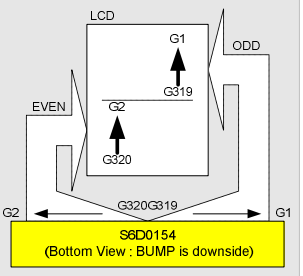
SM	0	0	1	1
GS	0	1	0	1
				
	G1→ G2→ G3→ ... → G318→ G319→ G320	G320→ G319→ G318→ ... → G3→ G2→ G1	G1→G3→ ... → G319→G2→G4→ ... →G320	G320→G318→ ... →G2→G319→G317→... →G1

Figure 21. Gate Clock Generation order selection using GS and SM (NL=6'b101000, SCN=6'b000000)

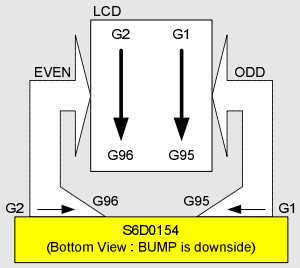
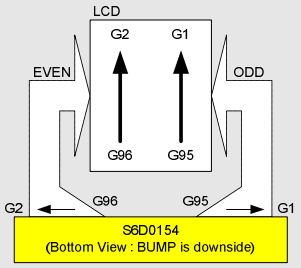
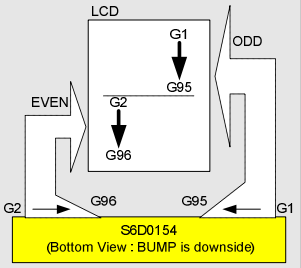
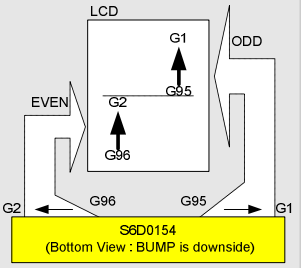
SM	0	0	1	1
GS	0	1	0	1
				
	G1→ G2 → G3 → ... → G94 → G95 → G96	G96 → G95 → G94 → ... → G3 → G2 → G1	G1 → G3 → ...→ G95→ G2→ G4→ ...→G96	G96→ G94→ ...→ G2→ G95→ G93→ ...→ G1

Figure 22. Gate Clock Generation order selection using GS and SM (NL = 6'b001100, SCN = 6'b000000)

SS

Select the direction of the source driver channel in pixel unit.

When user changes the value of SS, memory should be updated to apply the change.

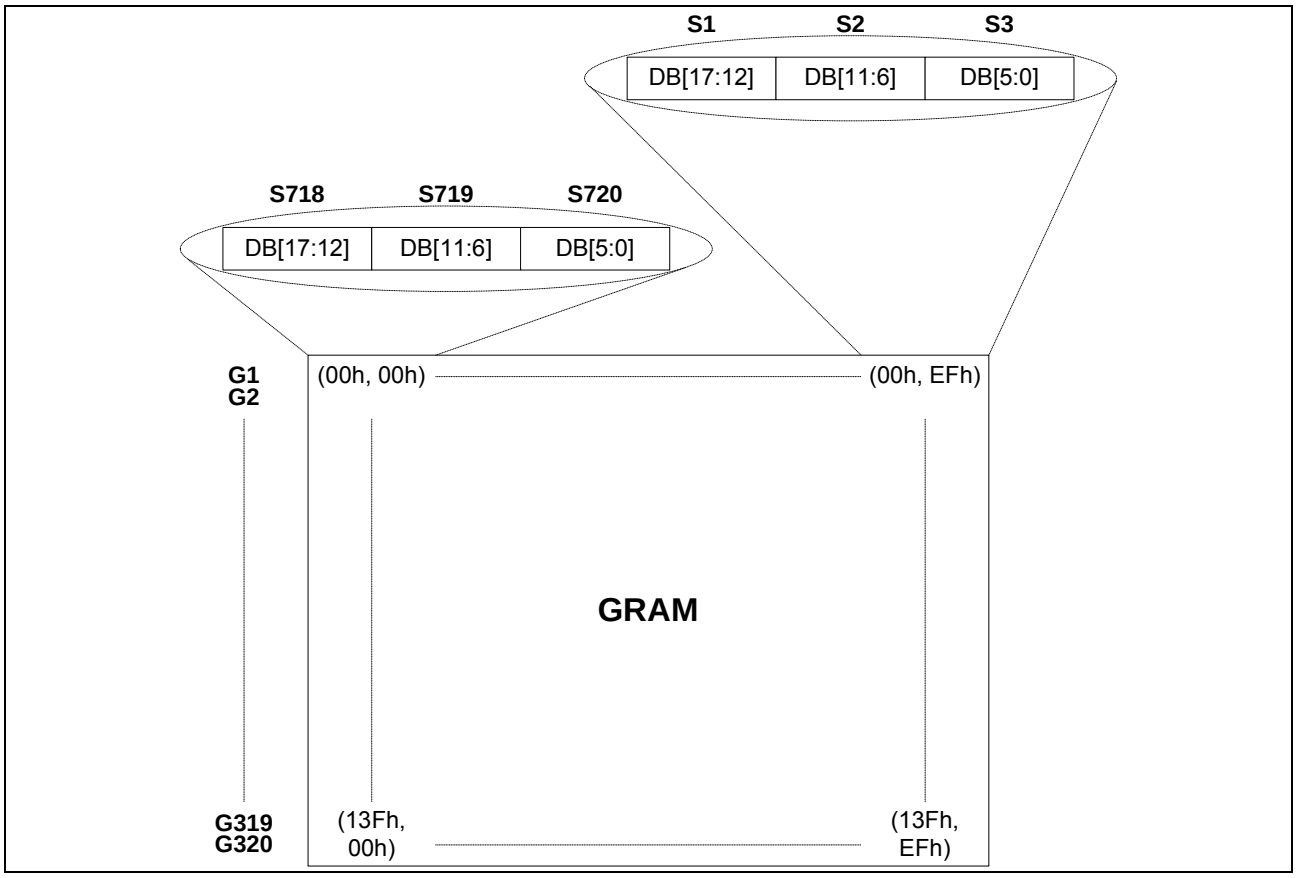


Figure 23. Image mirroring using SS register (SS = "1")

Note.

The display condition of this figure is like this.

SS = 1, BGR = 0, GS = 0.

NL

Specify the number of horizontal lines to be driven. The number of the lines can be adjusted in units of eight. GRAM address mapping is independent of this setting. The set value should be more than the panel size. Do not change setting of NL [5:0] in DISPLAY ON STATE.

Table 31. NL bit and Drive Duty (SCN = "000000")

NL[5:0]	Display Size	Drive Line	Gate Driver- Lines Used
000000	*Reserved*		
000001	720 X 8 dots	8	G1 to G8
000010	720 X 16 dots	16	G1 to G16
000011	720 X 24 dots	24	G1 to G24
000100	720 X 32 dots	32	G1 to G32
000101	720 X 40 dots	40	G1 to G40
000110	720 X 48 dots	48	G1 to G48
000111	720 X 56 dots	56	G1 to G56
001000	720 X 64 dots	64	G1 to G64
001001	720 X 72 dots	72	G1 to G72
001010	720 X 80 dots	80	G1 to G80
001011	720 X 88 dots	88	G1 to G88
001100	720 X 96 dots	96	G1 to G96
001101	720 X 104 dots	104	G1 to G104
001110	720 X 112 dots	112	G1 to G112
001111	720 X 120 dots	120	G1 to G120
010000	720 X 128 dots	128	G1 to G128
010001	720 X 136 dots	136	G1 to G136
010010	720 X 144 dots	144	G1 to G144
010011	720 X 152 dots	152	G1 to G152
010100	720 X 160 dots	160	G1 to G160
010101	720 X 168 dots	168	G1 to G168
010110	720 X 176 dots	176	G1 to G176
010111	720 X 184 dots	184	G1 to G184
011000	720 X 192 dots	192	G1 to G192
011001	720 X 200 dots	200	G1 to G200
011010	720 X 208 dots	208	G1 to G208
011011	720 X 216 dots	216	G1 to G216
011100	720 X 224 dots	224	G1 to G224
011101	720 X 232 dots	232	G1 to G232
011110	720 X 240 dots	240	G1 to G240
011111	720 X 248 dots	248	G1 to G248
100000	720 X 256 dots	256	G1 to G256
100001	720 X 264 dots	264	G1 to G264
100010	720 X 272 dots	272	G1 to G272
100011	720 X 280 dots	280	G1 to G280
100100	720 X 288 dots	288	G1 to G288
100101	720 X 296 dots	296	G1 to G296
100110	720 X 304 dots	304	G1 to G304
100111	720 X 312 dots	312	G1 to G312
101000	720 X 320 dots	320	G1 to G320
101001 … 111111	Setting Disable		

Note.

1. A FP (front porch) and BP (back porch) period will be inserted as blanking period (All gates output VGL level) before / after the driver scan through all of the scans.
2. When SM = 1, NL setting is disable.

9.3.5. LCD-Driving-Waveform Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	INV1	INV0	0	0	0	0	0	0	0	FLD

INV1-0 / FLD

Set LCD inversion method as show below.

Enables or disables 3-field interlaced scanning function like below. When you want to save power consumption, you'd better enable 3 field interlaced scanning function. 3-field interlaced scanning function and Two Line Mixed Inversion scanning function are properly operated in FP=2, SM=0 and VCIR2-0=000.

Table 32. LCD inversion selection / Interlaced scanning method control

INV[1:0]	FLD	Description
00	0	Frame Inversion
	1	3 field interlace
01	0	Line Inversion
	1	Setting Disable
10	0	Two Line Mixed Inversion
	1	Setting Disable
11	0	No Inversion. Active with positive polarity (VCOM = Low)
	1	No Inversion. Active with negative polarity (VCOM = High)

Note.

1. The interlaced scanning method can be set in the 3-field interlace when both window addresses and display area is related with 240x320 resolution in normal mode e.g. window address setting, partial screen driving position, number of driving lines.
2. Employing 3-field interlaced scanning method could deteriorate the display quality.

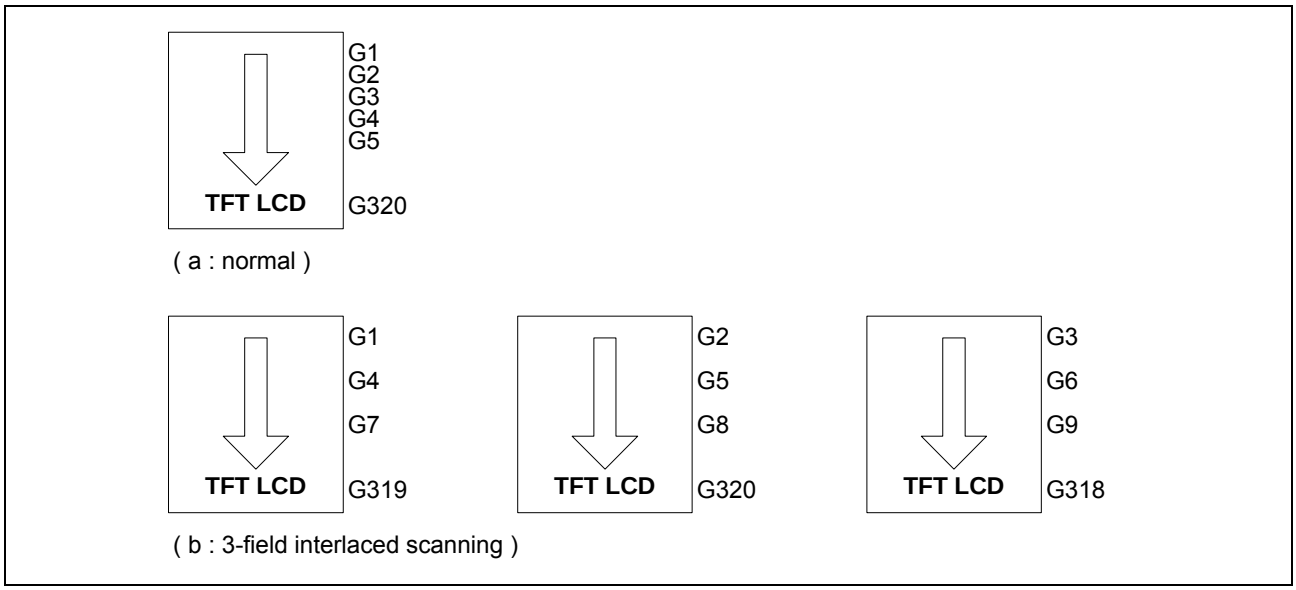


Figure 24. Interlaced scanning methods

GS = "0"

INV1-0, FLD : setting value	000	001		
Gate \ Field	-	(1)	(2)	(3)
G1	O	O		
G2	O		O	
G3	O			O
G4	O	O		
G5	O		O	
G6	O			O
G7	O	O		
G8	O		O	
G9	O			O
G317	O		O	
G318	O			O
G319	O	O		
G320	O		O	

GS = "1"

INV1-0, FLD : setting value	000	001		
Gate \ Field	-	(1)	(2)	(3)
G320	O	O		
G319	O		O	
G318	O			O
G317	O	O		
G316	O		O	
G315	O			O
G314	O	O		
G313	O		O	
G312	O			O
G4	O		O	
G3	O			O
G2	O	O		
G1	O		O	

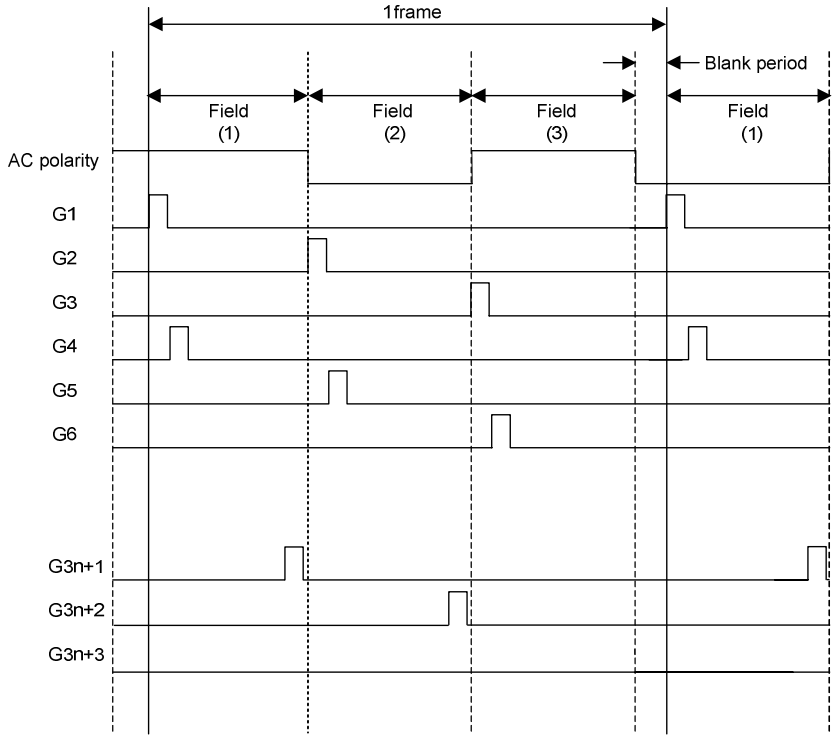


Figure 25. Interlace drive and output waveform (3 Field Interlace)

GS = "0"

INV1-0, FLD : setting value	000	100				
Gate \ Field	-	(1)	(2)	(3)	· · ·	(160)
G1	O	O			· · ·	
G2	O		O		· · ·	
G3	O	O			· · ·	
G4	O		O		· · ·	
G5	O			O	· · ·	
G6	O				· · ·	
G7	O			O	· · ·	
G8	O				· · ·	
G9	O				· · ·	
G317	O				· · ·	
G318	O				· · ·	O
G319	O				· · ·	
G320	O				· · ·	O

GS = "1"

INV1-0, FLD : setting value	000	100				
Gate \ Field	-	(1)	(2)	(3)	· · ·	(160)
G320	O	O			· · ·	
G319	O		O		· · ·	
G318	O	O			· · ·	
G317	O		O		· · ·	
G316	O			O	· · ·	
G315	O				· · ·	
G314	O			O	· · ·	
G313	O				· · ·	
G312	O				· · ·	
G4	O				· · ·	
G3	O				· · ·	O
G2	O				· · ·	
G1	O				· · ·	O

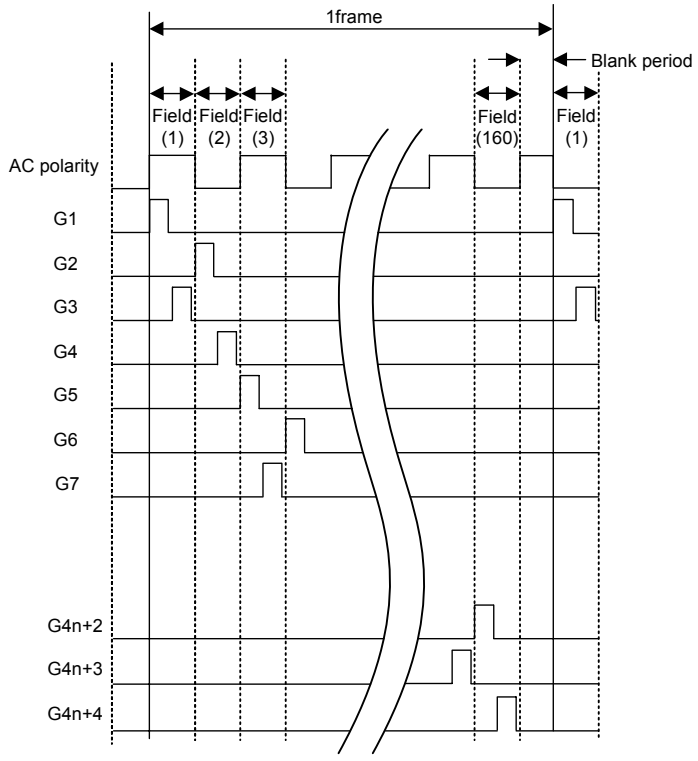


Figure 26. Interlace drive and output waveform (Two Line Mixed Inversion)

9.3.6. Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	BGR	0	0	MDT1	MDT0	0	0	ID1	ID0	AM	0	0	0

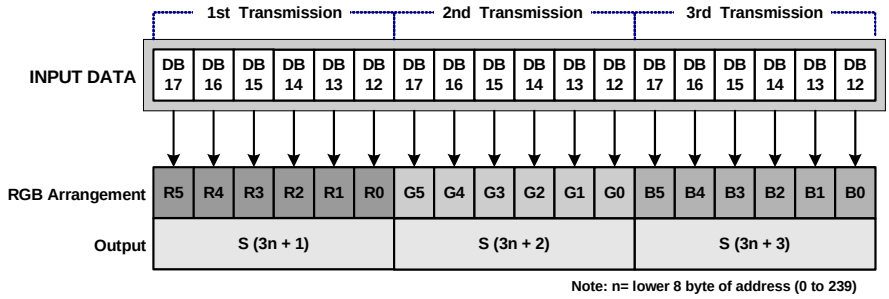
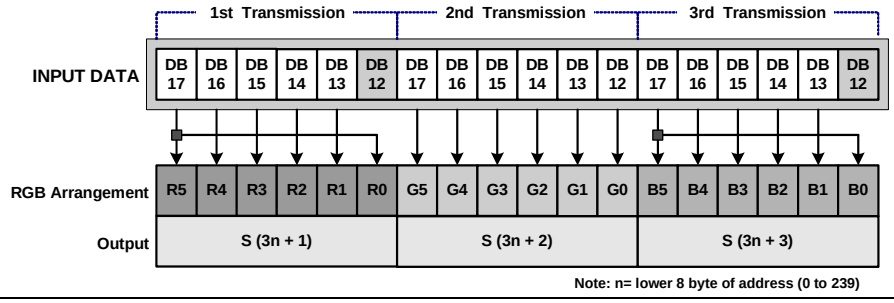
BGR

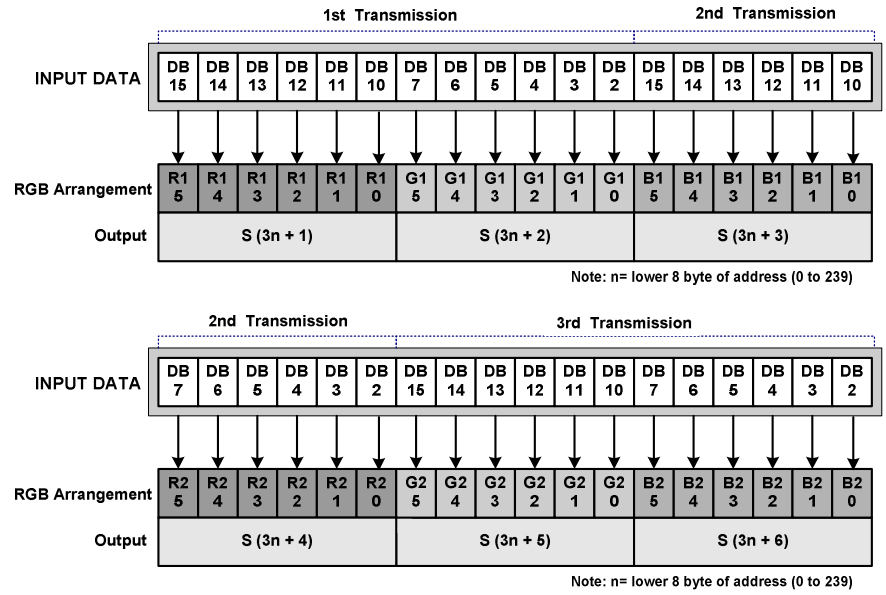
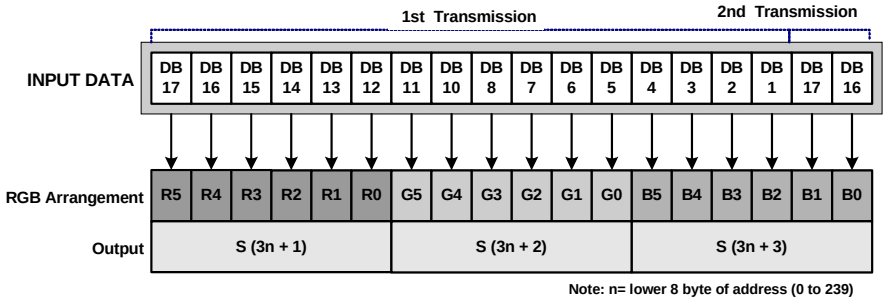
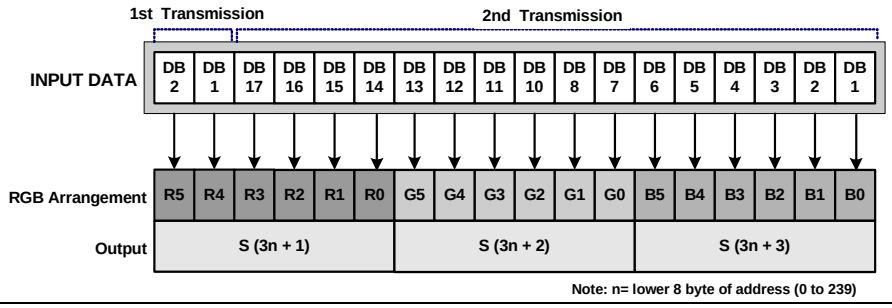
When 18-bit data is written to GRAM through DB bus, RGB assignment can be changed.

- BGR = 0; {DB [17:12], DB [11:6], DB [5:0]} is assigned to {R, G, B}. Actually the analog value that corresponds to DB [17:12] is output firstly at source output
- BGR = 1; {DB [17:12], DB [11:6], DB [5:0]} is assigned to {B, G, R}. Actually the analog value that corresponds to DB [5:0] is output firstly at source output.

MDT1: This bit is active on the 68/80-system of 8-bit bus, and the data for 1-pixel is transported to the memory for 3 write cycles. This bit is on the 68/80-system of 16-bit bus, and the data for 1-pixel is transported to the memory for 2 write cycles. When the 68/80-system interface mode is not set in the 8-bit or16-bit mode, set MDT1 bit to be “0”.

MDT0: When 8-bit or16-bit 68/80 interface mode and MDT1 bit =1, MDT0 defines color depth for the IC.

<table>
<tr><th>Interface Mode</th><th>MDT1</th><th>MDT0</th><th>Write data to GRAM</th></tr>
<tr><td>*</td><td>0</td><td>0</td><td>Default value. Multiple Data Transfer (MDT1-0) function is not available. Data Transfer is controlled by interface mode.</td></tr>
<tr><td rowspan="3">68/80-system 8-bit</td><td>0</td><td>1</td><td>Multiple Data Transfer (MDT1-0) function is not available.</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td> 
</td></tr>
<tr><td>1</td><td> 
</td></tr>
</table>

Interface Mode	MDT1	MDT0	Data Assignment
68/80-system 16-bit	0	1	
	1	0	
		1	

8-bit (68/80-system), MDT0 = 0: 262k-color mode (3 times of 6-bit data transfer to GRAM)

8-bit (68/80-system), MDT0 = 1: 65k-color mode (5-bit, 6-bit, 5-bit data transfer to GRAM)

16-bit (68/80-system), MDT0 = 0: 262k-color mode (16-bit, 2-bit data transfer to GRAM)

16-bit (68/80-system), MDT0 = 1: 262k-color mode (2-bit, 16-bit data transfer to GRAM)

ID

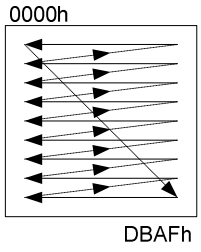
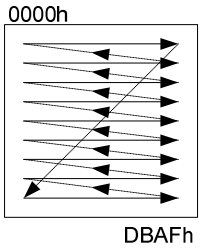
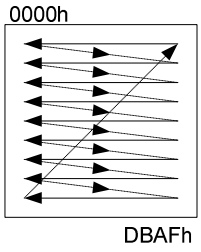
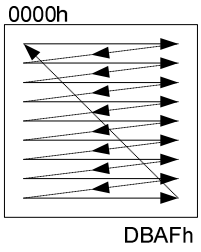
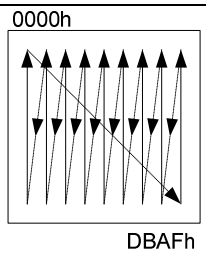
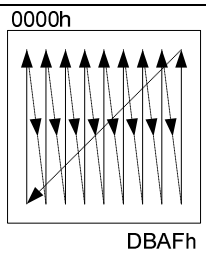
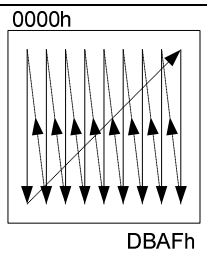
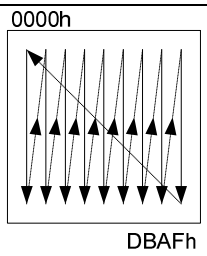
When ID [1], ID [0] = 1, the address counter (AC) is automatically increased by 1 after the data is written to the GRAM. When ID [1], ID [0] = 0, the AC is automatically decreased by 1 after the data is written to the GRAM.

The increment/decrement setting of the address counter using ID [1:0] is done independently for the horizontal address and vertical address.

AM

Set the automatic update method of the AC after the data is written to GRAM. When AM = “0”, the data is continuously written in horizontally. When AM = “1”, the data is continuously written vertically. When window addresses are specified, the GRAM in the window range can be written to according to the ID [1:0] and AM.

Table 33. Address Direction Setting

	ID[1:0] = “00” H: decrement V: decrement	ID[1:0] = “01” H: increment V: decrement	ID[1:0] = “10” H: decrement V: increment	ID[1:0] = “11” H: increment V: increment
AM=”0” Horizontal Update				
AM=”1” Vertical Update				

Note. When window addresses have been set, the GRAM can only be written within the window.

When AM or ID is set, the start address should be written accordingly prior to memory write.

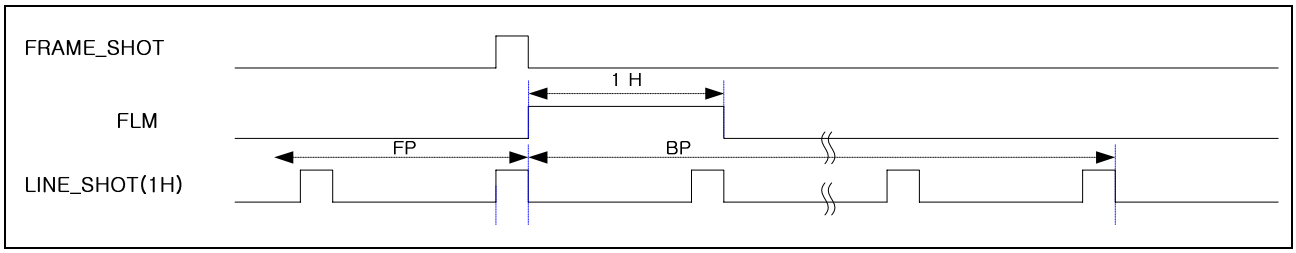
9.3.7. Display Control (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	FLM_MON	0	0	0	0	0	0	0	GON	CL	REV	D1	D0

FLM_MON:

FLM_MON = 1, Enable the Frame flag output signal from the FLM signal line for preventing Tearing Effect.

FLM_MON = 0, Disable the Frame flag output signal from the FLM signal line for preventing Tearing Effect.



GON: Gate on/off control signal. All gate outputs are set to be gate off level when GON = 0.

When GON = 1, gate driver is working: G1 to G220 output is either VGH or VGL level. See the Instruction set up flow for further description on the display on/off flow.

GON	Gate Output
0	All gates off (VGL)
1	Gate on(VGH / VGL)

CL: CL = 1 selects 8-color display mode. For details, see the section on 8-COLOR DISPLAY MODE.

CL	Number of display colors
0	262,144 colors
1	8 colors

REV: Displays all character and graphics display sections with reversal when REV = 1. For details, see the Reversed Display Function section. Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels.

REV	GRAM Data	Display Area	
		Positive	Negative
0	6'b000000 : 6'b111111	V63 : V0	V0 : V63
1	6'b000000 : 6'b111111	V0 : V63	V63 : V0

D1–0: Display is on when D1 = 1 and off when D1 = 0. When off, the display data remains in the GRAM, and can be re-displayed instantly by setting D1 = 1. When D1 is 0, the display is off with the entire source outputs set to the VSS level. Because of this, the S6D0154 can control the charging current for the LCD with AC driving. Control the display on/off while control GON. For details, see the Instruction set up flow.

When D1–0 = 01, the internal display of the S6D0154 is performed although the display is off. When D1-0 = 00, the internal display operation halts and the display is off.

D1	D0	GON	Source output	Gate Output	VCOM Output	display
0	0	X	AVSS	AVSS	AVSS	off
0	1	0	AVSS	VGL	AVSS	off
		1	AVSS	Operate	AVSS	on
1	0	0	White on Normally White Panel Black on Normally Black Panel	VGL	Operate	off
		1	White on Normally White Panel Black on Normally Black Panel	Operate	Operate	on
1	1	0	Normal Display	VGL	Operate	off
		1	Normal Display	Operate	Operate	on

Note.

1. In standby mode or D1–0 = 00, gate outputs go to AVSS level
2. Writing from MCU to GRAM is independent of D1–0.
3. When source output is the same phase with VCOM, white screen is displayed at normally white LCD panel

9.3.8. Blank Period Control 1 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

The blanking period in the front and end of the display area can be defined using this register.
When N-raster-row is driving, a blank period is inserted after all screens are drawn. Front and Back porch can be adjusted using FP3-0 and BP3-0 bits (R08h).

FP3-0/BP3-0: Set the blanking periods (the front and back porch) which are placed at the beginning and the end of the data in. FP3-0 is for a front porch and BP3-0 is for a back porch. When front and back porches are set, the settings should meet the following conditions.

BP + FP ≤ 16 raster-rows
FP ≥ 2 raster-rows
BP ≥ 2 raster-rows

When the external display interface is in use, the back porch (BP) will start on the falling edge of the VSYNC signal and the display operation will commence at the end of the back-porch period. The front porch (FP) will start when data for the number of raster-rows specified by the NL bits has been displayed. During the period between the completion of the front-porch period and the next VSYNC signal, the display will remain blank.

Table 34. Front/Back Porch

FP3 BP3	FP2 BP2	FP1 BP1	FP0 BP0	# of Raster Periods In the Front Porch # of Raster Periods In the Back Porch
0	0	0	0	Setting Disabled
0	0	0	1	Setting Disabled
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	Setting Disabled

9.3.9. Frame Cycle Control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO3	NO2	NO1	NO0	SDT3	SDT2	SDT1	SDT0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

NO3-0: Set amount of non-overlap for the gate output.

NO3	NO2	NO1	NO0	Amount of non-overlap		
				Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)	
					18-bit RGB	6-bit RGB
0	0	0	0	Setting disable	Setting disable	Setting disable
0	0	0	1	1 INCLK	8 dot clock	8*3 dot clock
0	0	1	0	2 INCLK	16 dot clock	16*3 dot clock
0	0	1	1	3 INCLK	24 dot clock	24*3 dot clock
0	1	0	0	4 INCLK	32 dot clock	32*3 dot clock
0	1	0	1	5 INCLK	40 dot clock	40*3 dot clock
0	1	1	0	6 INCLK	48 dot clock	48*3 dot clock
0	1	1	1	7 INCLK	56 dot clock	56*3 dot clock
1	0	0	0	8 INCLK	64 dot clock	64*3 dot clock
1	0	0	1	9 INCLK	72 dot clock	72*3 dot clock
1	0	1	0	10 INCLK	80 dot clock	80*3 dot clock
1	0	1	1	Setting disable	88 dot clock	88*3 dot clock
1	1	0	0	Setting disable	96 dot clock	96*3 dot clock
1	1	0	1	Setting disable	104 dot clock	104*3 dot clock
1	1	1	0	Setting disable	112dot clock	112*3 dot clock
1	1	1	1	Setting disable	120dot clock	120*3 dot clock

Note. The amount of non-overlap time is defined from starting time of 1H.

SDT3-0: Set delay amount from gate edge (end) to source output.

SDT3	SDT2	SDT1	SDT0	Delay amount of the source output		
				Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)	
					18-bit RGB	6-bit RGB
0	0	0	0	Setting disable	Setting disable	Setting disable
0	0	0	1	1 INCLK	8 dot clock	8*3 dot clock
0	0	1	0	2 INCLK	16 dot clock	16*3 dot clock
0	0	1	1	3 INCLK	24 dot clock	24*3 dot clock
0	1	0	0	4 INCLK	32 dot clock	32*3 dot clock
0	1	0	1	5 INCLK	40 dot clock	40*3 dot clock
0	1	1	0	6 INCLK	48 dot clock	48*3 dot clock
0	1	1	1	7 INCLK	56 dot clock	56*3 dot clock
1	0	0	0	8 INCLK	64 dot clock	64*3 dot clock
1	0	0	1	9 INCLK	72 dot clock	72*3 dot clock
1	0	1	0	10 INCLK	80 dot clock	80*3 dot clock
1	0	1	1	Setting disable	88 dot clock	88*3 dot clock
1	1	0	0	Setting disable	96 dot clock	96*3 dot clock
1	1	0	1	Setting disable	104 dot clock	104*3 dot clock
1	1	1	0	Setting disable	112dot clock	112*3 dot clock
1	1	1	1	Setting disable	120dot clock	120*3 dot clock

RTN3-0: Set the 1H period (1 raster-row).

RTN3	RTN2	RTN1	RTN0	1 Horizontal clock cycle (CL1)
0	0	0	0	16 INCLK
0	0	0	1	17 INCLK
0	0	1	0	18 INCLK
0	0	1	1	19 INCLK
0	1	0	0	20 INCLK
0	1	0	1	21 INCLK
0	1	1	0	22 INCLK
0	1	1	1	23 INCLK
1	0	0	0	24 INCLK
1	0	0	1	25 INCLK
1	0	1	0	26 INCLK
1	0	1	1	27 INCLK
1	1	0	0	28 INCLK
1	1	0	1	29 INCLK
1	1	1	0	30 INCLK
1	1	1	1	31 INCLK

9.3.10. External Display Interface Control (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

RM: Specify the interface for GRAM access as shown below. This register and DM register can be set independently. The display data can be written through System Interface by clearing this register while the RGB interface is used.

Table 35. RM and GRAM Access Interface

RM	GRAM Access Interface
0	System interface
1	RGB interface

DM1-0: Specify the display operation mode. The interface can be set based on the bits of DM. This setting enables switching interface between internal operation and the external display interface.
Switching between two external display interfaces (RGB interface) should not be done.

DM[1:0]	Display Operation Mode	Display Operation Mode in MDDI
00	Internal clock operation	Internal clock operation
01	RGB interface	Setting Disable
10	Setting Disable	Setting Disable
11	RGB interface for PNP mode	Setting Disable

RIM1-0: Specify the RGB interface mode when the RGB interface is used. Specifically, this setting specifies the mode when the bits of DM and RM are set to RGB interface. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (one transfer/pixel)
0	1	16-bit RGB interface (one transfer /pixel)
1	0	6-bit RGB interface (three transfers /pixel)
1	1	Setting disabled

You should notice that some display functions, which will be described later, cannot be used according to the display mode shown below.

Table 36. Display Functions and Display Modes

Function	External Clock Operation Mode	Internal Clock Operation Mode
Partial Display	Cannot be used	Can be used
Scroll Function	Cannot be used	Can be used
Rotation	Cannot be used	Can be used
Mirroring	Cannot be used	Can be used
Window Function	Cannot be used	Can be used

Depending on the external display interface setting, various interfaces can be specified to match the display state. While displaying motion pictures (RGB interface), the data for display can be written in high-speed write mode, which achieves both low power consumption and high-speed access.

Table 37. Display State and Interface

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM[1:0])
Still Pictures	Internal Clock	System interface (RM=0)	Internal clock (DM[1:0]=00)
Motion Pictures	RGB interface (1)	RGB interface (RM=1)	RGB interface (DM[1:0]=01)
Rewrite still picture area while displaying motion pictures	RGB interface (2)	System interface (RM=0)	RGB interface (DM[1:0]=01)

Note.

1. The instruction register can only be set through the system interface (SPI).
2. The RGB interface mode should not be set during operation.
3. For more information about the transition flow of each operation mode, see the Transition Sequences between Display Modes section.
4. When RGB interface mode 2 is used, EPL must be low.

Internal Clock Mode

All display operation is controlled by signals generated by the internal clock in internal clock mode.
All inputs through the external display interface are invalid. The internal RAM can be accessed only via the system interface.

RGB Interface Mode (1)

The display operations are controlled by the frame synchronization clock (VSYNC), raster-row synchronization signal (HSYNC), and dot clock (DOTCLK) in RGB interface mode. These signals should be supplied during display operation in this mode.

The display data is transferred to the internal RAM via DB17-0 for each pixel. Combining the function of the high-speed write mode and the window address enables display of both the motion picture area and the internal RAM area simultaneously. In this method, data is only transferred when the screen is updated, which reduces the amount of data transferred.

The periods of the front (FP), back (BP) porch, and the display are automatically generated in the S6D0154 by counting the raster-row synchronization signal (HSYNC) based on the frame synchronization signal (VSYNC).

RGB Interface Mode (2)

When RGB interface is in use, data can be written to RAM via the system interface. This write operation should be performed while data for display is not being transferred via RGB interface (ENABLE = active). Before the next data transfer for display via RGB interface, the setting above should be changed, and then the address and index (R22h) should be set.

MDDI Interface Mode

The MDDI standard, an optimized high-speed serial interconnection technology developed by Qualcomm, increases reliability and reduces power consumption, which interface for forward and reverse data transmission. Internal bus architecture provides a way to read and write registers via MDDI.

The MDDI has a differential pair to get low EMI, low power and high speed, increasing the speed of forward direction, encodes data to strobe signal in host.

The front and back porch period and the display period are automatically generated by the frame synchronization signal (VSYNC) according to the setting of the S6D0154 registers.

Start Oscillation (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	FOSC4	FOSC3	FOSC2	FOSC1	FOSC0	0	0	0	0	0	0	0	OSC ON

FOSC4-0: Select the oscillation frequency of internal oscillator

Table 38. Oscillation Frequency

FOSC[4:0]	Oscillation Frequency	FOSC[4:0]	Oscillation Frequency
00000	X 0.91	10000	X 1.28
00001	X 0.93	10001	X 1.32
00010	X 0.94	10010	X 1.35
00011	X 0.96	10011	X 1.39
00100	X 0.98	10100	X 1.43
00101	X 1.00 (Default)	10101	X 1.47
00110	X 1.02	10110	X 1.52
00111	X 1.04	10111	X 1.56
01000	X 1.06	11000	X 1.61
01001	X 1.09	11001	X 1.67
01010	X 1.11	11010	X 1.72
01011	X 1.14	11011	X 1.79
01100	X 1.16	11100	X 1.85
01101	X 1.19	11101	X 1.92
01110	X 1.22	11110	X 2.00
01111	X 1.25	11111	X 2.08

Note. If the default oscillation frequency is 323 KHz and register setting of FOSC [4:0] is 00101.

OSCON: This instruction starts the oscillator from the Halt State in the standby mode. After this instruction, wait at least 10 ms for oscillation to stabilize before giving the next instruction.

When OSCON = 1: OSC ON, OSCON = 0: OSC OFF

9.3.11. Power Control 1 (R10h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	SAP3	SAP2	SAP1	SAP0	0	0	0	0	0	0	DSTB	STB

SAP3-0: Adjust the slew-rate of the operational amplifier for the source driver. If higher SAP3-0 is set, LCD panel having higher resolution or higher frame frequency can be driven because the slew-rate of the operational amplifier is increased. But these bits must be set as adequate value because the amount of fixed current of the operational amplifier is also adjusted. During non-display, when SAP3-0 ="0000", operational amplifiers are turned off, so current consumption can be reduced.

SAP3	SAP2	SAP1	SAP0	Source Amp. Current Level	Slew rate[us/V]	Delay[us]
0	0	0	0	Amp. Stop	-	-
0	0	0	1	Setting Disable		
0	0	1	0	Setting Disable		
0	0	1	1	Slow 3	5.38	26.9
0	1	0	0	Medium Slow 1	4.18	20.9
0	1	0	1	Medium Slow 2	3.44	17.2
0	1	1	0	Medium Slow 3	2.88	14.4
0	1	1	1	Medium Slow 4	2.54	12.7
1	0	0	0	Medium Fast 1	2.40	12.0
1	0	0	1	Medium Fast 2	2.04	10.2
1	0	1	0	Medium Fast 3	1.96	9.8
1	0	1	1	Medium Fast 4	1.76	8.8
1	1	0	0	Fast1	1.66	8.3
1	1	0	1	Fast2	1.60	8.0
1	1	1	0	Fast3	1.52	7.6
1	1	1	1	Fast4 (the Fastest)	1.42	7.1

DSTB: When DSTB = 1, the S6D0154 enters the deep standby mode, where the power supply for the internal logic is turned off to save more power than the standby mode. Writing the GRAM data or setting any instructions are prohibited during the deep-standby mode and they must be reset after releasing from the deep standby mode.

For more information, see the Standby Mode section.

STB: When STB = 1, the S6D0154 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For more information, see the Standby Mode section.

Outputs	Conditions
VCOM	AVSS
Gate	AVSS
Source	AVSS

9.3.12. Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	APON	PON3	PON2	PON1	PON	0	AB_VCI1	AON	VCI1_EN	VC3	VC2	VC1	VC0

APON: This is an automatic-boosting-operation-starting bit for the booster circuits. In case of APON=0, the automatic booster sequence circuit is stopped, but the booster circuits are independently operated by PON, PON1, PON2 and PON3 bits. In case of APON=1, booster circuits are automatically and sequentially operated. For further information about timing, please refer to the SET UP FLOW OF POWER SUPPLY.

PON3: This is an operation-starting bit for the booster circuit 3(VCL). In case of PON3 = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON3= 1, please refer to the SET UP FLOW OF POWER SUPPLY.

PON2: This is an operation-starting bit for the booster circuit 2(VGL). In case of PON2 = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON2= 1, please refer to the SET UP FLOW OF POWER SUPPLY.

PON1: This is an operation-starting bit for the booster circuit 2(VGH). In case of PON1 = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON1= 1, please refer to the SET UP FLOW OF POWER SUPPLY.

PON: This is an operation-starting bit for the booster circuit1. In case of PON = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON = 1, please refer to the SET UP FLOW OF POWER SUPPLY.

AB_VCI1: Set VCI1 output equal to VCI. VCI1 output is internally connected to VCI via switching circuit when AB_VCI="H".

AON: This is an operation-starting bit for the Amplifier. In case of AON = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the AON= 1, please refer to the SET UP FLOW OF POWER SUPPLY.

VCI1_EN: Internal VCI1 generation amplifier operation control bit. When VCI1_EN=0, VCI1 voltage is not generated.

VC3-0: Set the VCI1 voltage. These bits set the VCI1 voltage up to 3V as the nominal output (Upper limit value may depend on VCI voltage)

VC3	VC2	VC1	VC0	VCI1
0	0	0	0	1.35
0	0	0	1	1.75
0	0	1	0	2.07
0	0	1	1	2.16
0	1	0	0	2.25
0	1	0	1	2.34
0	1	1	0	2.43
0	1	1	1	2.52
1	0	0	0	2.58
1	0	0	1	2.64
1	0	1	0	2.70
1	0	1	1	2.76
1	1	0	0	2.82
1	1	0	1	2.88
1	1	1	0	2.94
1	1	1	1	3

Note. Do not set any higher VCI1 level than VCI.

Power Control 3 (R12h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	BT2	BT1	BT0	0	0	DC11	DC10	0	0	DC21	DC20	0	0	DC31	DC30

BT2–0: The output factor of step-up is switched. Adjust scale factor of the step-up circuit by the voltage used. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

BT2	BT1	BT0	VGH	VGL	Notes*	
0	0	0	5 X Vci1	-3X Vci1	13.75V	-8.25V
0	0	1	5 X Vci1	-4X Vci1	13.75V	-11V
0	1	0	6 X Vci1	-3X Vci1	16.5V	-8.25V
0	1	1	6 X Vci1	-4X Vci1	16.5V	-11V
1	0	0	6 X Vci1	-5X Vci1	16.5V	-13.75V
1	0	1	7 X Vci1	-4X Vci1	19.25V	-11V
1	1	0	Setting disabled			
1	1	1	Setting disabled			

Note. The values in table above are example of nominal upper-limit by register setting when VCI1=2.75V.

DC11-0: The operating frequency in the step-up circuit1 is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

DC11	DC10	Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)
		f(CL1) : f(DCCLK1)	f(DCCLK):f(DCCLK1)
0	0	1:4	1:1
0	1	1:2	1:0.5
1	0	1:1	1:0.25
1	1	Setting disabled	Setting disabled

Note.

1. DCCLK1 is pumping clock for step-up circuit1
2. f(CL1) is horizontal frequency (1 raster-row)

DC21-0: The operating frequency in the step-up circuit 2 is selected.

DC21	DC20	Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)
		f(CL1) : f(DCCLK2)	f(DCCLK) : f(DCCLK2)
0	0	1:2	1:0.5
0	1	1:1	1:0.25
1	0	1:0.5	1:0.125
1	1	1:0.25	1:0.0625

Note. DCCLK2 is pumping clock for step-up circuit2

DC31-0: The operating frequency in the step-up circuit 3 is selected.

DC31	DC30	Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)
		f(CL1) : f(DCCLK3)	f(DCCLK) : f(DCCLK3)
0	0	1:4	1:1
0	1	1:2	1:0.5
1	0	1:1	1:0.25
1	1	Setting disabled	Setting disabled

Note. DCCLK3 is pumping clock for step-up circuit3

9.3.13. Power Control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	DCR_EX	0	DCR2	DCR1	DCR0	0	GVD6	GVD5	GVD4	GVD3	GVD2	GVD1	GVD0

DCR_EX: Input signal selection register for external interface mode. (0: internal operation clock, 1: DOTCLK) Set DCR_EX bit to 1 for DOTCLK to be DCCLK (clock cycle for step-up circuit) source when external interface mode is in use (DM=1).

DCR 2-0: Set clock cycle for step-up circuit in external interface mode. Please set DCR_EX bit to "1" and DCR1-0 value when external interface is in use. In this case, DOTCLK must be input periodically and continuously.

DCR2	DCR1	DCR0	Clock cycle for step-up circuits (DCCLK) in external interface mode	
			18-bit RGB	6-bit RGB
0	0	0	6 dot clock	18 dot clock
0	0	1	8 dot clock	24 dot clock
0	1	0	12 dot clock	36 dot clock
0	1	1	16 dot clock	48 dot clock
1	0	0	24 dot clock	72 dot clock
1	0	1	32 dot clock	96 dot clock
1	1	0	48 dot clock	144 dot clock
1	1	1	64 dot clock	192 dot clock

GVD6-0: Set the amplifying factor of the GVDD voltage (the voltage for the Gamma voltage). It allows ranging from 2.5V to 5.0V.

GVD6-0	GVDD Voltage	GVD6-0	GVDD Voltage
0000000	2.50V	1000000	3.76V
0000001	2.52V	1000001	3.78V
0000010	2.54V	1000010	3.80V
0000011	2.56V	1000011	3.82V
0000100	2.58V	1000100	3.84V
0000101	2.60V	1000101	3.86V
0000110	2.62V	1000110	3.88V
0000111	2.64V	1000111	3.90V
0001000	2.66V	1001000	3.92V
0001001	2.68V	1001001	3.94V
0001010	2.70V	1001010	3.96V
0001011	2.72V	1001011	3.98V
0001100	2.74V	1001100	4.00V
0001101	2.76V	1001101	4.02V
0001110	2.78V	1001110	4.04V
0001111	2.80V	1001111	4.06V
0010000	2.81V	1010000	4.07V
0010001	2.83V	1010001	4.09V
0010010	2.85V	1010010	4.11V
0010011	2.87V	1010011	4.13V
0010100	2.89V	1010100	4.15V

GVD6-0	GVDD Voltage	GVD6-0	GVDD Voltage
0010101	2.91V	1010101	4.17V
0010110	2.93V	1010110	4.19V
0010111	2.95V	1010111	4.21V
0011000	2.97V	1011000	4.23V
0011001	2.99V	1011001	4.25V
0011010	3.01V	1011010	4.27V
0011011	3.03V	1011011	4.29V
0011100	3.05V	1011100	4.31V
0011101	3.07V	1011101	4.33V
0011110	3.09V	1011110	4.35V
0011111	3.11V	1011111	4.37V
0100000	3.13V	1100000	4.39V
0100001	3.15V	1100001	4.41V
0100010	3.17V	1100010	4.43V
0100011	3.19V	1100011	4.45V
0100100	3.21V	1100100	4.47V
0100101	3.23V	1100101	4.49V
0100110	3.25V	1100110	4.51V
0100111	3.27V	1100111	4.53V
0101000	3.29V	1101000	4.55V
0101001	3.31V	1101001	4.57V
0101010	3.33V	1101010	4.59V
0101011	3.35V	1101011	4.61V
0101100	3.37V	1101100	4.63V
0101101	3.39V	1101101	4.65V
0101110	3.41V	1101110	4.67V
0101111	3.43V	1101111	4.69V
0110000	3.44V	1110000	4.70V
0110001	3.46V	1110001	4.72V
0110010	3.48V	1110010	4.74V
0110011	3.50V	1110011	4.76V
0110100	3.52V	1110100	4.78V
0110101	3.54V	1110101	4.80V
0110110	3.56V	1110110	4.82V
0110111	3.58V	1110111	4.84V
0111000	3.60V	1111000	4.86V
0111001	3.62V	1111001	4.88V
0111010	3.64V	1111010	4.90V
0111011	3.66V	1111011	4.92V
0111100	3.68V	1111100	4.94V
0111101	3.70V	1111101	4.96V
0111110	3.72V	1111110	4.98V
0111111	3.74V	1111111	5.00V

Note. Do not set any higher GVDD level than AVDD-0.5V

9.3.14. Power Control 5 (R14h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VCOMG	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCMR	VML6	VML5	VML4	VML3	VML2	VML1	VML0

VCOMG: When VCOMG = 1, low level of VCOM signal is to be fixed at AVSS. Therefore, the amplitude of VCOM signal is determined as |VCOMH – AVSS| regardless of VML setting. In this case, VCOML pin should be connected to GND, because VCOML amp is off and VCOML output is floated.
When VCOMG=0, the amplitude of VCOM signal is determined as |VCOMH – VCOML|.

VCM6-0: Set the VCOMH voltage (a high level voltage at the Vcom alternating drive), these bits amplify the VcomH voltage from 0.4015 to 1.1000 times the GVDD voltage.

Table 39. VCOMH Setting

VCM6-0	VCOMH Output	VCM6-0	VCOMH Output
0000000	GVDD X 0.4015	1000000	GVDD X 0.7535
0000001	GVDD X 0.4070	1000001	GVDD X 0.7590
0000010	GVDD X 0.4125	1000010	GVDD X 0.7645
0000011	GVDD X 0.4180	1000011	GVDD X 0.7700
0000100	GVDD X 0.4235	1000100	GVDD X 0.7755
0000101	GVDD X 0.4290	1000101	GVDD X 0.7810
0000110	GVDD X 0.4345	1000110	GVDD X 0.7865
0000111	GVDD X 0.4400	1000111	GVDD X 0.7920
0001000	GVDD X 0.4455	1001000	GVDD X 0.7975
0001001	GVDD X 0.4510	1001001	GVDD X 0.8030
0001010	GVDD X 0.4565	1001010	GVDD X 0.8085
0001011	GVDD X 0.4620	1001011	GVDD X 0.8140
0001100	GVDD X 0.4675	1001100	GVDD X 0.8195
0001101	GVDD X 0.4730	1001101	GVDD X 0.8250
0001110	GVDD X 0.4785	1001110	GVDD X 0.8305
0001111	GVDD X 0.4840	1001111	GVDD X 0.8360
0010000	GVDD X 0.4895	1010000	GVDD X 0.8415
0010001	GVDD X 0.4950	1010001	GVDD X 0.8470
0010010	GVDD X 0.5005	1010010	GVDD X 0.8525
0010011	GVDD X 0.5060	1010011	GVDD X 0.8580
0010100	GVDD X 0.5115	1010100	GVDD X 0.8635
0010101	GVDD X 0.5170	1010101	GVDD X 0.8690
0010110	GVDD X 0.5225	1010110	GVDD X 0.8745
0010111	GVDD X 0.5280	1010111	GVDD X 0.8800
0011000	GVDD X 0.5335	1011000	GVDD X 0.8855
0011001	GVDD X 0.5390	1011001	GVDD X 0.8910
0011010	GVDD X 0.5445	1011010	GVDD X 0.8965
0011011	GVDD X 0.5500	1011011	GVDD X 0.9020
0011100	GVDD X 0.5555	1011100	GVDD X 0.9075
0011101	GVDD X 0.5610	1011101	GVDD X 0.9130
0011110	GVDD X 0.5665	1011110	GVDD X 0.9185
0011111	GVDD X 0.5720	1011111	GVDD X 0.9240

VCM6-0	VCOMH Output	VCM6-0	VCOMH Output
0100000	GVDD X 0.5775	1100000	GVDD X 0.9295
0100001	GVDD X 0.5830	1100001	GVDD X 0.9350
0100010	GVDD X 0.5885	1100010	GVDD X 0.9405
0100011	GVDD X 0.5940	1100011	GVDD X 0.9460
0100100	GVDD X 0.5995	1100100	GVDD X 0.9515
0100101	GVDD X 0.6050	1100101	GVDD X 0.9570
0100110	GVDD X 0.6105	1100110	GVDD X 0.9625
0100111	GVDD X 0.6160	1100111	GVDD X 0.9680
0101000	GVDD X 0.6215	1101000	GVDD X 0.9735
0101001	GVDD X 0.6270	1101001	GVDD X 0.9790
0101010	GVDD X 0.6325	1101010	GVDD X 0.9845
0101011	GVDD X 0.6380	1101011	GVDD X 0.9900
0101100	GVDD X 0.6435	1101100	GVDD X 0.9955
0101101	GVDD X 0.6490	1101101	GVDD X 1.0010
0101110	GVDD X 0.6545	1101110	GVDD X 1.0065
0101111	GVDD X 0.6600	1101111	GVDD X 1.0120
0110000	GVDD X 0.6655	1110000	GVDD X 1.0175
0110001	GVDD X 0.6710	1110001	GVDD X 1.0230
0110010	GVDD X 0.6765	1110010	GVDD X 1.0285
0110011	GVDD X 0.6820	1110011	GVDD X 1.0340
0110100	GVDD X 0.6875	1110100	GVDD X 1.0395
0110101	GVDD X 0.6930	1110101	GVDD X 1.0450
0110110	GVDD X 0.6985	1110110	GVDD X 1.0505
0110111	GVDD X 0.7040	1110111	GVDD X 1.0560
0111000	GVDD X 0.7095	1111000	GVDD X 1.0615
0111001	GVDD X 0.7150	1111001	GVDD X 1.0670
0111010	GVDD X 0.7205	1111010	GVDD X 1.0725
0111011	GVDD X 0.7260	1111011	GVDD X 1.0780
0111100	GVDD X 0.7315	1111100	GVDD X 1.0835
0111101	GVDD X 0.7370	1111101	GVDD X 1.0890
0111110	GVDD X 0.7425	1111110	GVDD X 1.0945
0111111	GVDD X 0.7480	1111111	GVDD X 1.1000

Note.

VcomH = GVDD x (0.4015 + 0.0055 x VCM)
When using VCI recycling function, VCOMH voltage should be higher than VCI.
TOTAL_VCM [6:0] is VCM [6:0] + VCM_OFFSET_MTP [4:0] when MTP_SEL=0 and is VCM [6:0] + VCM_OFFSET_REG [4:0] when MTP_SEL=1.

VCMR: If VCMR is LOW, VCOMH is adjusted by VCM6-0 register and VCOMR pin is used to monitor the input voltage of the amplifier which outputs the VCOMH voltage.

If VCMR is HIGH, VCM6-0 register is ignored and VCOMH voltage is adjusted by VCOMR voltage. VCOMR voltage is externally supplied. The relationship between VCOMH and VCOMR is given as VCOMH=1.1xVCOMR.

VML6-0: Set the alternating amplitudes of VCOM at the VCOM alternating drive. These bits amplify VCOM from 0.534 to 1.20 times the GVDD voltage. When the VCOM alternation is not driven, the settings become invalid.

Table 40. VCOM Amplitude Control

VML[6:0]	VCOM Amplitude	VML[6:0]	VCOM Amplitude
0000000	Setting disable	1000111	GVDD X 0.864
…	Setting disable	1001000	GVDD X 0.870
0001111	Setting disable	1001001	GVDD X 0.876
0010000	GVDD X 0.534	1001010	GVDD X 0.882
0010001	GVDD X 0.540	1001011	GVDD X 0.888
0010010	GVDD X 0.546	1001100	GVDD X 0.894
0010011	GVDD X 0.552	1001101	GVDD X 0.900
0010100	GVDD X 0.558	1001110	GVDD X 0.906
0010101	GVDD X 0.564	1001111	GVDD X 0.912
0010110	GVDD X 0.570	1010000	GVDD X 0.918
0010111	GVDD X 0.576	1010001	GVDD X 0.924
0011000	GVDD X 0.582	1010010	GVDD X 0.930
0011001	GVDD X 0.588	1010011	GVDD X 0.936
0011010	GVDD X 0.594	1010100	GVDD X 0.942
0011011	GVDD X 0.600	1010101	GVDD X 0.948
0011100	GVDD X 0.606	1010110	GVDD X 0.954
0011101	GVDD X 0.612	1010111	GVDD X 0.960
0011110	GVDD X 0.618	1011000	GVDD X 0.966
0011111	GVDD X 0.624	1011001	GVDD X 0.972
0100000	GVDD X 0.630	1011010	GVDD X 0.978
0100001	GVDD X 0.636	1011011	GVDD X 0.984
0100010	GVDD X 0.642	1011100	GVDD X 0.990
0100011	GVDD X 0.648	1011101	GVDD X 0.996
0100100	GVDD X 0.654	1011110	GVDD X 1.002
0100101	GVDD X 0.660	1011111	GVDD X 1.008
0100110	GVDD X 0.666	1100000	GVDD X 1.014
0100111	GVDD X 0.672	1100001	GVDD X 1.020
0101000	GVDD X 0.678	1100010	GVDD X 1.026
0101001	GVDD X 0.684	1100011	GVDD X 1.032
0101010	GVDD X 0.690	1100100	GVDD X 1.038
0101011	GVDD X 0.696	1100101	GVDD X 1.044
0101100	GVDD X 0.702	1100110	GVDD X 1.050
0101101	GVDD X 0.708	1100111	GVDD X 1.056
0101110	GVDD X 0.714	1101000	GVDD X 1.062
0101111	GVDD X 0.720	1101001	GVDD X 1.068
0110000	GVDD X 0.726	1101010	GVDD X 1.074
0110001	GVDD X 0.732	1101011	GVDD X 1.080
0110010	GVDD X 0.738	1101100	GVDD X 1.086
0110011	GVDD X 0.744	1101101	GVDD X 1.092
0110100	GVDD X 0.750	1101110	GVDD X 1.098
0110101	GVDD X 0.756	1101111	GVDD X 1.104
0110110	GVDD X 0.762	1110000	GVDD X 1.110

VML[6:0]	VCOM Amplitude	VML[6:0]	VCOM Amplitude
0110111	GVDD X 0.768	1110001	GVDD X 1.116
0111000	GVDD X 0.774	1110010	GVDD X 1.122
0111001	GVDD X 0.780	1110011	GVDD X 1.128
0111010	GVDD X 0.786	1110100	GVDD X 1.134
0111011	GVDD X 0.792	1110101	GVDD X 1.140
0111100	GVDD X 0.798	1110110	GVDD X 1.146
0111101	GVDD X 0.804	1110111	GVDD X 1.152
0111110	GVDD X 0.810	1111000	GVDD X 1.158
0111111	GVDD X 0.816	1111001	GVDD X 1.164
1000000	GVDD X 0.822	1111010	GVDD X 1.170
1000001	GVDD X 0.828	1111011	GVDD X 1.176
1000010	GVDD X 0.834	1111100	GVDD X 1.182
1000011	GVDD X 0.840	1111101	GVDD X 1.188
1000100	GVDD X 0.846	1111110	GVDD X 1.194
1000101	GVDD X 0.852	1111111	GVDD X 1.200
1000110	GVDD X 0.858		

Note.

Adjust the settings between GVDD and VML6-0 so that the VCOM amplitudes are lower than 6.0 V.

VCOML voltage should be satisfied the following condition. : 0.0V > VCOML > VCL+0.5V.

VCOM amplitude = GVDD x (0.534 + 0.006(VDV-16))

9.3.15. VCI Recycling (R15h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	VCIR2	VCIR1	VCIR0	0	0	0	0

VCIR2-0: VCI recycling period is sustained for the number of clock cycle which is set on VCIR2-0.

VCIR2	VCIR1	VCIR0	Period of VCIR recycling			
			VCI recycling period. (Synchronized with OSC clock) * unit : clock cycle			RGB I/F operation (Synchronized with DOTCLK)
			Sn	Vcom1	Vcom2	
0	0	0	Off			Off
0	0	1	setting disable			Setting disable
0	1	0	2	1 / 2	2 / 1	16 dot clock
0	1	1	3	1.5 / 3	3 / 1.5	32 dot clock
1	0	0	4	2 / 4	4 / 2	48 dot clock
1	0	1	5	2.5 / 5	5 / 2.5	64 dot clock
1	1	0	6	3 / 6	6 / 3	80 dot clock
1	1	1	7	3.5 / 7	7 / 3.5	96 dot clock

Note. When VCI Recycling is used, VCOMH level must be larger than VCI level.

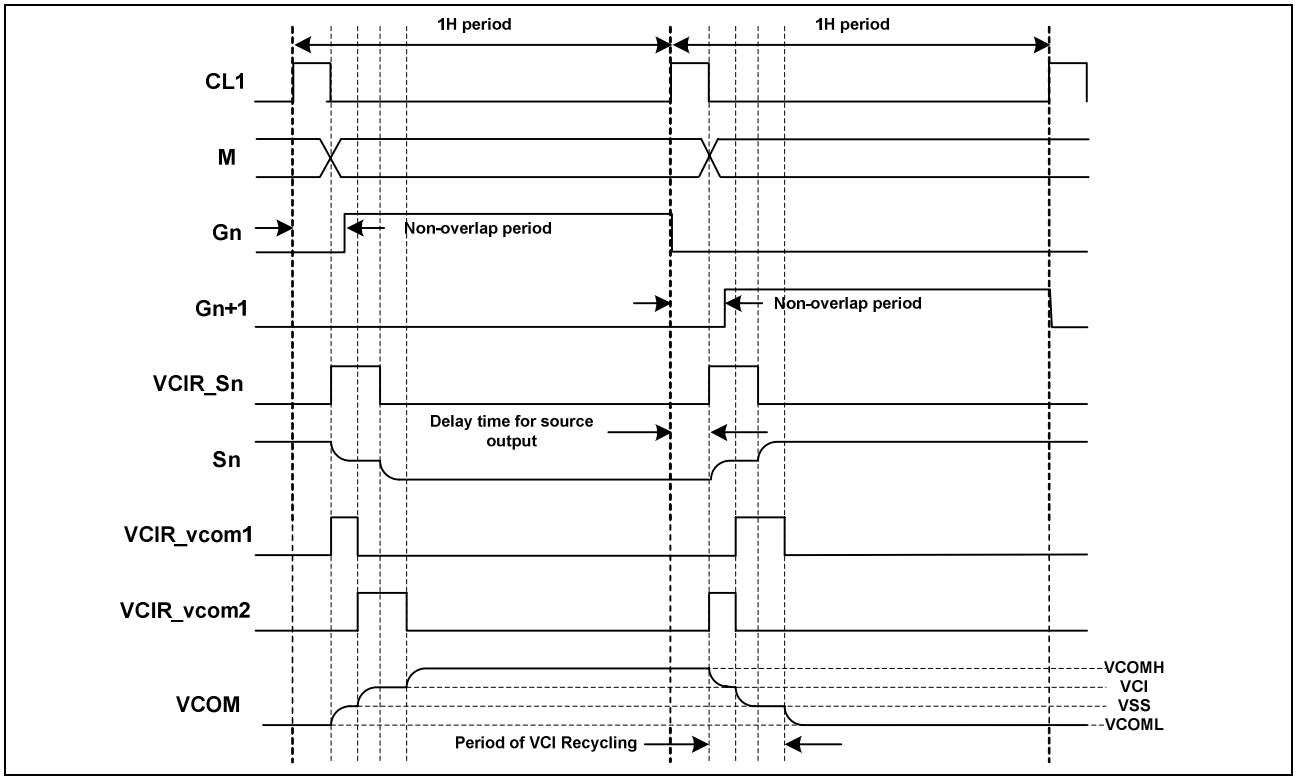


Figure 27. Set Delay From Gate Output To Source Output And VCIR Signal

9.3.16. GRAM Address Set (R20h,R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD

You can write initial GRAM address into internal Address Counter (AC). When GRAM data is transferred through System Interface or RGB Interface, the AC is automatically updated according to AM and ID. This allows consecutive write without re-setting address in AC. But when GRAM data is read, the AC is not automatically updated.

GRAM address setting is not allowed in Standby mode. Ensure that the address is set within the specified window area specified with VSA, VEA, HSA and HEA.

When RGB interface is used (RM="1") to access GRAM, AD [16:0] will be set in the address counter at the falling edge of the VSYNC signal. And when one uses System Interface to access GRAM (RM = "0"), AD [16:0] will be set upon the execution of an instruction.

Table 41. GRAM Address Range

AD[16:0]	GRAM setting
"00000H" to "000EF"H	Bitmap data for G1
"00100H" to "001EF"H	Bitmap data for G2
"00200H" to "002EF"H	Bitmap data for G3
"00300H" to "003EF"H	Bitmap data for G4
:	:
"13C00H" to "13CEF"H	Bitmap data for G317
"13D00H" to "13DEF"H	Bitmap data for G318
"13E00H" to "13EEF"H	Bitmap data for G319
"13F00H" to "13FEF"H	Bitmap data for G320

9.3.17. Write Data to GRAM (R22h)

R/W	RS	
W	1	RAM write data (WD17 ~ WD0). ※Interface mode controls the width of WD

WDR

Data on DB bus is expanded to 18-bits before being written to GRAM and the data determines grayscale level of S6D0154's source output. Please keep in mind that the expansion format varies with interface mode. GRAM cannot be accessed in Standby mode. When data is written to GRAM via system interface while another data is being written to through RGB interface, please make sure that the two write operations does not conflict.

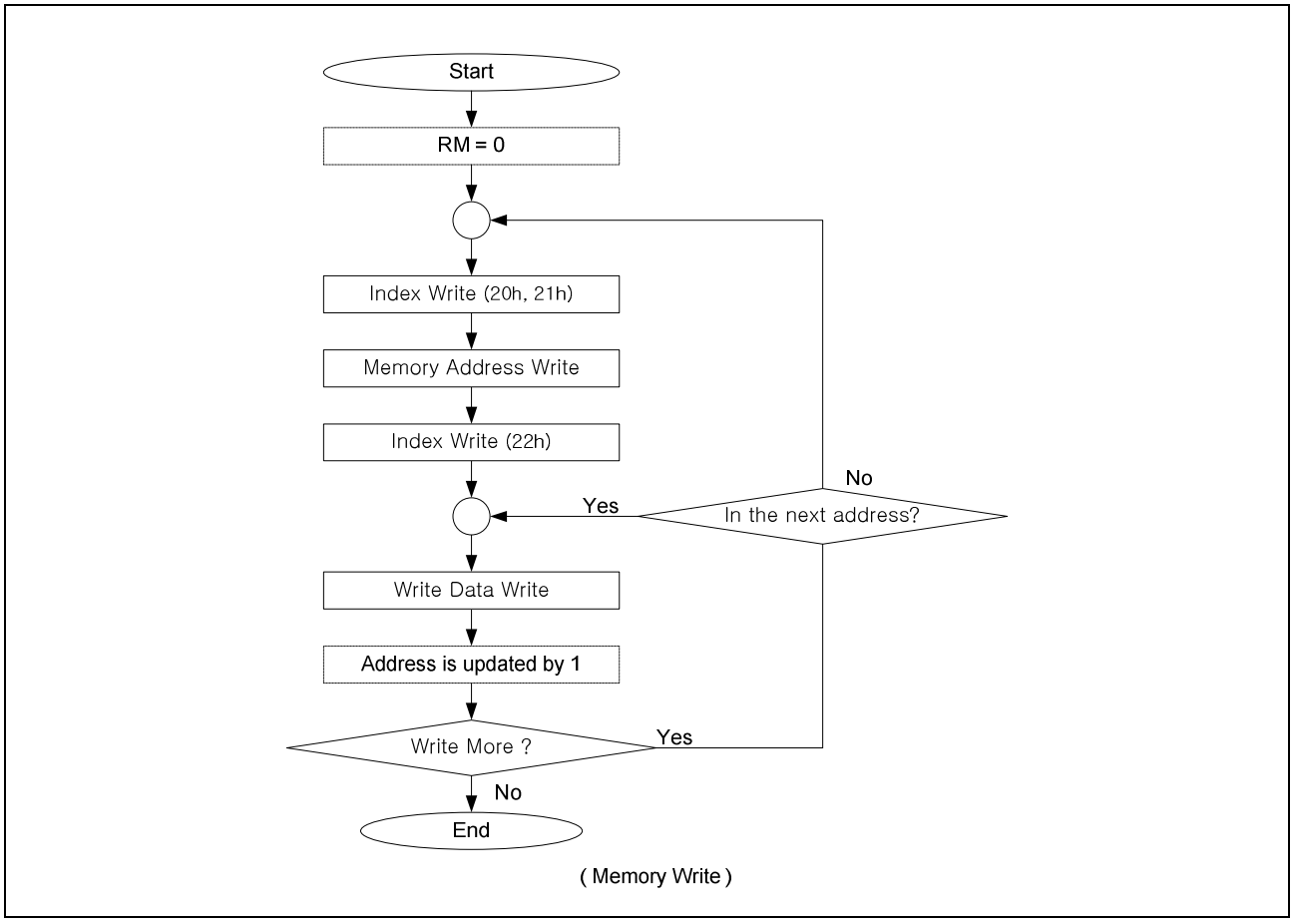


Figure 28. Memory Data Write Sequence

9.3.18. Read Data from GRAM (R22h)

R/W	RS	
R	1	RAM read data (RD17 ~ RD0). ※Interface mode controls the width of RD

RDR

You may read data from GRAM using this register. When you make read operations, you can get a proper data on the second read operation as shown below. The first word you get just after address setting may be invalid.

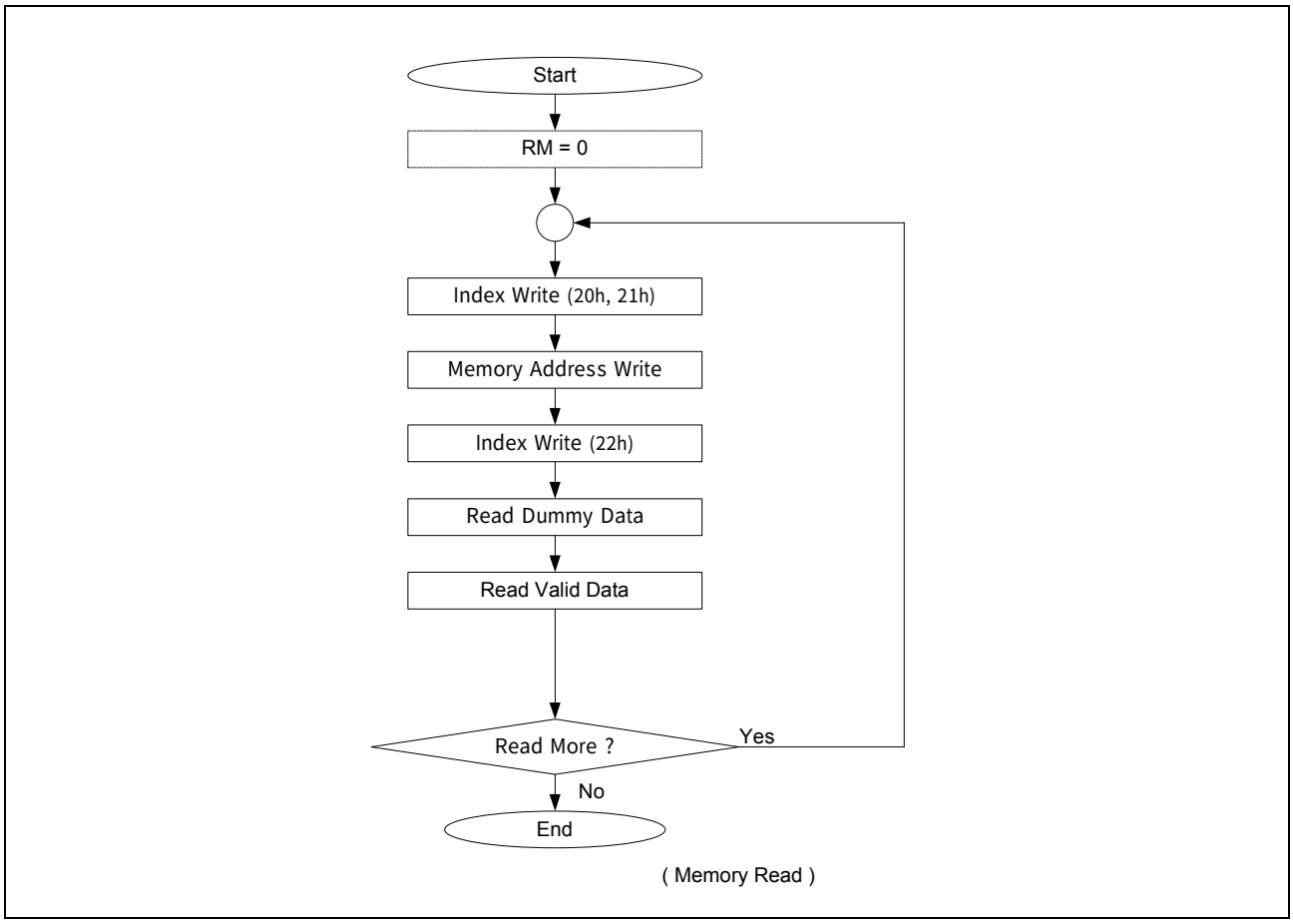


Figure 29. Memory Data Read Sequence

9.3.19. Software Reset (R28h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0

When Software Reset parameter is 00CEh, It cause a software reset. This register automatically set to high after a Software Reset.

9.3.20. FLM Function (R29h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	FLM _INT1	FLM _INT0	0	0	0	0	FLM _POS8	FLM _POS7	FLM _POS6	FLM _POS5	FLM _POS4	FLM _POS3	FLM _POS2	FLM _POS1	FLM _POS0

FLM_POS8-0: The S6D0154 outputs an FLM pulse when the S6D0154 is driving the line specified by FLM_POS [8:0] bits. The FLM signal can be used as a trigger signal to write display data in synchronization with display operation by detecting the address where data is read out for display operation.

FLM_POS[8:0]	FLM Output Position
9'h000	0
9'h001	1st line
9'h002	2nd line
. . .	. . .
9'h14D	333rd line
9'h14E	334th line
9'h14F	335th line
9'h150 ~ 1FF	Setting disabled

FLM_INT1-0: The FLM output interval is set by FLM_INT [2:0] bits. Set FLM_INT [2:0] bits in accordance with display data rewrite cycle and data transfer rate.

FLM_INT[1]	FLM_INT[0]	FLM Output Position
0	0	One frame period
0	1	2 frame periods
1	0	4 frame periods
1	1	8 frame periods
Other setting		Setting disabled

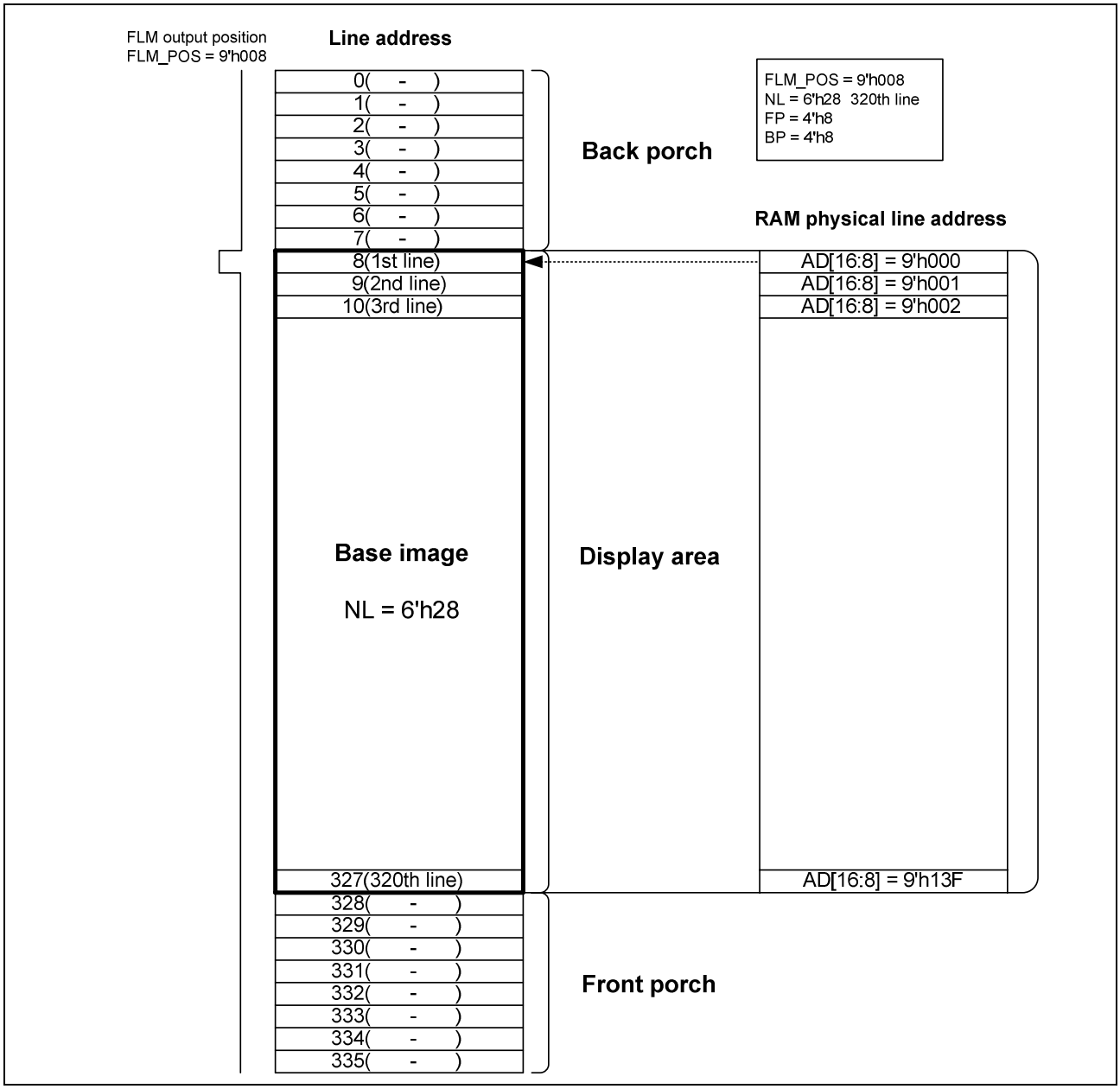


Figure 30. FLM_POS Setting

9.3.21. Gate Scan Position (R30h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

SCN5-0: Set the scanning start position of the gate driver.

SCN5-0	Start Position	
	GS=0	GS=1
000000	G1	G320
000001	G9	G312
000010	G17	G304
---	---	---
100101	G297	G24
100110	G305	G16
100111	G313	G8

Note. Ensure that gate start position (SCN) + the number of LCD driver lines (NL) ≤ 320 when GS = 0, and that gate start position (SCN) - the number of LCD driver lines (NL) ≥ 0 when GS = 1

* Initial Value: SCN5-0 = 000000

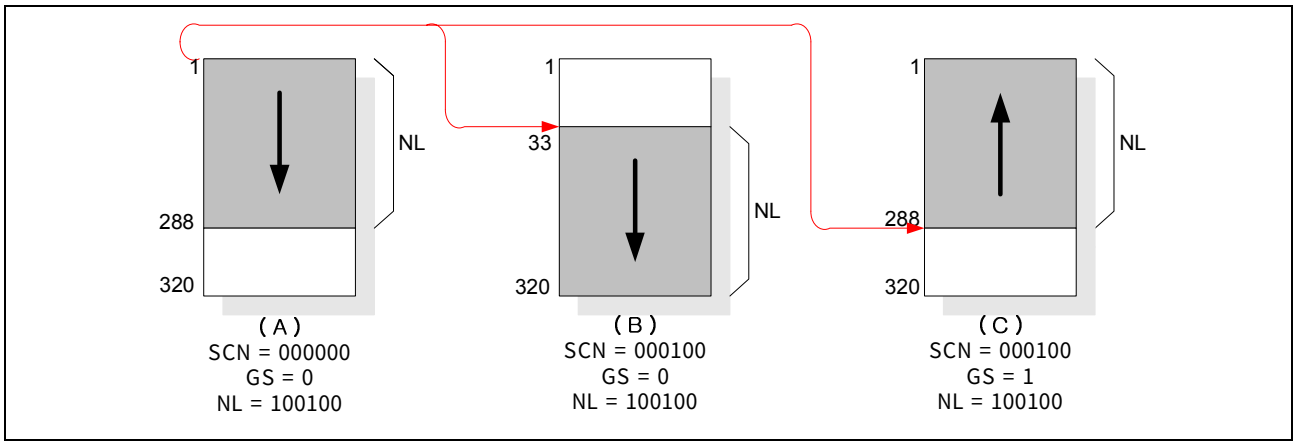


Figure 31. Gate Scan Position Control

9.3.22. Vertical Scroll Control 1 (R31h, R32h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SEA 8	SEA 7	SEA 6	SEA 5	SEA 4	SEA 3	SEA 2	SEA 1	SEA 0
W	1	0	0	0	0	0	0	0	SSA 8	SSA 7	SSA 6	SSA 5	SSA 4	SSA 3	SSA 2	SSA 1	SSA 0

SSA8-0: Specify scroll start address at the scroll display for vertical smooth scrolling.

SSA8	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	Scroll Start Address
0	0	0	0	0	0	0	0	0	0 raster-row
0	0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	0	1	0	2 raster-row
0	0	0	0	0	0	0	1	1	3 raster-row
0	0	0	0	0	0	1	0	0	4 raster-row
0	0	0	0	0	0	1	0	1	5 raster-row
:	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	0	0	316 raster-row
1	0	0	1	1	1	1	0	1	317 raster-row
1	0	0	1	1	1	1	1	0	318 raster-row
1	0	0	1	1	1	1	1	1	319 raster-row

SEA8-0: Specify scroll end address at the scroll display for vertical smooth scrolling.

SEA8	SEA7	SEA6	SEA5	SEA4	SEA3	SEA2	SEA1	SEA0	Scroll End Address
0	0	0	0	0	0	0	0	0	0 raster-row
0	0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	0	1	0	2 raster-row
0	0	0	0	0	0	0	1	1	3 raster-row
0	0	0	0	0	0	1	0	0	4 raster-row
0	0	0	0	0	0	1	0	1	5 raster-row
:	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	0	0	316 raster-row
1	0	0	1	1	1	1	0	1	317 raster-row
1	0	0	1	1	1	1	1	0	318 raster-row
1	0	0	1	1	1	1	1	1	319 raster-row

Note.

1. Do not set any higher raster-row than 319 (“13F”H).
2. Set SS18-10 ≤ SSA8-0, if set out of range, SSA8-0 = SS18-10.
3. Set SE18-10 ≥ SEA8-0, if set out of range, SEA8-0 = SE18-10

9.3.23. Vertical Scroll Control 2 (R33h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SST 8	SST 7	SST 6	SST 5	SST 4	SST 3	SST 2	SST 1	SST 0

SST8-0: Specify scroll start and step at the scroll display for vertical smooth scrolling. Any raster-row from the 1st to 320th can be scrolled for the number of the raster-row. After 219th raster-row is displayed, the display restarts from the first raster-row. When SST7-0 = 00000000, Vertical Scroll Function is disabled.

SST8	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0	Scroll Step
0	0	0	0	0	0	0	0	0	0 raster-row
0	0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	0	1	0	2 raster-row
0	0	0	0	0	0	0	1	1	3 raster-row
0	0	0	0	0	0	1	0	0	4 raster-row
0	0	0	0	0	0	1	0	1	5 raster-row
:	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	0	0	316 raster-row
1	0	0	1	1	1	1	0	1	317 raster-row
1	0	0	1	1	1	1	1	0	318 raster-row
1	0	0	1	1	1	1	1	1	319 raster-row

Note.

Do not set any higher raster-row than 319 (“13F”H)

Set SS18-10 < SSA8-0 + SST8-0 ≤ SEA8-0 ≤ SE18-10, if set out of range, Scroll function is disabled

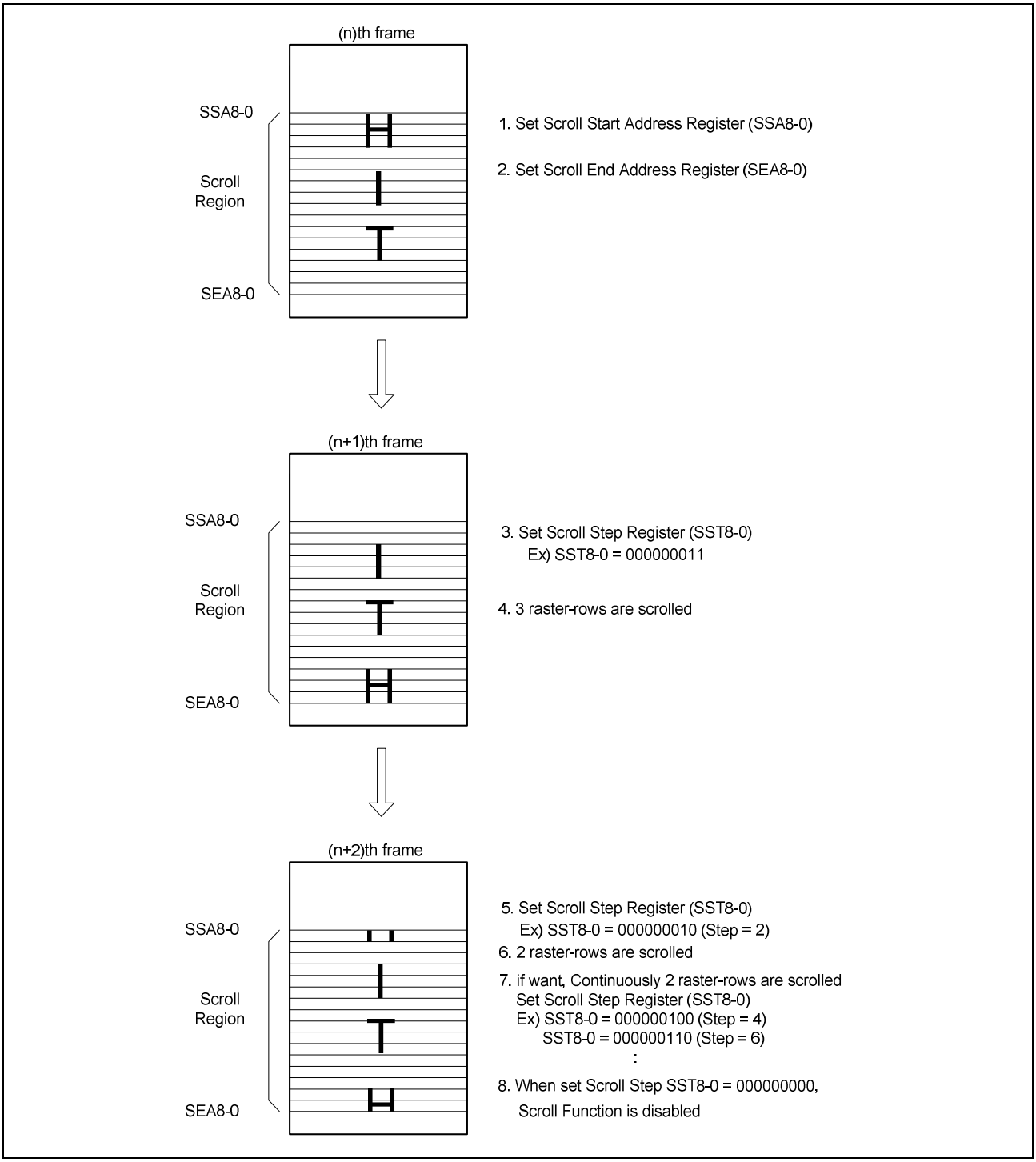


Figure 32. Vertical Scroll Display

9.3.24. Partial Screen Driving Position (R34h, R35h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
W	1	0	0	0	0	0	0	0	SS17	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10

SE18–10: Specify the driving end position for the screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For instance, when SS18–10 = 019h and SE18–10 = 029h are set, the LCD driving is performed from G26 to G42, and non-display driving is performed for G1 to G25, G43, and others. Ensure that SS18–10 ≦ SE18–10 ≦ 13Fh.

SS18–10: Specify the drive starting position for the first screen in a line unit. The LCD driving starts from the 'set value +1' gate driver.

Note. Do not set the partial setting when the operation is in the normal display condition. Set this register only when in the partial display condition.

Ex) SS8-0=007h and SE8-0=010h are performed from G8 to G17.

The S6D0154 can select and drive partial screens at any position with the screen-driving position registers (R34H, R35H). Any partial screens required for display are selectively driven and reducing LCD-driving voltage and power consumption.

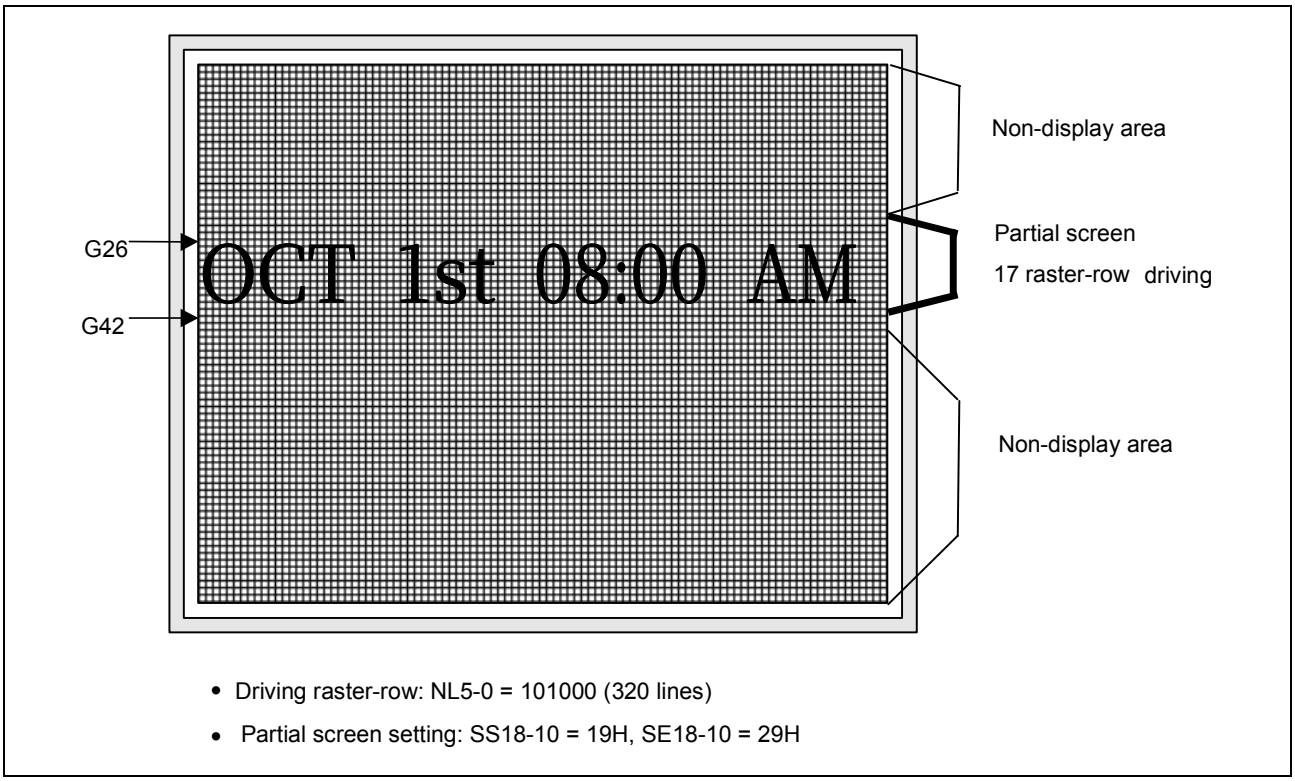


Figure 33. Driving On Partial Screen

9.3.25. Horizontal RAM Address Position (R36h, R37h)

9.3.26. Vertical RAM Address Position (R38h, R39h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	HEA8	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HEA 2	HEA 1	HEA 0
W	1	0	0	0	0	0	0	0	HSA8	HSA 7	HSA 6	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0
W	1	0	0	0	0	0	0	0	VEA8	VEA 7	VEA 6	VEA 5	VEA 4	VEA 3	VEA 2	VEA 1	VEA 0
W	1	0	0	0	0	0	0	0	VSA8	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

HSA8-0/HEA8-0: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by HSA8-0 to the address specified by HEA8-0. Note that an address must be set before RAM is written..

VSA8-0/VEA8-0: Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by VSA8-0 to the address specified by VEA8-0. Note that an address must be set before RAM is written.

When AM=0, 00h ≤ HSA8-0 ≤ HEA8-0 ≤ EFh and 00h ≤ VSA8-0 ≤ VEA8-0 ≤ 13Fh

AM=1, 00h ≤ HSA8-0 ≤ HEA8-0 ≤ 13Fh and 00h ≤ VSA8-0 ≤ VEA8-0 ≤ EFh

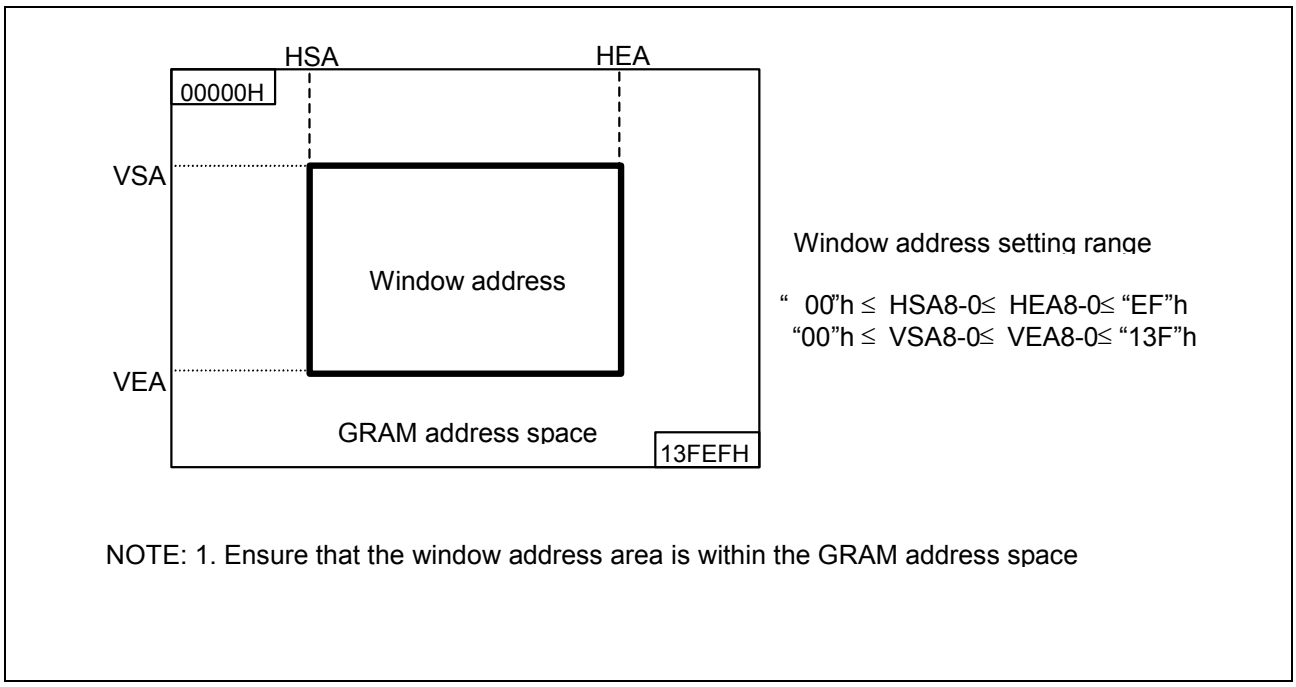


Figure 34. Window Address Setting Range (AM=0)

9.3.27. Gamma Control (R50h to R59h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	PKP 13	PKP 12	PKP 11	PKP 10	0	0	0	0	PKP 03	PKP 02	PKP 01	PKP 00
W	1	0	0	0	0	PKP 33	PKP 32	PKP 31	PKP 30	0	0	0	0	PKP 23	PKP 22	PKP 21	PKP 20
W	1	0	0	0	0	PKP 53	PKP 52	PKP 51	PKP 50	0	0	0	0	PKP 43	PKP 42	PKP 41	PKP 40
W	1	0	0	0	0	PRP 13	PRP 12	PRP 11	PRP 10	0	0	0	0	PRP 03	PRP 02	PRP 01	PRP 00
W	1	0	0	0	0	PKN 13	PKN 12	PKN 11	PKN 10	0	0	0	0	PKN 03	PKN 02	PKN 01	PKN 00
W	1	0	0	0	0	PKN 33	PKN 32	PKN 31	PKN 30	0	0	0	0	PKN 23	PKN 22	PKN 21	PKN 20
W	1	0	0	0	0	PKN 53	PKN 52	PKN 51	PKN 50	0	0	0	0	PKN 43	PKN 42	PKN 41	PKN 40
W	1	0	0	0	0	PRN 13	PRN 12	PRN 11	PRN 10	0	0	0	0	PRN 03	PRN 02	PRN 01	PRN 00
W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	VRP 04	VRP 03	VRP 02	VRP 01	VRP 00
W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	VRN 04	VRN 03	VRN 02	VRN 01	VRN 00

PKP53–00: The gamma fine adjustment registers for the positive polarity output

* Initial Value: PKP53-00 = 0000

PRP13-00: The gradient adjustment registers for the positive polarity output

* Initial Value: PRP13-00 = 0000

PKN53-00: The gamma fine adjustment registers for the negative polarity output

* Initial Value: PKN53-00 = 0000

PRN13-00: The gradient adjustment registers for the negative polarity output

* Initial Value: PRN13-00 = 0000

VRP14-00: The amplitude adjustment registers for the positive polarity output

* Initial Value: VRP14-00 = 00000

VRN14-00: The amplitude adjustment registers for the negative polarity output

* Initial Value: VRN14-00 = 00000

For details, see the GAMMA ADJUSTMENT FUNCTION.

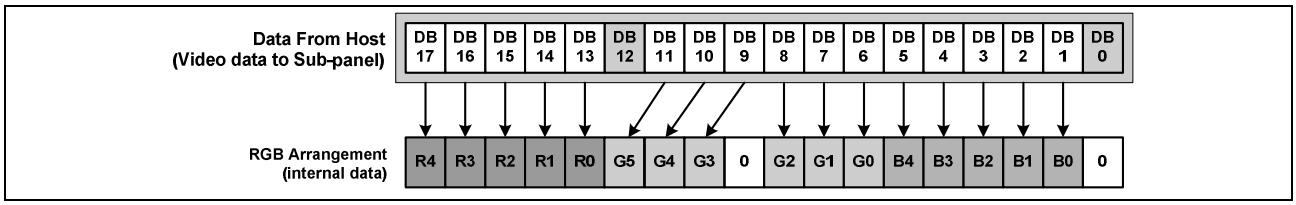
9.3.28. Sub Panel Control (R40h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	FCV_EN	0	MPU_MODE	STN_EN	SUB_IM1	SUB_IM0	0	VWAKE_EN

FCV_EN: data format conversion enable signal

FCV_EN	Description
0	Current 18-bit or 16-bit data format
1	16-bit data format conversion

When FCV_EN=1, convert 18-bit data to 16-bit data as below.



MPU_MODE: set the MPU interface

MPU_MODE	Description
0	80 mode
1	68 mode

STN_EN: set the panel property

STN_EN	Description
0	“TFT” panel
1	“STN” panel

SUB_IM1-0: set the sub-panel interface

SUB_IM1	SUB_IM0	Interface
0	0	Setting Disable
0	1	9bit
1	0	Setting Disable
1	1	8bit

VWAKE_EN: When VWAKE_EN is 1, client initiated wake-up is enabled. But parameter data IB [15:1] must be “0000h”, otherwise, client initiated wake-up is disabled.

9.3.29. MDDI Link Wake-up Start Position (R41h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	WKL 8	WKL 7	WKL 6	WKL 5	WKL 4	WKL 3	WKL 2	WKL 1	WKL 0	0	WKF 3	WKF 2	WKF 1	WKF 0	0	0

WKL8-0: When client initiated wakeup is used at MDDI, data is updated at the line defined by the value of WKL7-0 in the frame that is set by WKF3-0. The range of WKL is from '000h' to '1FFh'.
If WKL is '000h', data is updated at the first line, and if WKL is '1FFh', data update starts at the 256th line.

WKF3-0: When client initiated wake-up is used at MDDI, the frame position that data is updated is set by the value of WKF 3-0. The range of WKF is from '0000' to '1111'.
If WKF is '0000', data is updated at the first frame, and if "1111" data update starts after 16th frame.

Setting of WFK and WKL is needed for client-initiated link wake-up.
For example, WKF is "0010" and WKL is "0001", data is updated at second line of third frame.

9.3.30. Sub Panel Control(R42h / R43h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	SUB_SEL							
W	1	0	0	0	0	0	0	0	0	SUB_WR							

SUB_SEL: SUB_SEL is the index of main/sub panel selection. Initial value of SUB_SEL is '4Ah'.
In MDDI mode, If written register address is '4Ah' (initial state: SUB_SEL is '4Ah') and register data is '0001h', then main panel is selected, and if that is "0000h", then sub panel is selected.
Using SUB_SEL register, Main / Sub panel selection index change is possible.

SUB_WR: SUB_WR is the index of sub panel data write. Initial value of SUB_WR is '22h'.
When MDDI host transfer GRAM data to sub panel driver IC via video stream packet, SUB_WR (initially 22h), index for GRAM access is automatically transferred before GRAM data transfer.
When sub panel driver IC uses other address, 22h address have to be changed. Then user can change SUB_WR value from 22h to other value.

9.3.31. GPIO CONTROL (R44h / R45h / R46h / R47h / R48h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
W	1	0	0	0	0	0	0	0	0	0	0	GPIO_CON5	GPIO_CON4	GPIO_CON3	GPIO_CON2	GPIO_CON1	GPIO_CON0
W	1	0	0	0	0	0	0	0	0	0	0	GPCLR5	GPCLR4	GPCLR3	GPCLR2	GPCLR1	GPCLR0
W	1	0	0	0	0	0	0	0	0	0	0	GPIO_EN5	GPIO_EN4	GPIO_EN3	GPIO_EN2	GPIO_EN1	GPIO_EN0
W	1	0	0	0	0	0	0	0	0	0	0	GPPOL5	GPPOL4	GPPOL3	GPPOL2	GPPOL1	GPPOL0

GPIO: GPIO value. When GPIO is input mode, GPIO value is set to the register.

GPIO_CON: Control of GPIO, When GPIO_CON is “0”, then GPIO is input mode, and when “1”, then GPIO is output mode

GPCLR: After client is wakeup, GPIO

GPIO_EN: When GPIO is set input, if GPIO_EN is “1”, it acts as enable internal interrupt.

GPPOL: If the bit is set to “1”, GPIO interrupt happens at rising edge of GPAD, If set to “0”, it happens at falling edge.

For more information about these registers, refer to GPIO CONTROL section

9.3.32. TEST_KEY (R80h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	TEST_KEY[7:0]							

TEST_KEY

When you want to update MTP data, “8C” should be written to this register. And you should write different value for MTP data not to be corrupted.

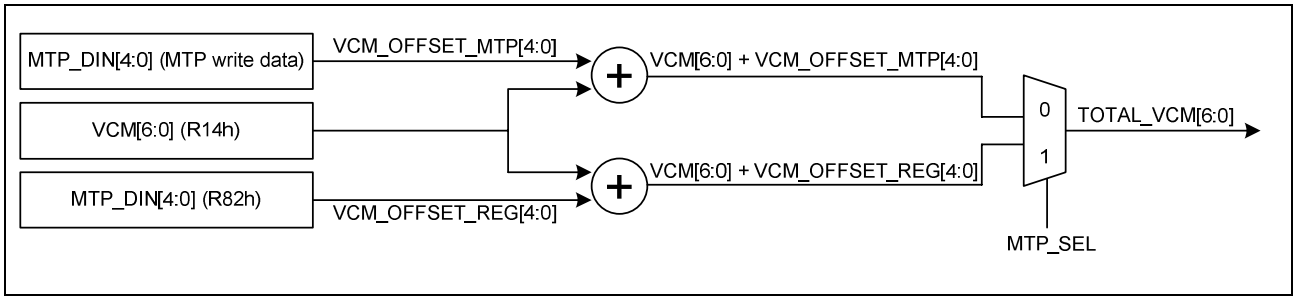
9.3.33. MTP Control (R81h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	MTP_ MODE	MTP _EX	0	MTP_ SEL	0	0	0	MTP_ ERB	0	0	0	MTP_ WRB	0	0	0	MTP_ LOAD

MTP_SEL: Select the VCOMH voltage setting register.

VCM [6:0]: Set the VCOMH voltage

MTP_SEL	VCOMH Control Data
0	VCM [6:0] Register + VCM_OFFSET_MTP4:0]
1	VCM[6:0] Register + VCM_OFFSET_REG[4:0]



MTP_MODE: Set the 2nd booster operating condition.

MTP_MODE = 0: The 2nd booster operates as a user-specified condition. VGH/VGL voltages are generated as a designated level by BT2-0 setting.

MTP_MODE = 1: Available BT2-0 settings are limited only '010' & '101'.

MTP_MODE	MTP operation mode
0	All BT2-0 settings are available (Normal operating condition)
1	Setting of BT2-0 is limited. (An MTP-programming / erasing condition)

Note. Do not execute MTP programming / erasing operation when MTP_MODE = 0.

MTP_EX: Select MTP power supply source.

MTP_EX = 0: Internally generated VGH voltage is used as a MTP-programming/erasing potential.

MTP_EX = 1: External power should be applied for programming / erasing MTP via VGH pad.

MTP_EX	Erase / Initial / Program supply
0	Used internally generated VGH
1	Needed external power supply

Note. MTP_EX register is valid only in case that MTP_MODE = 1. Do not access MTP_EX register when MTP_MODE = 0.

MTP_ERB: Enable for MTP initial or erase. When MTP_ERB = 0, MTP initialization or erase is enabled.

MTP_WRB: MTP Write enable signal. If you want to write data to MTP cell, set MTP_WRB = 0

MTP_LOAD: When MTP_LOAD is High, MTP data is loaded into internal register.

9.3.34. MTP Data Write (R82h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	GPI3	GPI2	GPI1	GPI0	0	0	0	MTP _DIN4	MTP _DIN3	MTP _DIN2	MTP _DIN1	MTP _DIN0
R	1	X	X	X	X	X	X	GPI3	GPI2	GPI1	GPI0	MTP_ DOUT5	MTP_ DOUT4	MTP_ DOUT3	MTP_ DOUT2	MTP_ DOUT1	MTP_ DOUT0

GPI3-0: These inputs are configured based upon glass size and type.

GPI[3:0]	Glass size and Type
0000	2.0” display (for reference only)
0001	2.1” display (for reference only)
0010	2.4” display (for reference only)
0011	2.0” Landscape display, Identifies this display

MTP_DIN

MTP_DIN [5:0] contain VCM Offset data. This MTP data and VCM register determines VCOMH level.

TOTAL_VCM [6:0] = VCM [6:0] + VCM_OFFSET.

MTP_DIN[4:0]	VCM_OFFSET	MTP_DIN[4:0]	VCM_OFFSET
00000	0	10000	0
00001	+1	10001	-1
00010	+2	10010	-2
00011	+3	10011	-3
00100	+4	10100	-4
00101	+5	10101	-5
00110	+6	10110	-6
00111	+7	10111	-7
01000	+8	11000	-8
01001	+9	11001	-9
01010	+10	11010	-10
01011	+11	11011	-11
01100	+12	11100	-12
01101	+13	11101	-13
01110	+14	11110	-14
01111	+15	11111	-15

For example, if VCM [6:0] = 0001011 and MTP_DIN [4:0] = 10001 is selected, then MTP_OFFSET is “-1”, and therefore TOTAL_VCM is “0001010”, which results in VCOMH voltage = 2.697 from VCM6-0 table.

Note that TOTAL_VCM [6:0] cannot be set to the value above “1111111” or below “0000000”, that is, 127 ≥ VCM [6:0] + VCM_OFFSET ≥ 0.

Note. TOTAL_VCM [6:0] is VCM [6:0] + VCM_OFFSET_MTP [4:0] when MTP_SEL=0 and is VCM [6:0] + VCM_OFFSET_REG [4:0] when MTP_SEL=1.

MTP_DOUT: Data of MTP Output

This command reads the VCOM MTP values, MTP_DOUT<5:0> bits. The MSB bit, MTP_DOUT5, protects re-write the MTP, when any bit of MTP is written, MSB bit is changed from low to high automatically.

Once MSB bit sets to be high, MTP cannot be written. To re-write the MTP, need initialization to set MTP_DOUT5 bit to be low.

MTP Control in Internal Mode

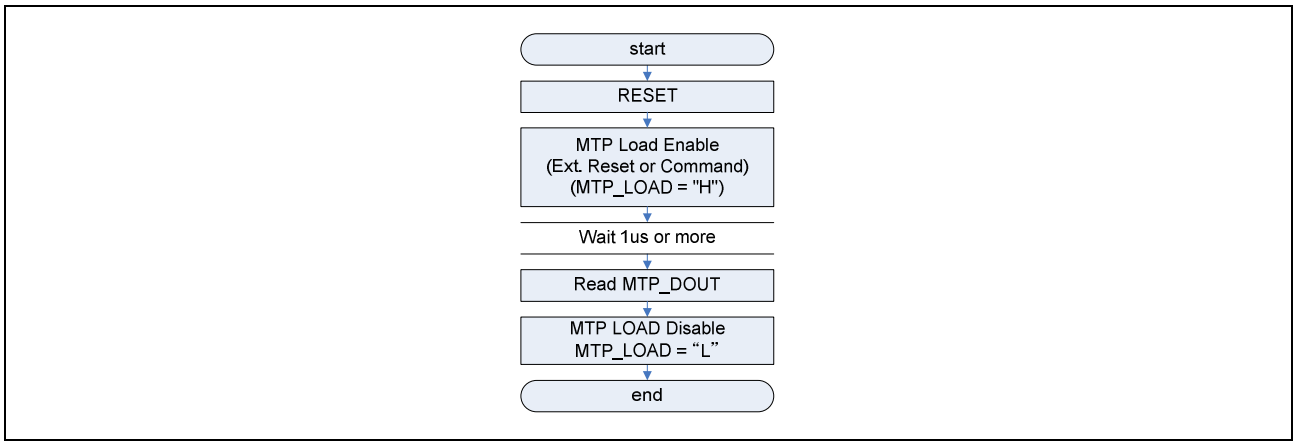


Figure 35. Flow of MTP Load / Read

a. Using VCI for MTP

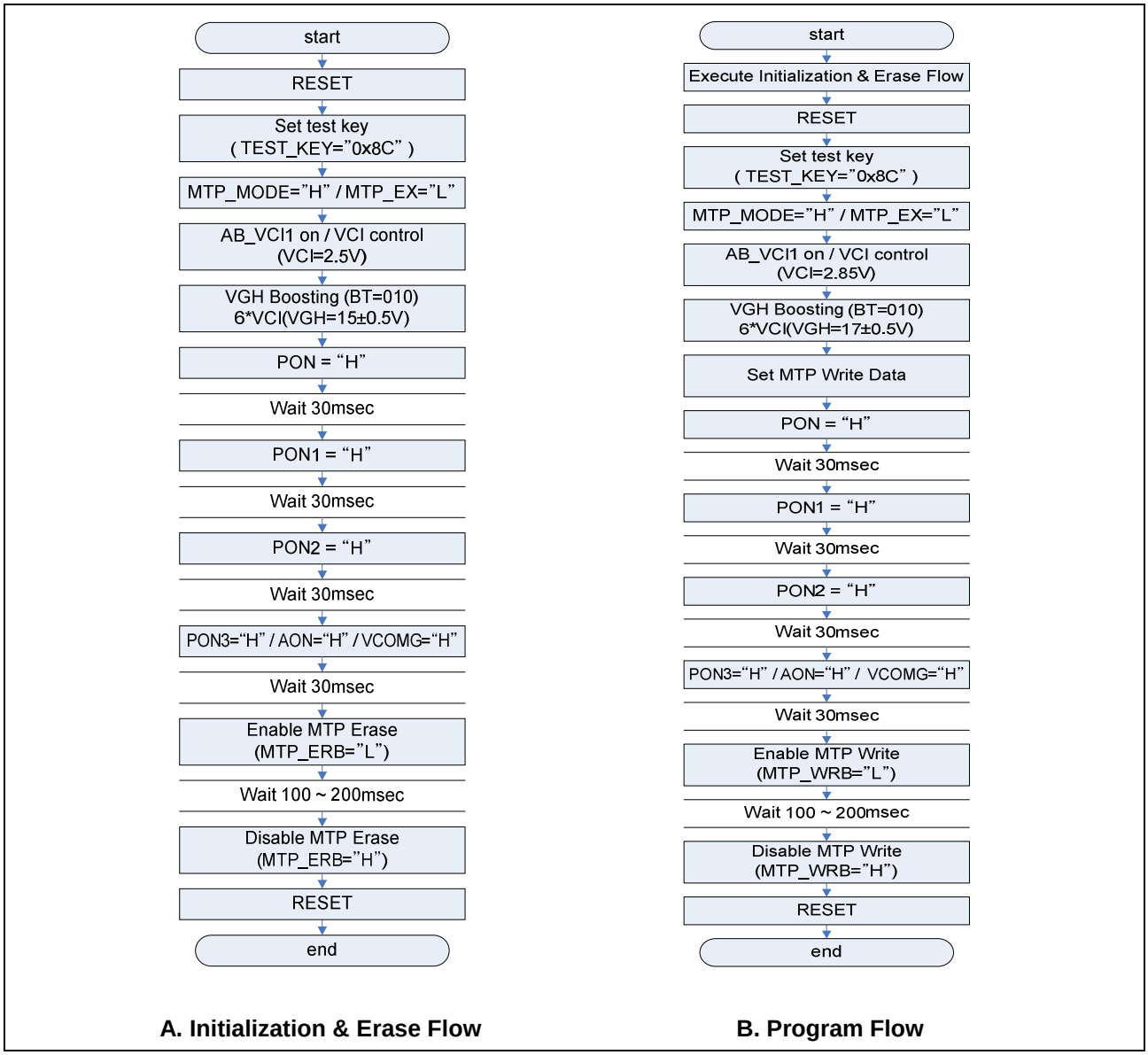


Figure 36. MTP Initialization, Erase and program

b. Using VCI1 for MTP

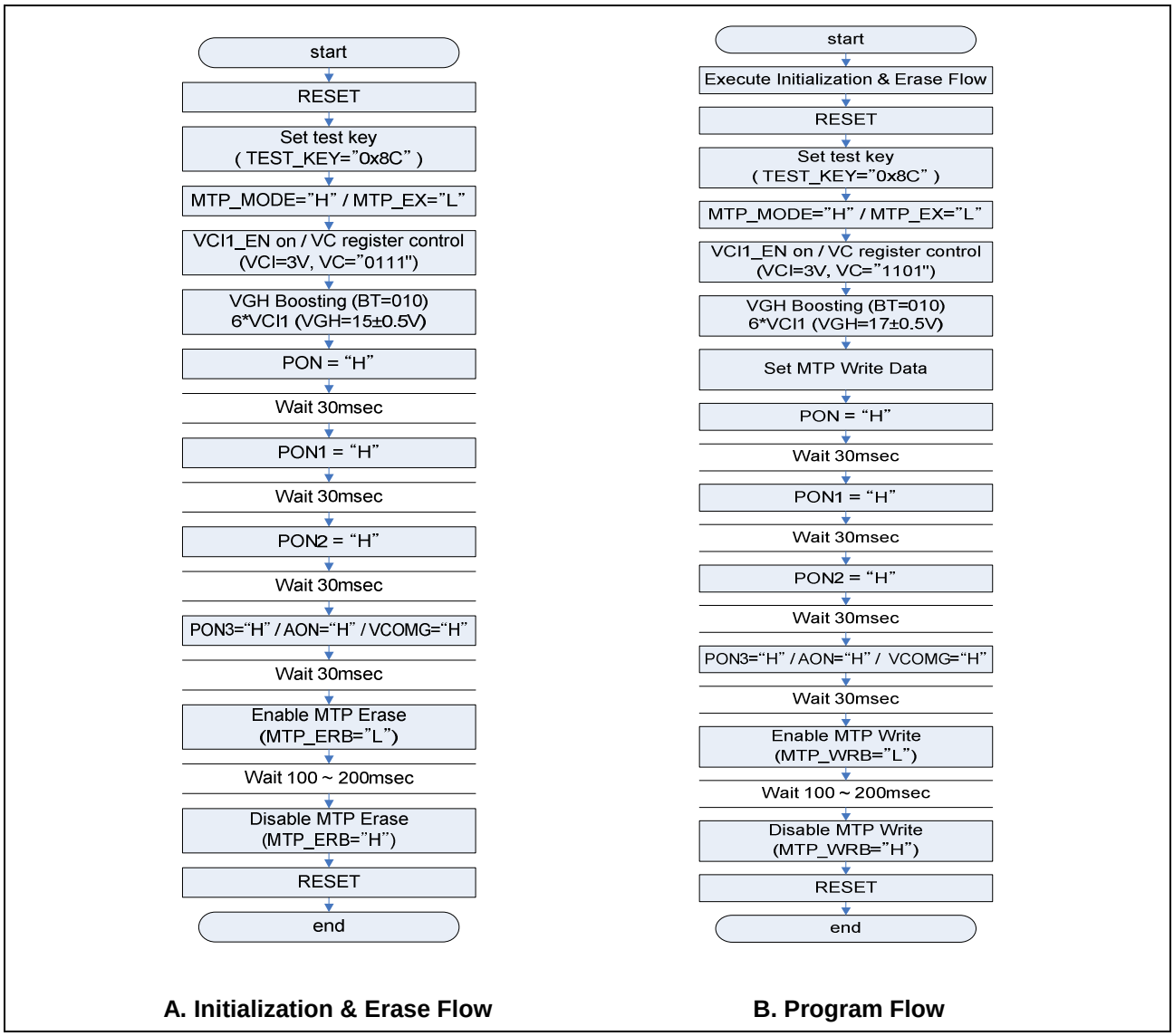


Figure 37. MTP Initialization, Erase and program

MTP Control in External Mode

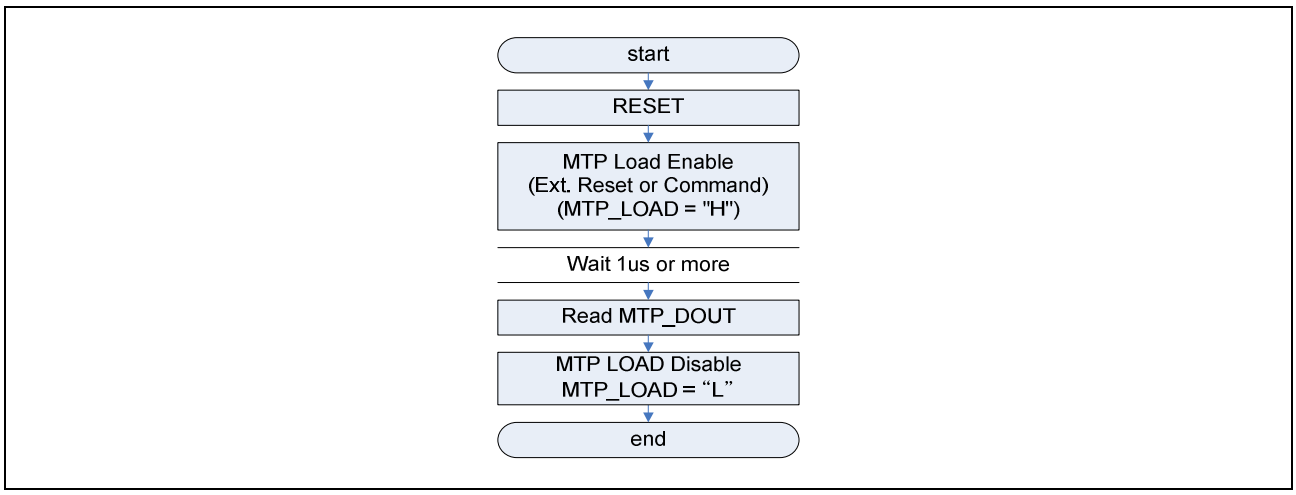
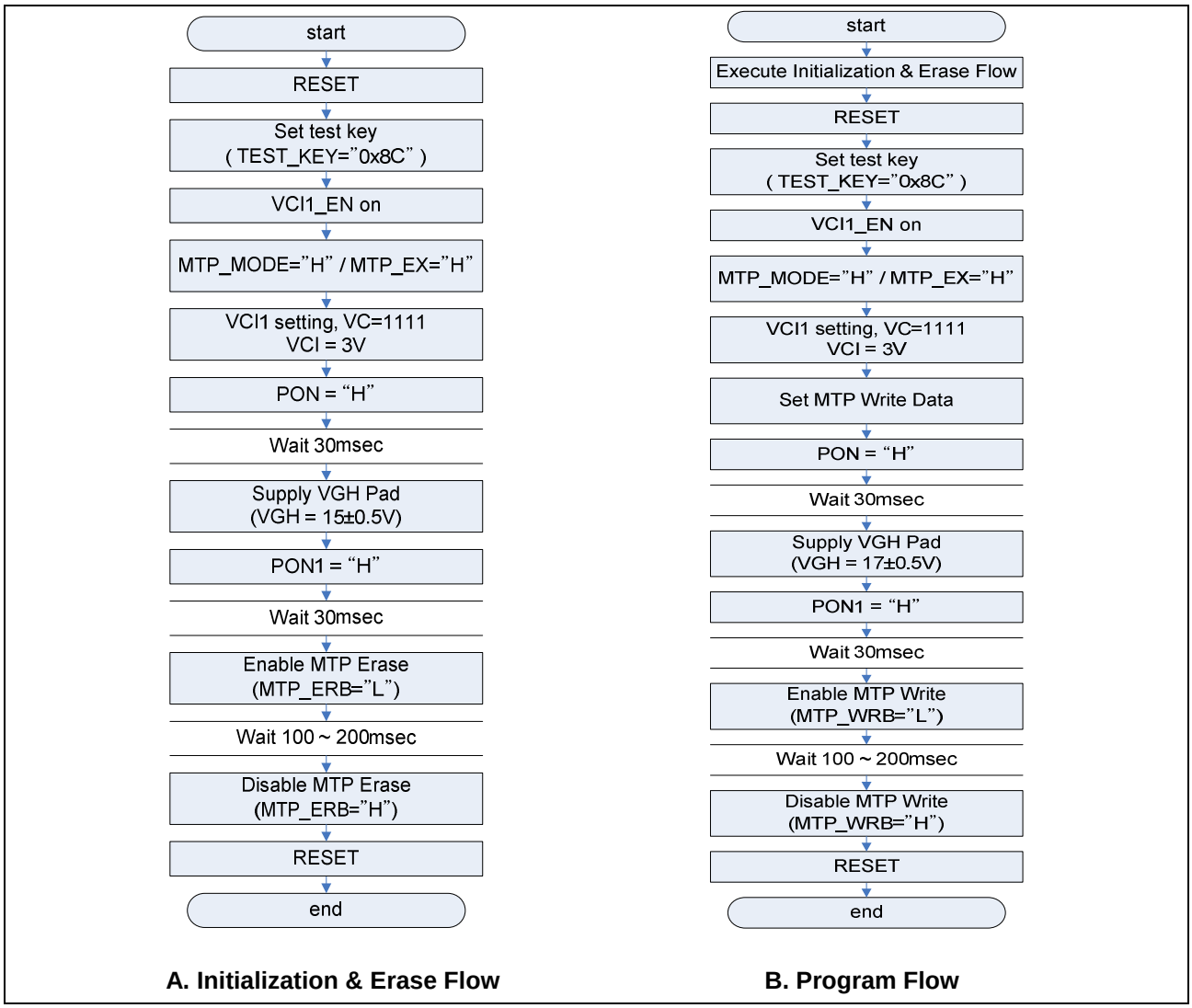


Figure 38. Flow of MTP Load / Read



A. Initialization & Erase Flow **B. Program Flow**

Figure 39. MTP Initialization, Erase and program

Timing of MTP Control

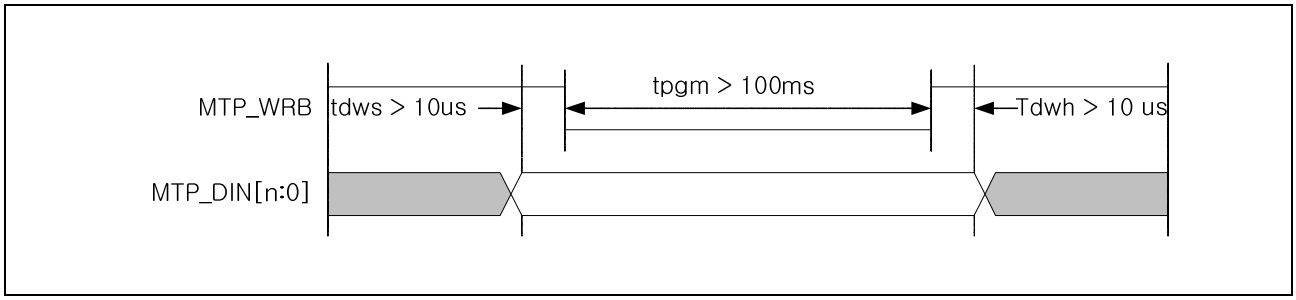


Figure 40. Timing of MTP Program

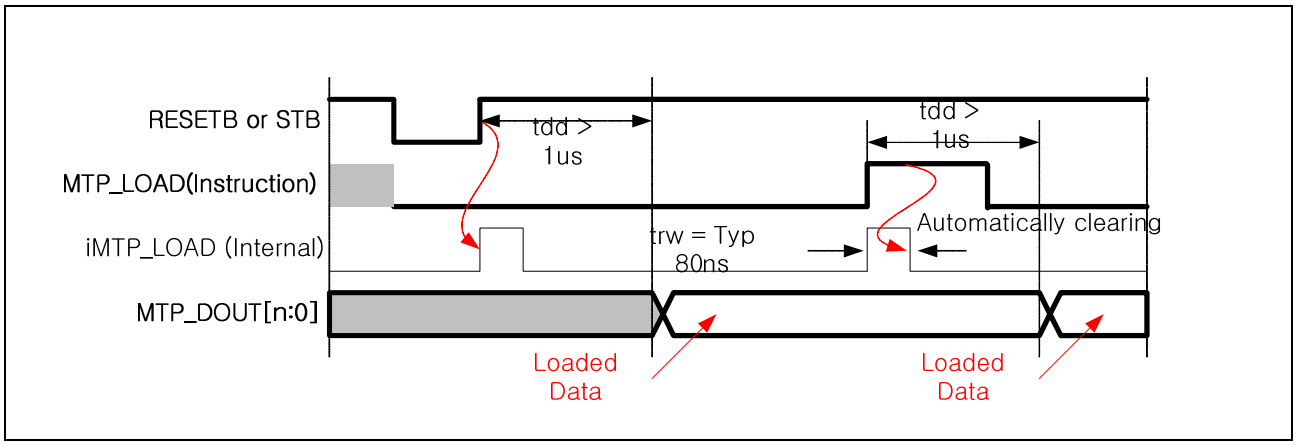


Figure 41. Timing of MTP Load

9.3.35. Product Name/Version Write (R83h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	P_NAME7	P_NAME6	P_NAME5	P_NAME4	P_NAME3	P_NAME2	P_NAME1	P_NAME0	P_VER7	P_VER6	P_VER5	P_VER4	P_VER3	P_VER2	P_VER1	P_VER0

P_NAME7-0: Write Product Name.

P_VER7-0: Write Product Version.

10. RESET FUNCTION

The S6D0154 is internally initialized by RESET input. The reset input must be held for at least 20us. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization

1. Driver output control (VSPL=0, HSPL=0, DPL=0, EPL=0, SM=0, GS=0, SS = 0, NL5–0 = 101000)
2. LCD driving AC control (INV1-0=01, FLD=0)
3. Entry mode set (BGR=0, MDT1-0 = 00, I/D1-0 = 11, AM=0)
4. Display control (FLM_MON = 0, GON = 0, CL = 0, REV = 0, D1–0 = 00: Display off)
5. Blank period control (FP3-0 = 1000, BP3-0 = 1000)
6. Frame cycle control (NO3-0 = 0001, SDT3-0 = 0001, RTN3-0 = 0000: 16 clock cycle in 1H period)
7. External display interface (RIM1-0=00:18-bit RGB interface, DM1-0=00: operated by internal clock, RM=0: system interface)
8. Start oscillation (FOSC4-0=00101, OSCON=1)
9. Power control 1 (SAP3-0 = 0010, DSTB= 0: Deep Standby mode off, STB=0)
10. Power control 2 (APON=0, PON3-0=0000, AB_VCI1=0, AON = 0, VCI1_EN=0, VC3-0 =0000)
11. Power control 3 (BT2-0=000, DC11-0=00, DC21-0=00, DC31-0=00)
12. Power control 4 (DCR_EX=0, DCR2-0=000, GVD6-0 = 0000000)
13. Power control 5 (VCOMG=1, VCMR = 0, VCM6-0 = 0000000, VML6-0 = 0000000)
14. VCIR Recycling (VCIR2-0 = 000)
15. RAM Address data (AD7-0 = 00000000, AD16-8 = 000000000)
16. FLM Function (FLM_INT1-0 = 00, FLM_POS8-0 = 000000000)
17. Gate scan position (SCN5-0=000000)
18. Vertical scroll control 1 (SSA8–0 = 000000000, SEA8-0 = 100111111)
19. Vertical scroll control 2 (SST8–0 = 000000000: No vertical scroll)
20. Partial screen division (SE18-10 = 100111111, SS18-10 = 000000000)
21. Horizontal RAM address position (HEA8-0 = 011101111, HSA8-0 = 000000000)
22. Vertical RAM address position (VEA8-0 = 100111111, VSA8-0 = 000000000)

23. Sub Panel Control (FCV_EN = 0, MPU_MODE = 0, STN_EN = 0, SUB_IM1-0 = 00, VWAKE_EN = 0)
24. MDDI link wake-up start position (WKL8-0 = 000000000, WKF3-0 = 0000)
25. Sub Panel selection index / write index (SUB_SEL7-0 = 01001010, SUB_WR7-0 = 00100010)
26. GPIO value (GPIO5-0 = 000000)
27. GPIO in/output control (GPIO_CON5-0 = 000000)
28. GPIO Clear (GPCLR5-0 = 000000)
29. GPIO interrupt enable (GPIO_EN5-0 = 000000)
30. GPIO polarity selection (GPPOL5-0 = 000000)
31. Gamma control
(PKP03–00 = 0000, PKP13–10 = 0000, PKP23–20 = 0000, PKP33–30 = 0000,
PKP43–40 = 0000, PKP53–50 = 0000, PRP03–00 = 0000, PRP13–10 = 0000)
(PKN03–00 = 0000, PKN13–10 = 0000, PKN23–20 = 0000, PKN33–30 = 0000,
PKN43–40 = 0000, PKN53–50 = 0000, PRN03–00 = 0000, PRN13–10 = 0000)
(VRP04–00 = 00000, VRP14–10 = 00000, VRN04–00 = 00000, VRN_14–10 = 00000)
32. Test key command (00000000)
33. MTP control (MTP_MODE=0, MTP_EX=0 , MTP_SEL=0, MTP_ERB=1, MTP_WRB=1,MTP_LOAD=0)
34. MTP load data (GPI3-0 = 0000, MTP_DIN4-0 = 00000)
35. Product Name/Version Write (P_NAME7-0 = 00000000, P_VER = 00000000)

GRAM Data Initialization

GRAM is not automatically initialized by reset input but must be initialized by software while display is off (D1-0 = 00).

Output pin Initialization

LCD driver output pins (Source output): Output AVSS level

(Gate output) : Output AVSS level

11. POWER SUPPLY

11.1. Power Supply Circuit

The following figure shows a configuration of the voltage generation circuit of S6D0154. The step-up circuits consist of step-up circuits 1, 2 and 3. Step-up circuit1 doubles input voltage supplied from VCI1 for AVDD level. Step-up circuit2 makes 2.5, 3 or 3.5 times AVDD voltage for VGH level, and makes -1.5, -2 or -2.5 times AVDD voltage for VGL level. Step-up circuit3 reverses the VCI1 voltage with respect to VSS to generate VCL level. These step-up circuits generate power supplies AVDD, VGH, VGL, and VCL. Reference voltage GVDD is generated with VREF from the voltage divide circuit. VCOMH and VCOML are generated with GVDD from the voltage adjustment circuit. Connect VCOM to the TFT panel.

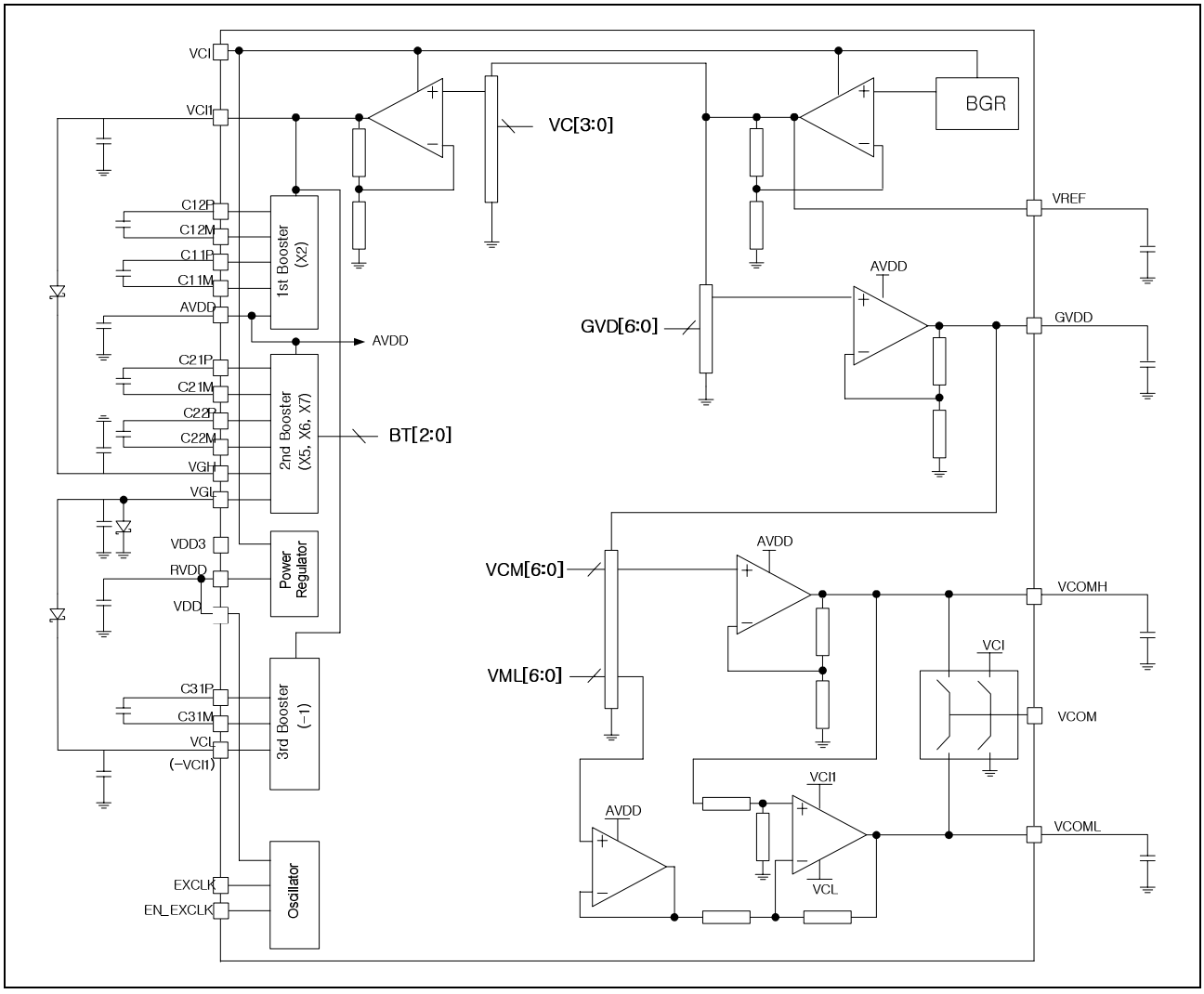


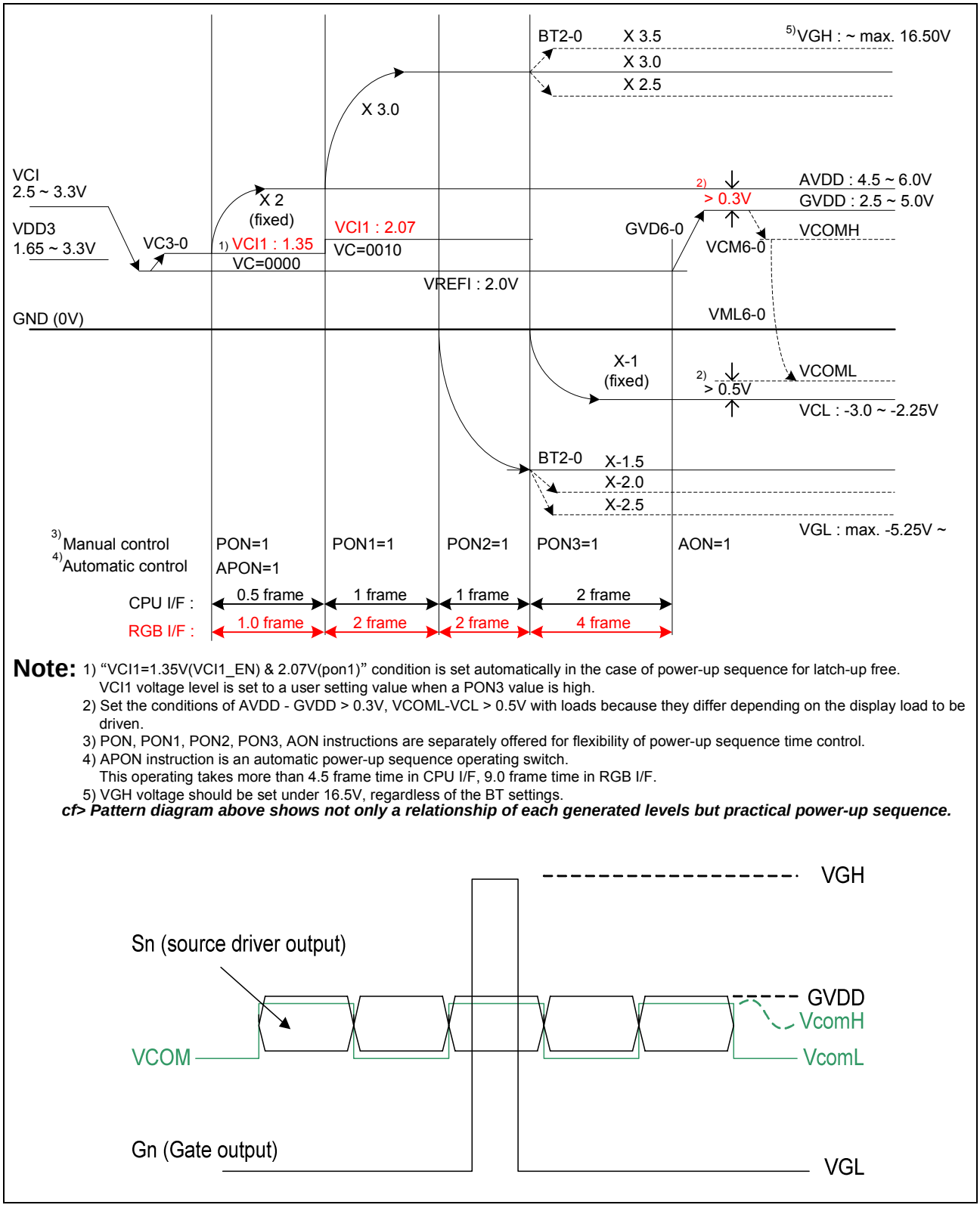
Figure 42. Configuration of the Internal Power-Supply Circuit

Note.

1. Use the 1uF capacitor.
2. Schottky diode between VGL and VSS is positively necessary for latch-up free.
3. Schottky diodes between VCL and VGL and between VGH and VCI1 may be necessary when latch-up
4. Occurs even if latch-up free power supply set-up flow is applied.
5. The Capacitor between VREF and VSS may be used by case when VCOM swing level fluctuates.

11.2. Pattern Diagrams for Voltage Setting

The following figure shows a pattern diagram for the voltage setting and an example of waveforms.



Note: 1) "VCI1=1.35V(VCI1_EN) & 2.07V(pon1)" condition is set automatically in the case of power-up sequence for latch-up free.
VCI1 voltage level is set to a user setting value when a PON3 value is high.
2) Set the conditions of AVDD - GVDD > 0.3V, VCOML-VCL > 0.5V with loads because they differ depending on the display load to be driven.
3) PON, PON1, PON2, PON3, AON instructions are separately offered for flexibility of power-up sequence time control.
4) APON instruction is an automatic power-up sequence operating switch.
This operating takes more than 4.5 frame time in CPU I/F, 9.0 frame time in RGB I/F.
5) VGH voltage should be set under 16.5V, regardless of the BT settings.

cf> Pattern diagram above shows not only a relationship of each generated levels but practical power-up sequence.

Figure 43. Power-Up Pattern Diagram & An Example Of Source/VCOM Waveforms

11.3. Set up Flow of Generated Power Supply

Apply the power in a sequential way as shown in the following figure. The settling time of the oscillation circuit, step-up1/2/3 circuits, and operational amplifier depend on the external resistance or capacitance value.

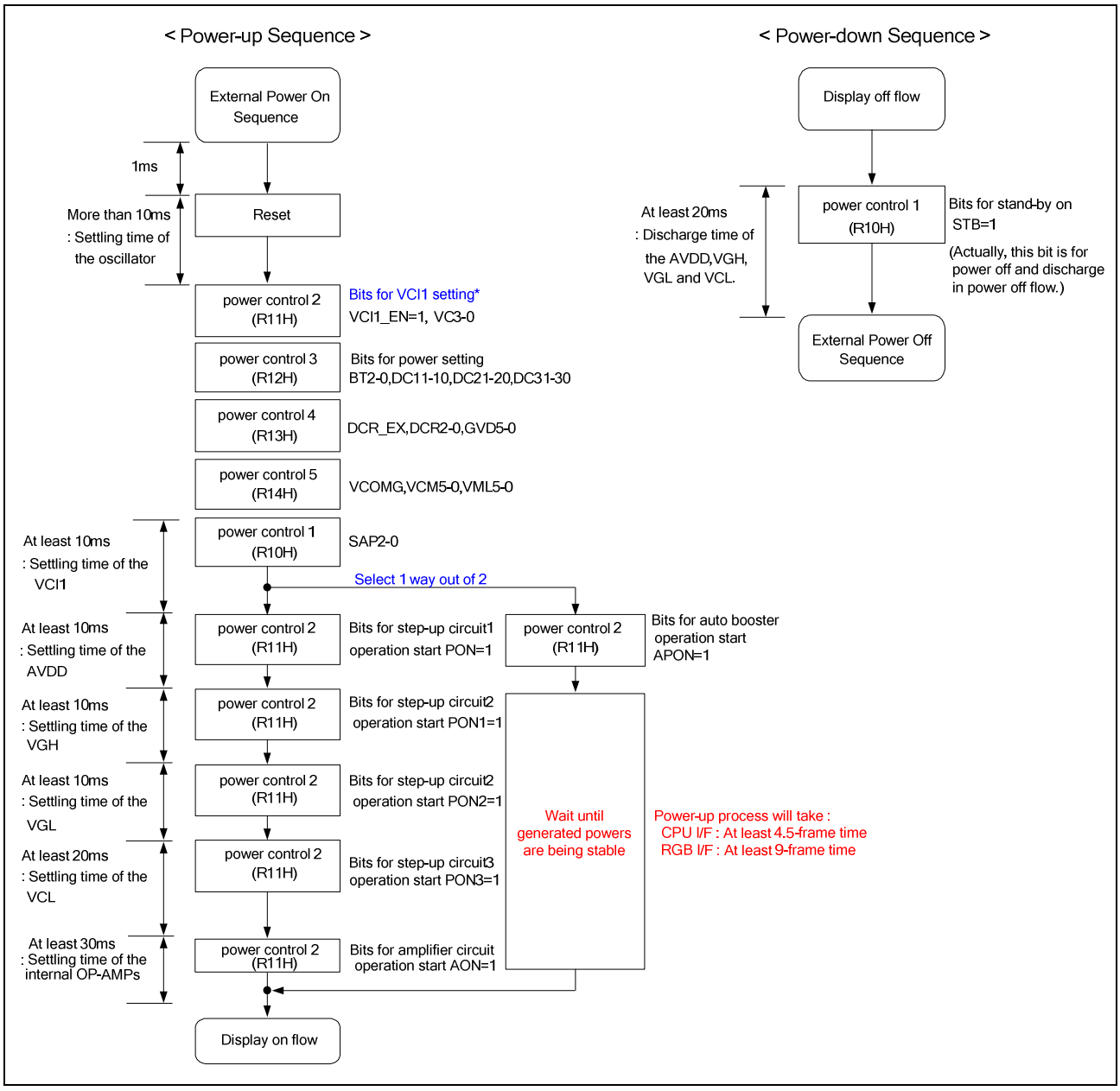


Figure 44. Setup Flow of Generated Power Supply

11.4. Voltage regulation function

The S6D0154 has the internal voltage regulator. By the use of this function, unexpected damages on internal logic circuit can be avoided. Furthermore, power consumption can also be obtained. Detailed function description and application configuration is described in the following diagram.

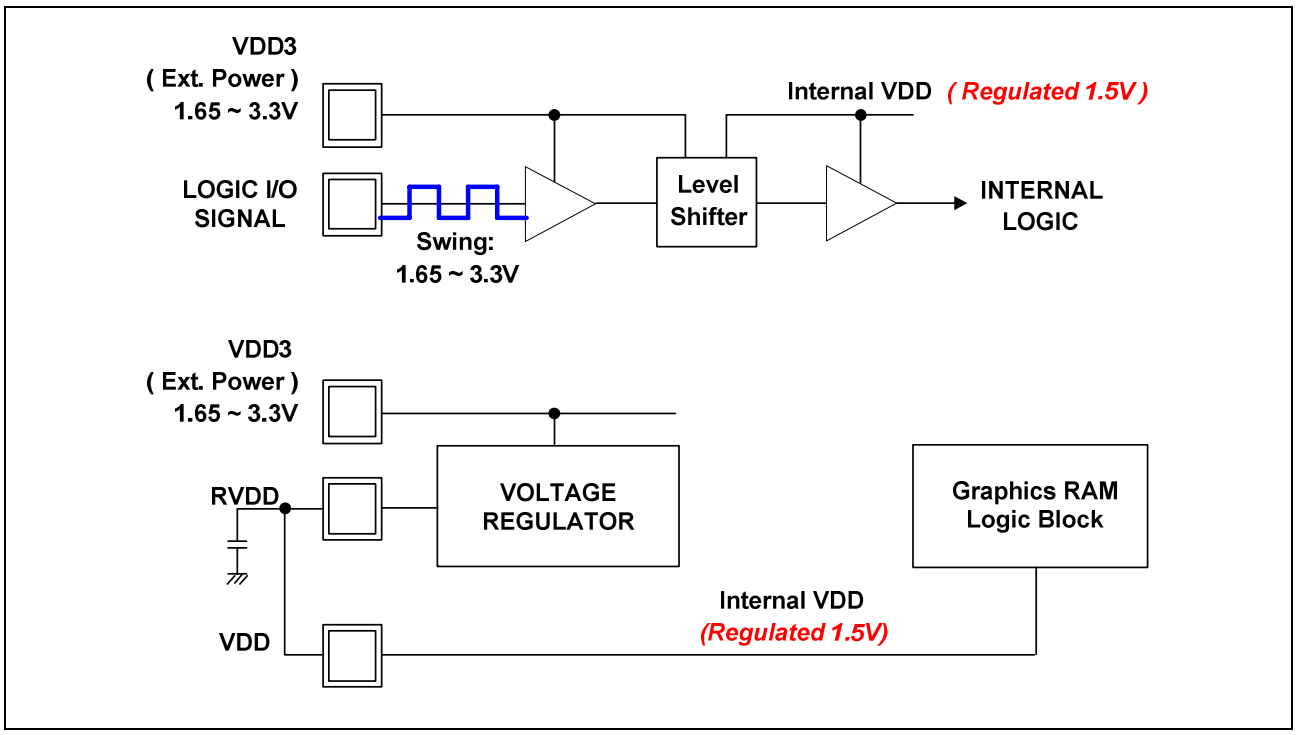


Figure 45. Voltage Regulation Function

12. INTERFACE SPECIFICATION

S6D0154 incorporates nine System Interfaces which are used to set instructions, and an RGB interface that is used to display motion pictures. Selecting one of these interfaces to match the screen data (motion picture or still picture) enables efficient transfer of data for display.

The External Clock Operation mode that uses RGB interface allows flicker-free screen update. In this mode, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for display operation. The data for display (DB [17:0]) is written according to the status of ENABLE in synchronization with VSYNC, HSYNC, and DOTCLK. In addition, using Window Address function enables rewriting only to the internal GRAM area to display motion pictures. Using this function also enables simultaneously display of motion picture and the GRAM data that was written earlier.

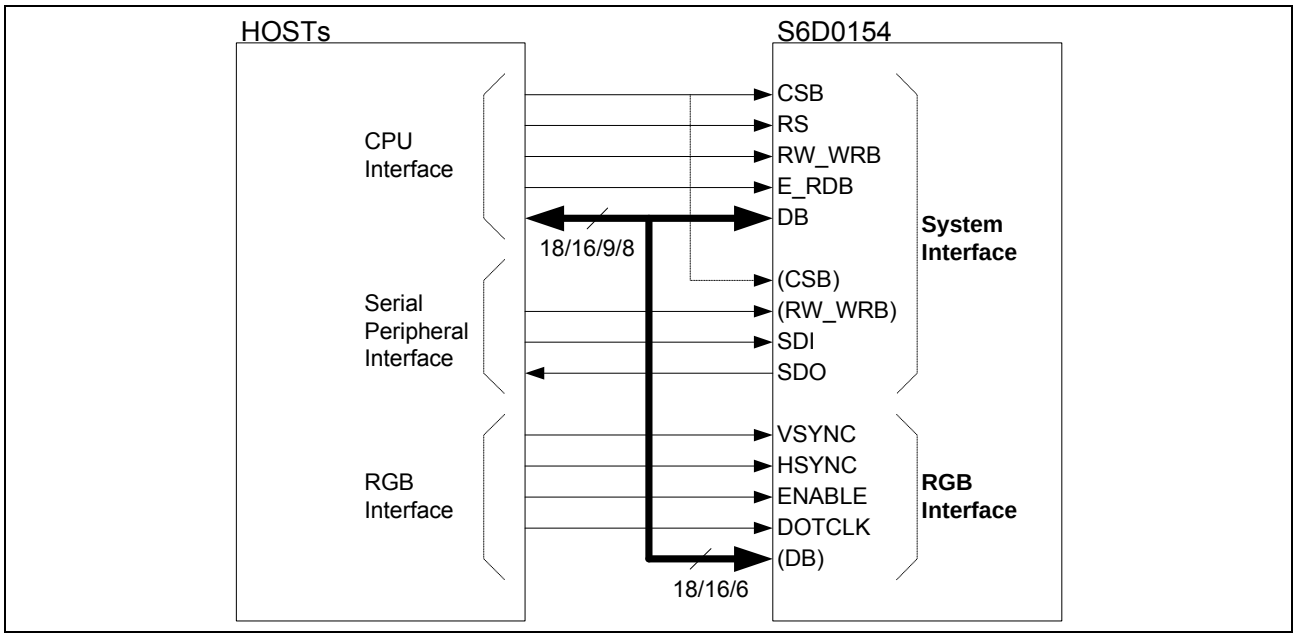


Figure 46. System Interface and RGB Interface

12.1. SYSTEM INTERFACE

S6D0154 has nine System Interfaces as show below.

Table 42. System Interfaces of S6D0154

IM[3:0]	System Interface
4'b0000	68-16bit CPU interface
4'b0001	68-8bit CPU interface
4'b0010	80-16bit CPU interface
4'b0011	80-8bit CPU interface
4'b010x	Serial peripheral interface (SPI)
4'b011x	Setting disabled
4'b1000	68-18bit CPU interface
4'b1001	68-9bit CPU interface
4'b1010	80-18bit CPU interface
4'b1011	80-9bit CPU interface
4'b110x	HSSI
4'b111x	Setting disabled

In order to select one of them you should set IM [3:0] properly. For detail, see "PAD DESCRIPTION" described earlier.

12.1.1. 68-18BIT CPU INTERFACE

Bit Assignment

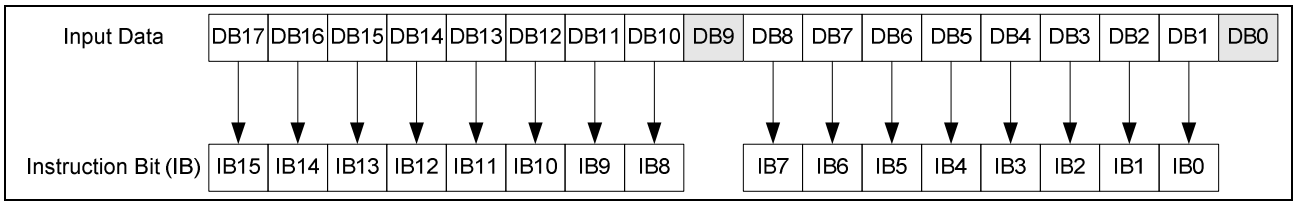


Figure 47. Bit Assignment of Instructions on 68-18bit CPU Interface

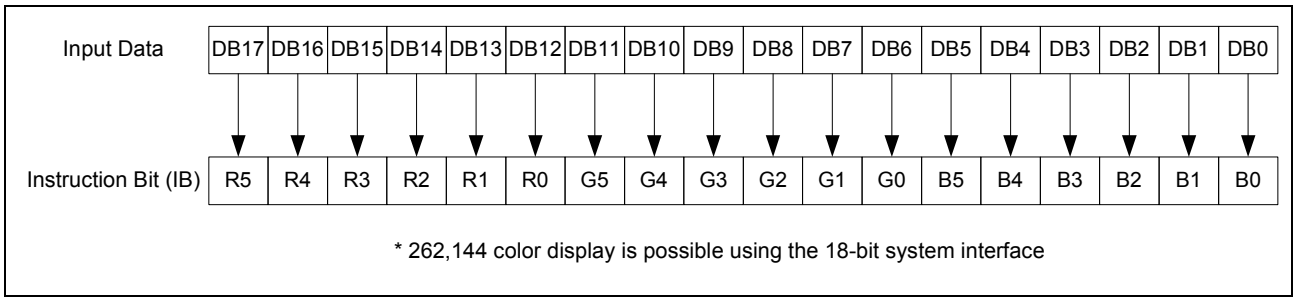


Figure 48. Bit Assignment of GRAM Data on 68-18bit CPU Interface

Timing Diagram

There are 4 timing conditions for 68 18-bit CPU interface, which are index write timing condition, data write timing condition and status read timing condition.

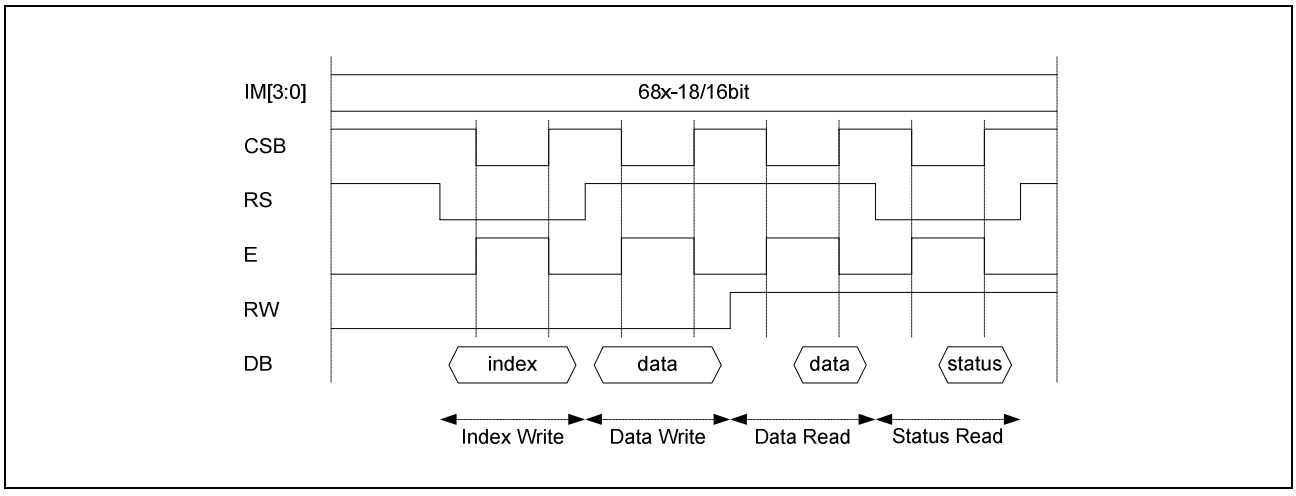


Figure 49. Timing Diagram of 68-18bit CPU Interface

12.1.2. 68-16BIT CPU INTERFACE

Bit Assignment

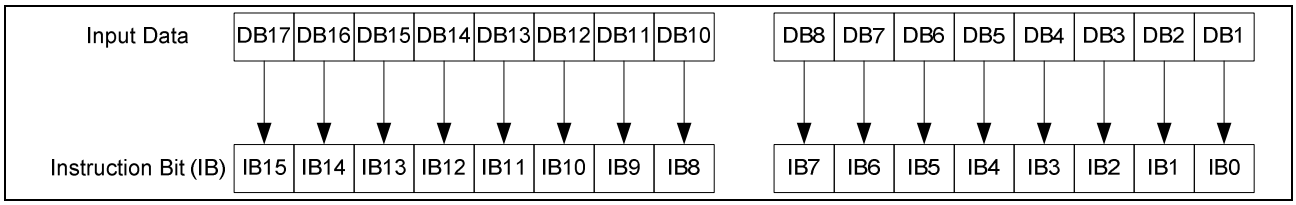


Figure 50. Bit Assignment of Instructions on 68-16bit CPU Interface

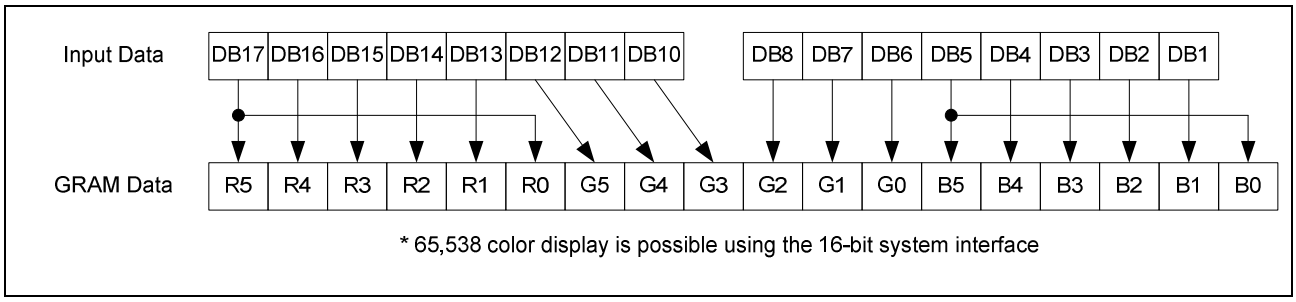


Figure 51. Bit Assignment of GRAM Data on 68-16bit CPU Interface

Timing Diagram

There are 4 timing conditions for 68-16bit CPU interface, which are index write timing condition, data write timing condition and status read timing condition.

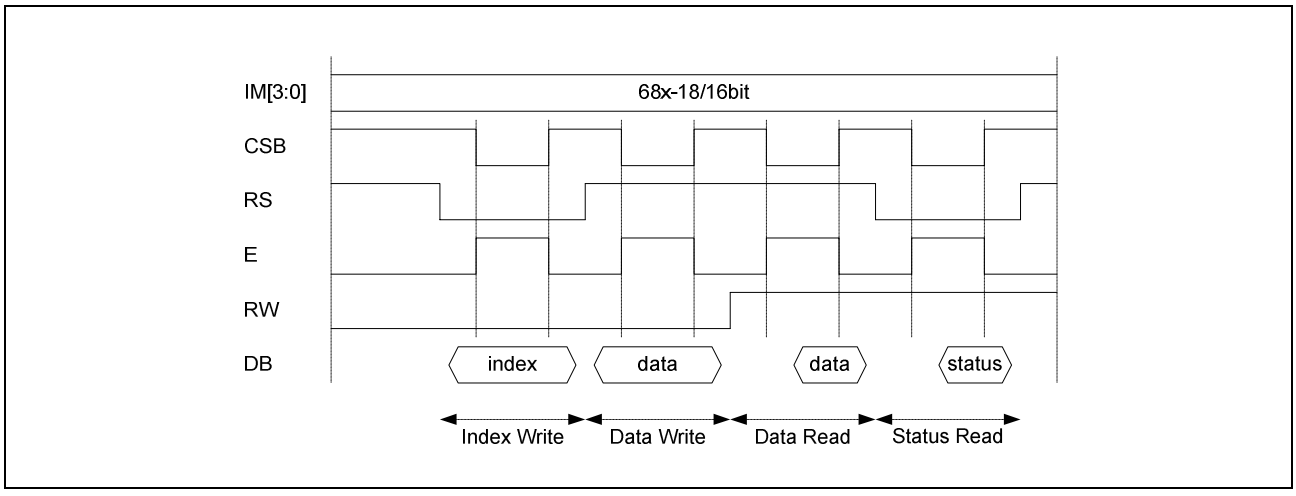


Figure 52. Timing Diagram of 68-16bit CPU Interface

12.1.3. 68-9BIT CPU INTERFACE

Bit Assignment

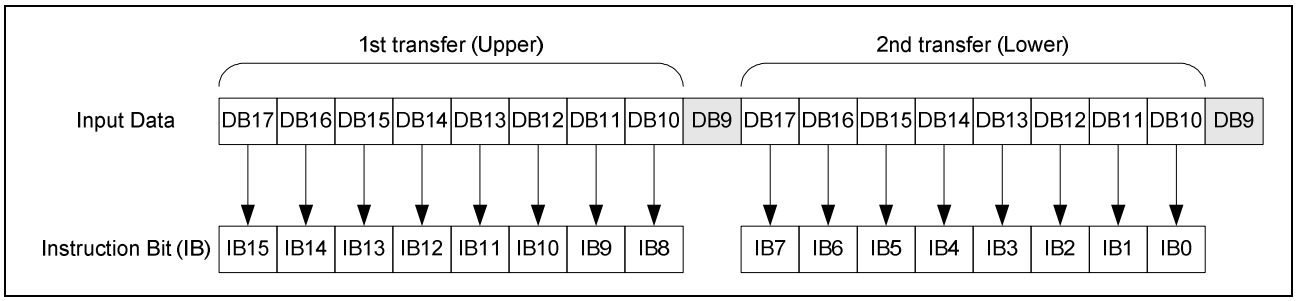


Figure 53. Bit Assignment of Instructions on 68-9bit CPU Interface

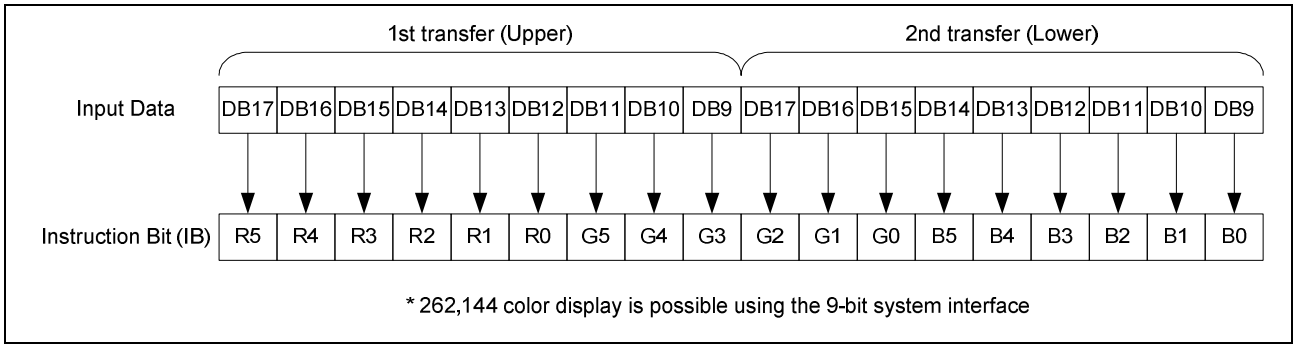


Figure 54. Bit Assignment of GRAM Data on 68-9bit CPU Interface

Timing Diagram

There are 4 timing conditions for 68-9bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.

In this mode, 16-bit instructions and GRAM data are divided into two half words and the transfer starts from the upper half word.

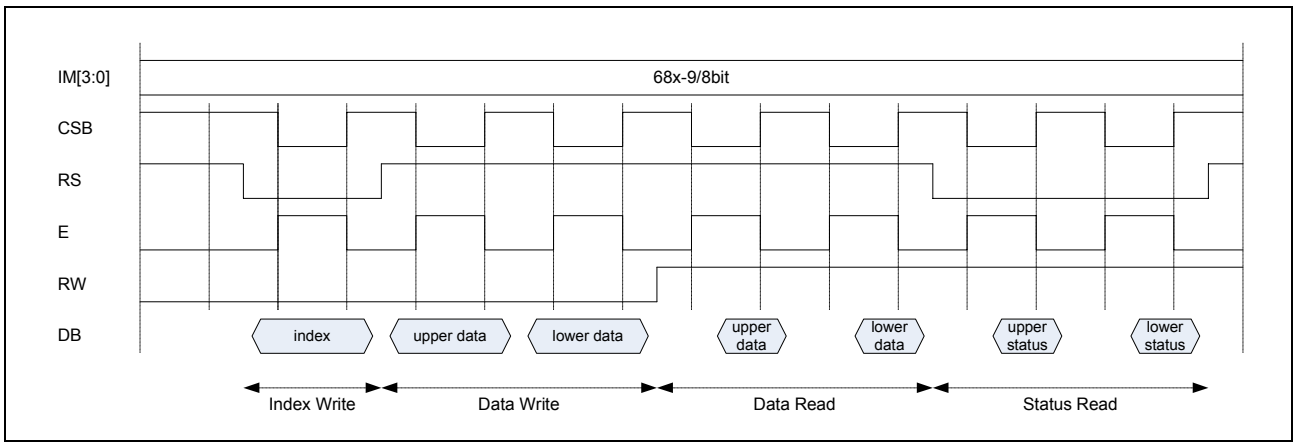


Figure 55. Timing Diagram of 68-9bit CPU Interface

12.1.4. 68-8BIT CPU INTERFACE

Bit Assignment

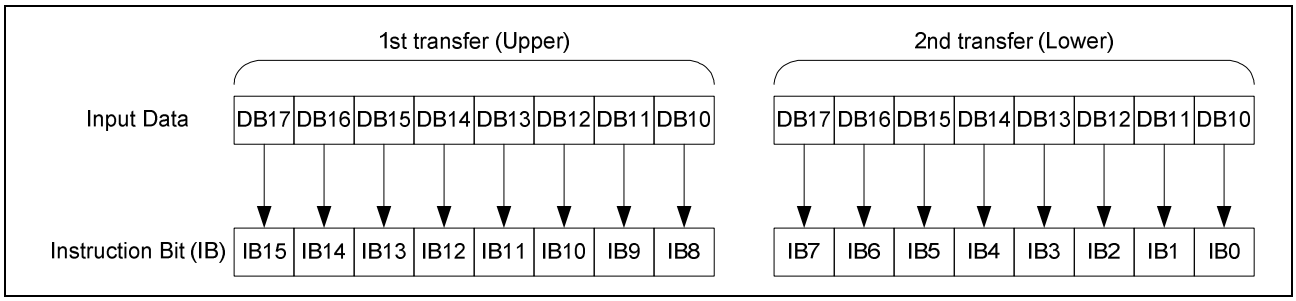


Figure 56. Bit Assignment of Instructions on 68-8bit CPU Interface

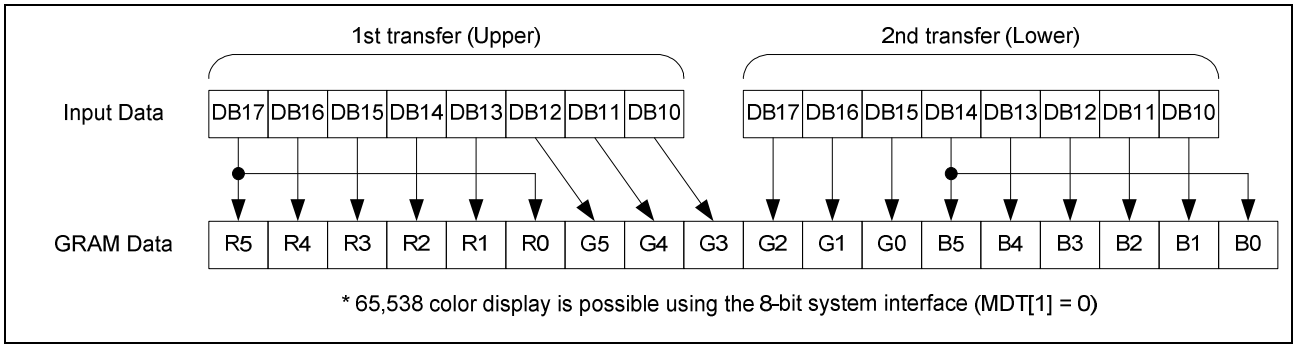


Figure 57. Bit Assignment of GRAM Data on 68-8bit CPU Interface

Timing Diagram

There are 4 timing conditions for 68-8bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.

In this mode, 16-bit instructions and GRAM data are divided into two half words and the transfer starts from the upper half word.

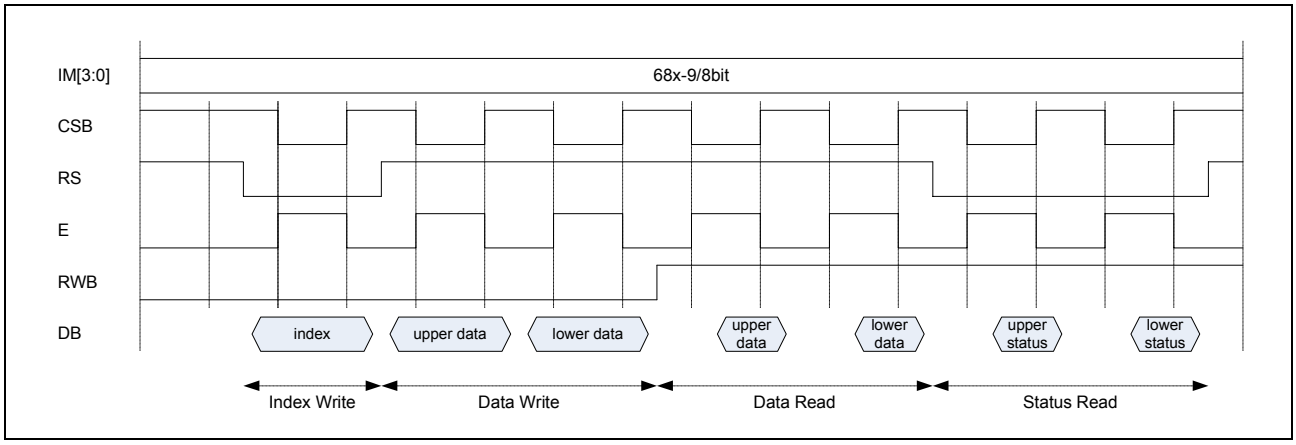


Figure 58. Timing Diagram of 68-8bit CPU Interface

12.1.5. 80-18BIT CPU INTERFACE

Bit Assignment

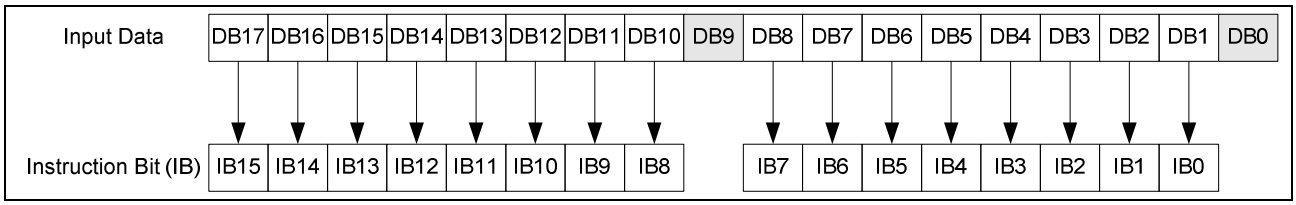


Figure 59. Bit Assignment of Instructions on 80-18bit CPU Interface

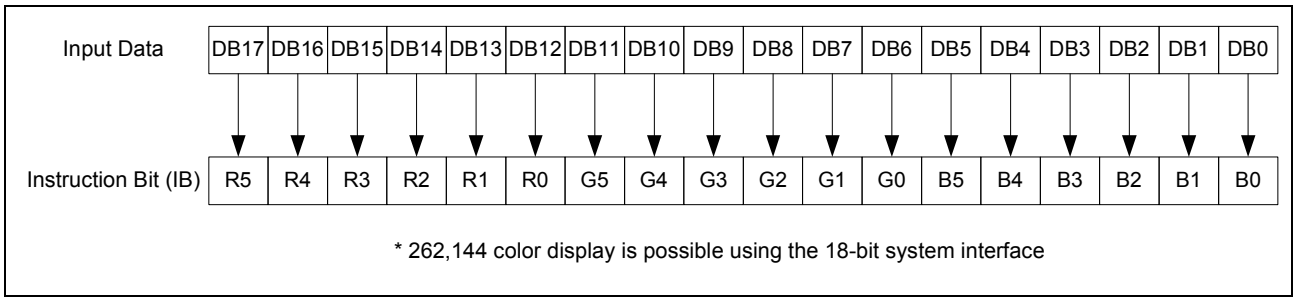


Figure 60. Bit Assignment of GRAM Data on 80-18bit CPU Interface

Timing Diagram

There are 4 timing conditions for 80 18-bit CPU interface, which are index write timing condition, data write timing condition and status read timing condition.

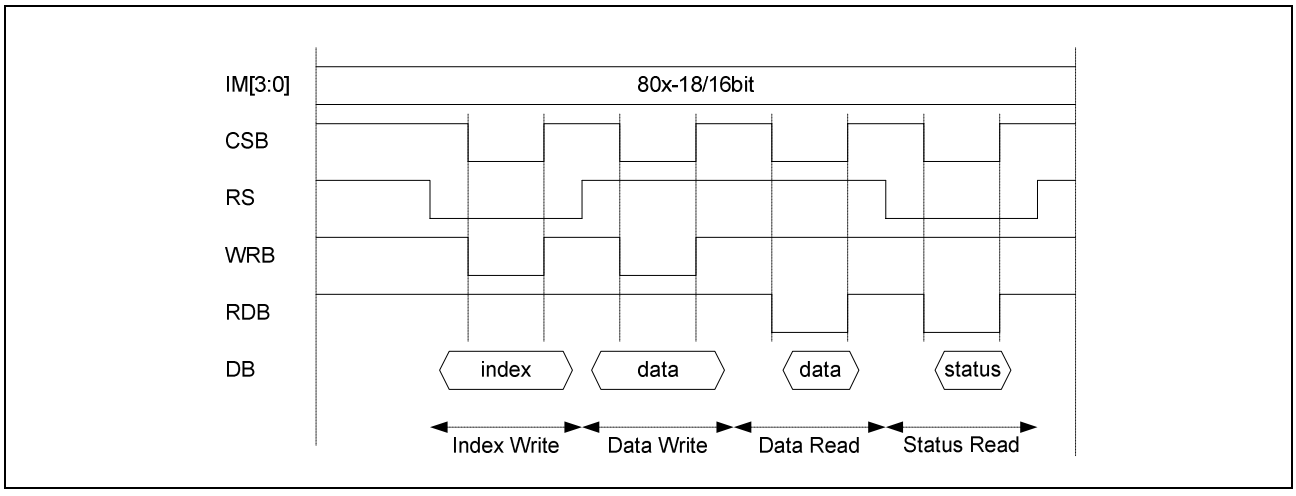


Figure 61. Timing Diagram of 80-18bit CPU Interface

12.1.6. 80-16BIT CPU INTERFACE

Bit Assignment

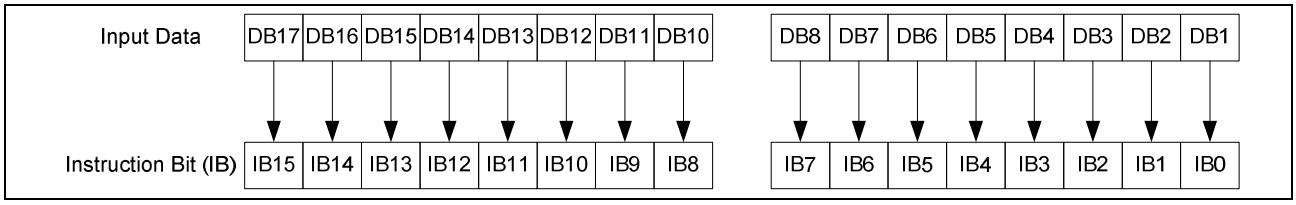


Figure 62. Bit Assignment of Instructions on 80-16bit CPU Interface

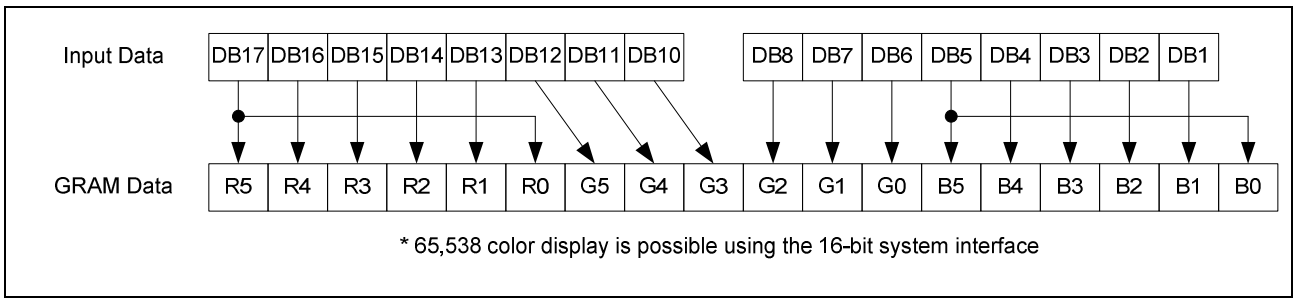


Figure 63. Bit Assignment of GRAM Data on 80-16bit CPU Interface

Timing Diagram

There are 4 timing conditions for 80-16bit CPU interface, which are index write timing condition, data write timing condition and status read timing condition.

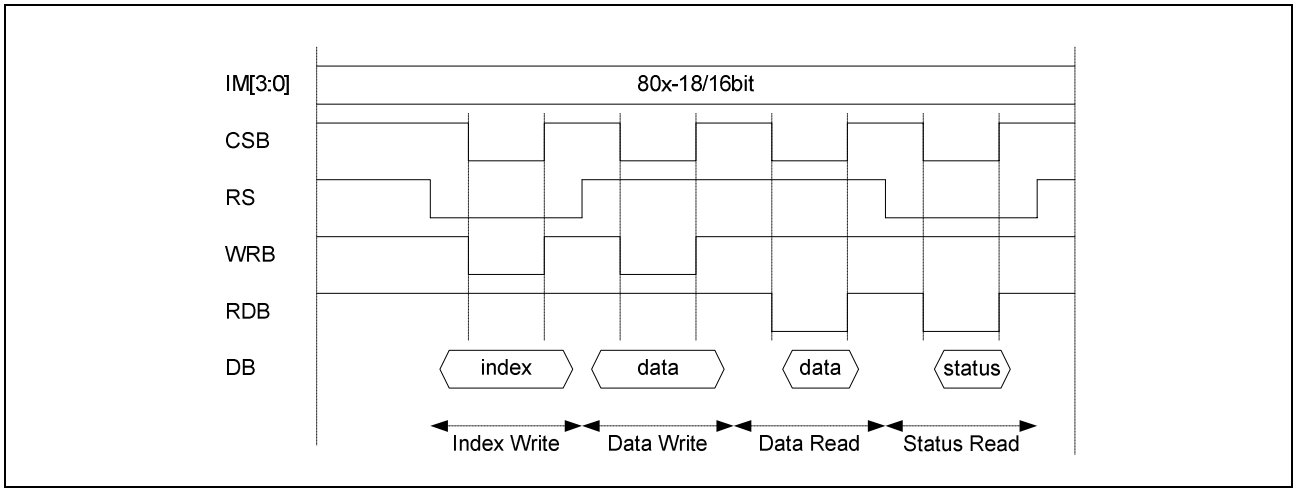


Figure 64. Timing Diagram of 80-16bit CPU Interface

12.1.7. 80-9BIT CPU INTERFACE

Bit Assignment

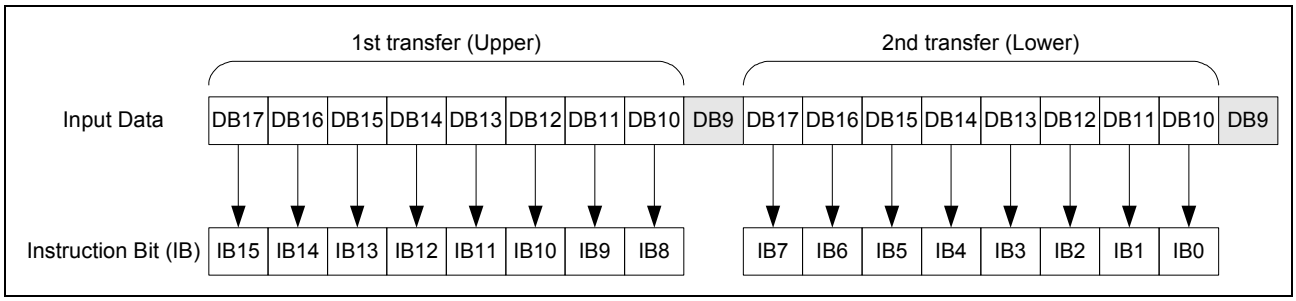


Figure 65. Bit Assignment of Instructions on 80-9bit CPU Interface

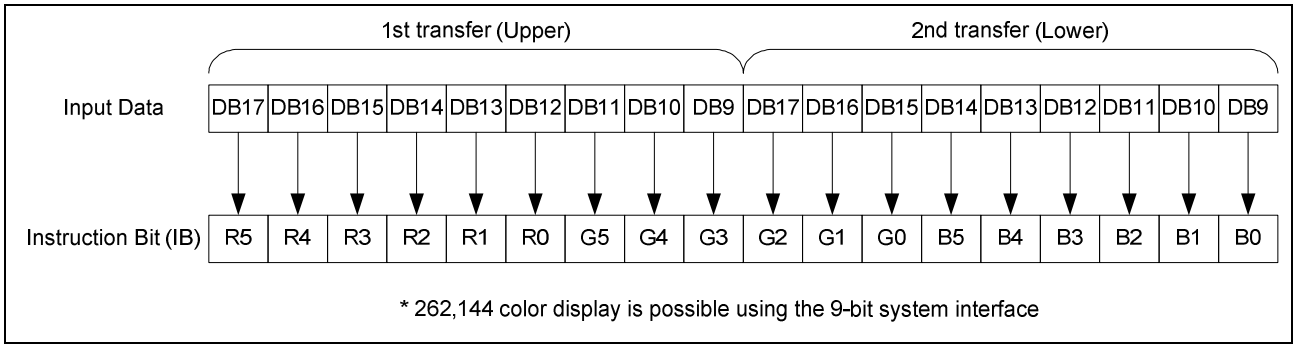


Figure 66. Bit Assignment of GRAM Data on 80-9bit CPU Interface

Timing Diagram

There are 4 timing conditions for 80-9bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.

In this mode, 16-bit instructions and GRAM data are divided into two half words and the transfer starts from the upper half word.

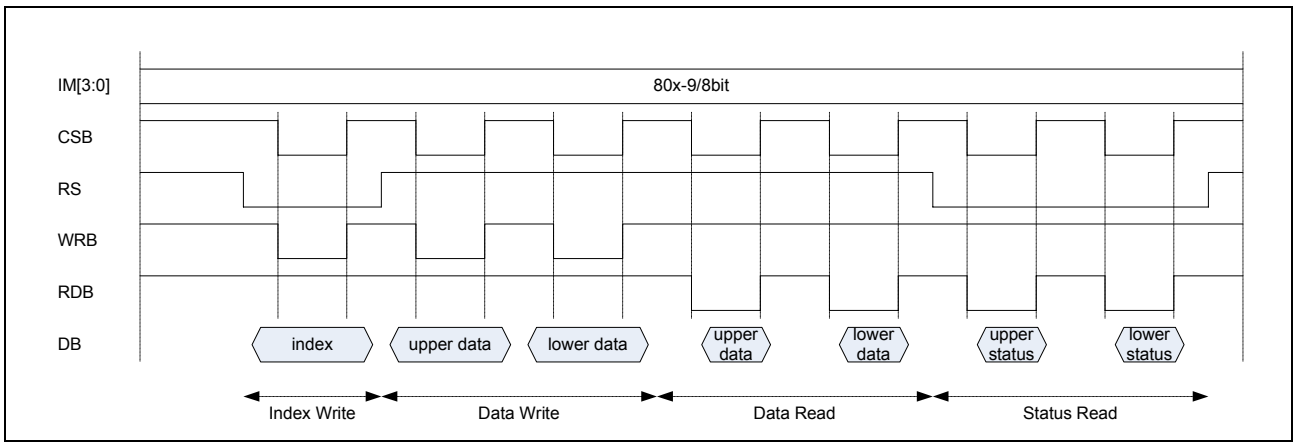


Figure 67. Timing Diagram of 80-9bit CPU Interface

12.1.8. 80-8BIT CPU INTERFACE

Bit Assignment

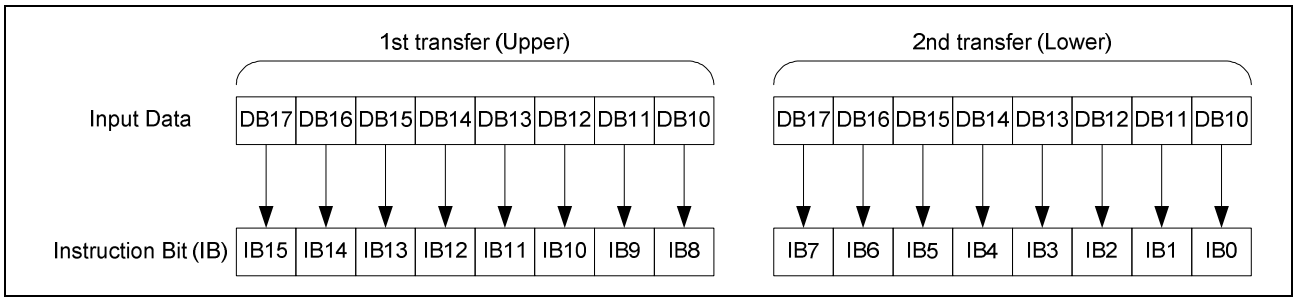


Figure 68. Bit Assignment of Instructions on 80-8bit CPU Interface

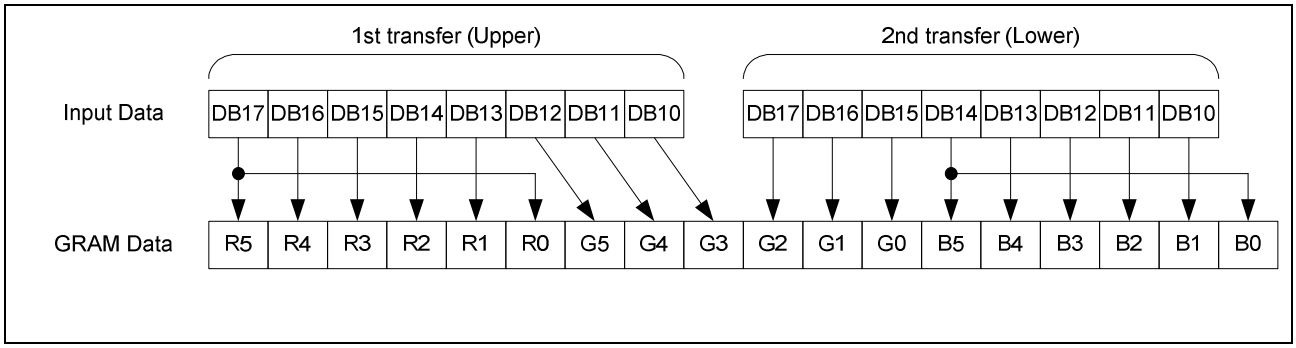


Figure 69. Bit Assignment of GRAM Data on 80-8bit CPU Interface

Timing Diagram

There are 4 timing conditions for 80-8bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.

In this mode, 16-bit instructions and GRAM data are divided into two half words and the transfer starts from the upper half word.

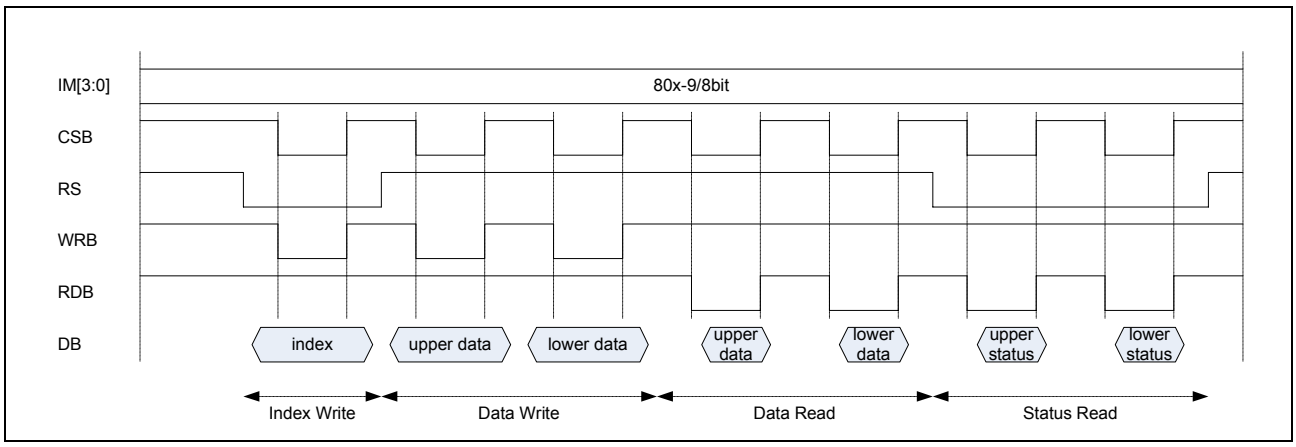


Figure 70. Timing Diagram of 80-8bit CPU Interface

12.1.9. SERIAL PERIPHERAL INTERFACE

Setting IM [3:0] properly allows standard clock-synchronized serial data transfer (SPI; Serial Peripheral Interface), using CSB (chip select), SCL (serial transfer clock), SDI (serial input data) and SDO (serial output data). For the serial interface, IM [0] is used as ID.

S6D0154 initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input.

S6D0154 is selected when the 6-bit chip address in the start byte transferred by the transmitting device matches the 6-bit device identification code assigned to S6D0154. ID is the least significant bit of the device identification code. S6D0154, when selected, receives the subsequent data string.

Two different chip addresses must be assigned to a single S6D0154 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = “0”, data can be written to the index register or status can be read, and when RS = “1”, an instruction can be issued or data can be written to or read from GRAM. Read or write is determined according to the eighth bit of the start byte (R/WB bit). The data is written (receives) when the R/WB bit is “0”, and is read (transmits) when the R/WB bit is “1”.

After receiving the start byte, S6D0154 receives or transmits the subsequent data. The data is transferred with the MSB first. All S6D0154 instructions are 16 bits, so two bytes are received with the MSB first (DB15 to 0), and then the instruction is internally executed.

Five bytes of GRAM data read just after the start byte are invalid. S6D0154 starts to read correct GRAM data from the sixth byte. Likewise, it starts to read correct register/status from the second byte.

Table 43. Start Byte Format

Transfer Bit	1st	2nd	3rd	4th	5th	6th	7th	8th
Start byte format	Device Identification code						RS	R/WB
	0	1	1	1	0	ID		

Note. The IM [0] pin is used as ID

Table 44. RS and RWB Bit Function

RS bit	R/WB bit	Function
0	0	Set index register
0	1	Read status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

Bit Assignment

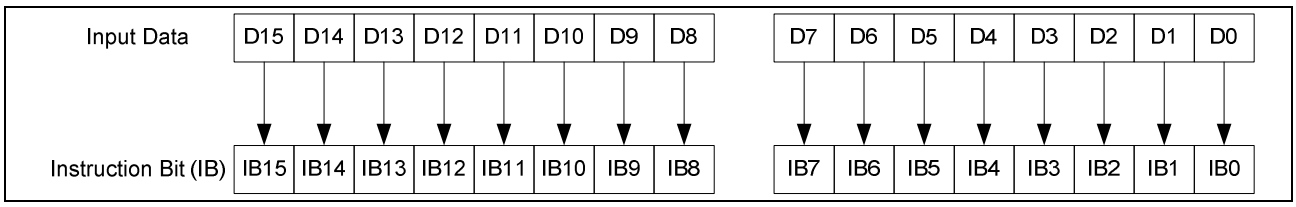


Figure 71. Bit Assignment of Instructions on SPI

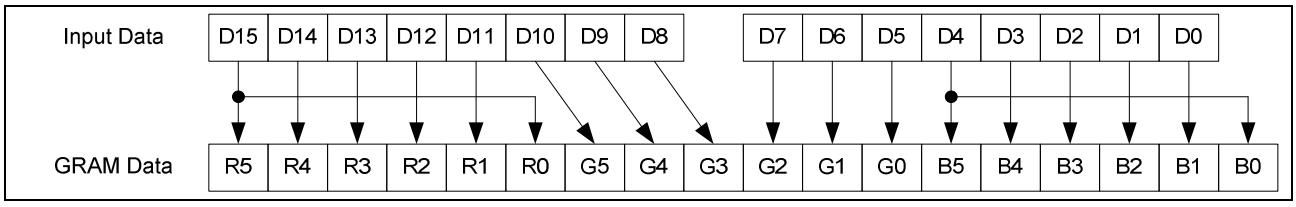


Figure 72. Bit Assignment of GRAM Data on SPI

Timing Diagrams

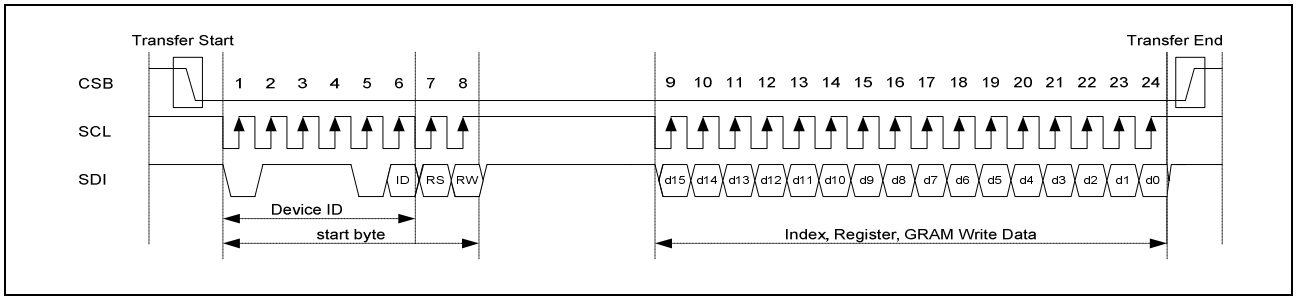


Figure 73. Basic Timing Diagram of Data Transfer through SPI

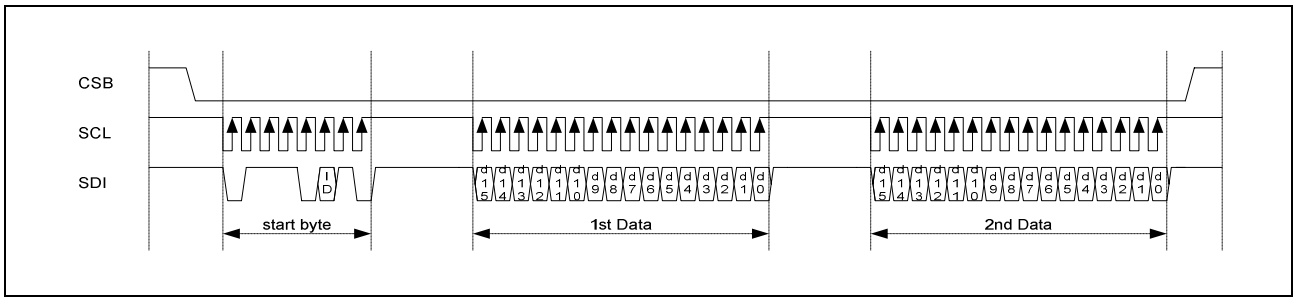


Figure 74. Timing Diagram of Consecutive Data-Write through SPI

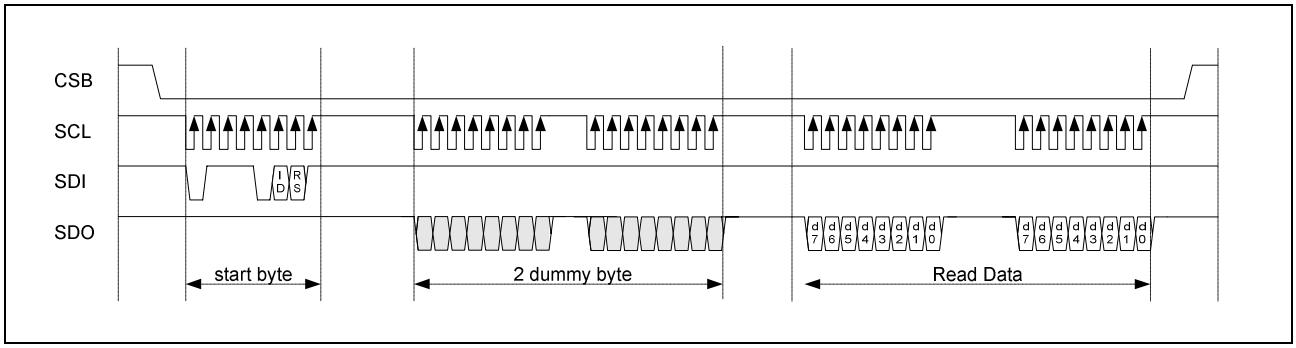


Figure 75. Timing Diagram of Register / Status Read through SPI

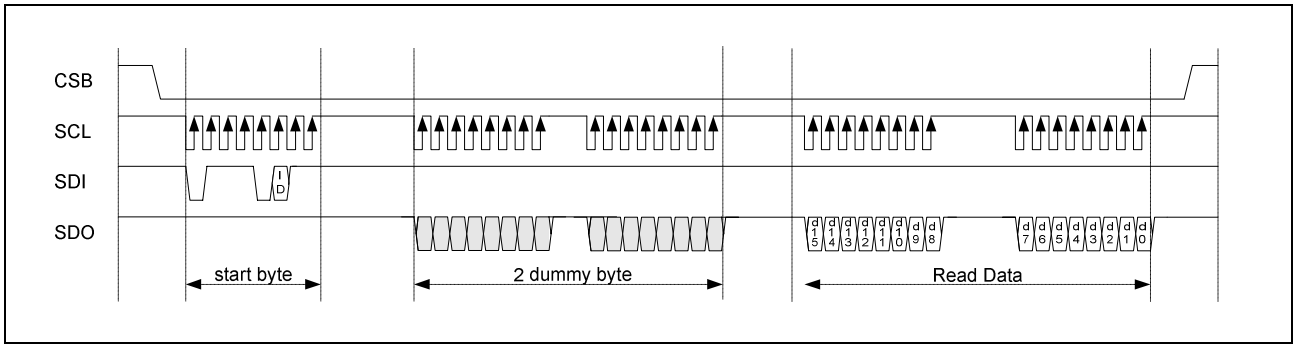


Figure 76. Timing Diagram of GRAM-Data Read through SPI

12.2. RGB INTERFACE

12.2.1. MOTION PICTURE DISPLAY

S6D0154 incorporates RGB interface to display motion pictures and GRAM to store data for display.
To display motion pictures, S6D0154 has the following features.
- Only motion picture area can be transferred by the Window Address function.
- Only motion picture area to be rewritten can be transferred selectively.
- Reducing the amount of data transferred enables reduce the power consumption of the whole system.
- Still picture area, such as an icon, can be updated while displaying motion pictures combining with the system interface (for details, refer to “GRAM ACCESS VIA RGB INTERFACE AND SPI” described later).

The RGB interface is performed in synchronization with VSYNC, HSYNC, and DOTCLK.
Window Address Function enables transfer only the screen to be updated and reduce the power consumption.

In the period between the completion of displaying one frame data and the next VSYNC signal, the display status will remain in front porch period.

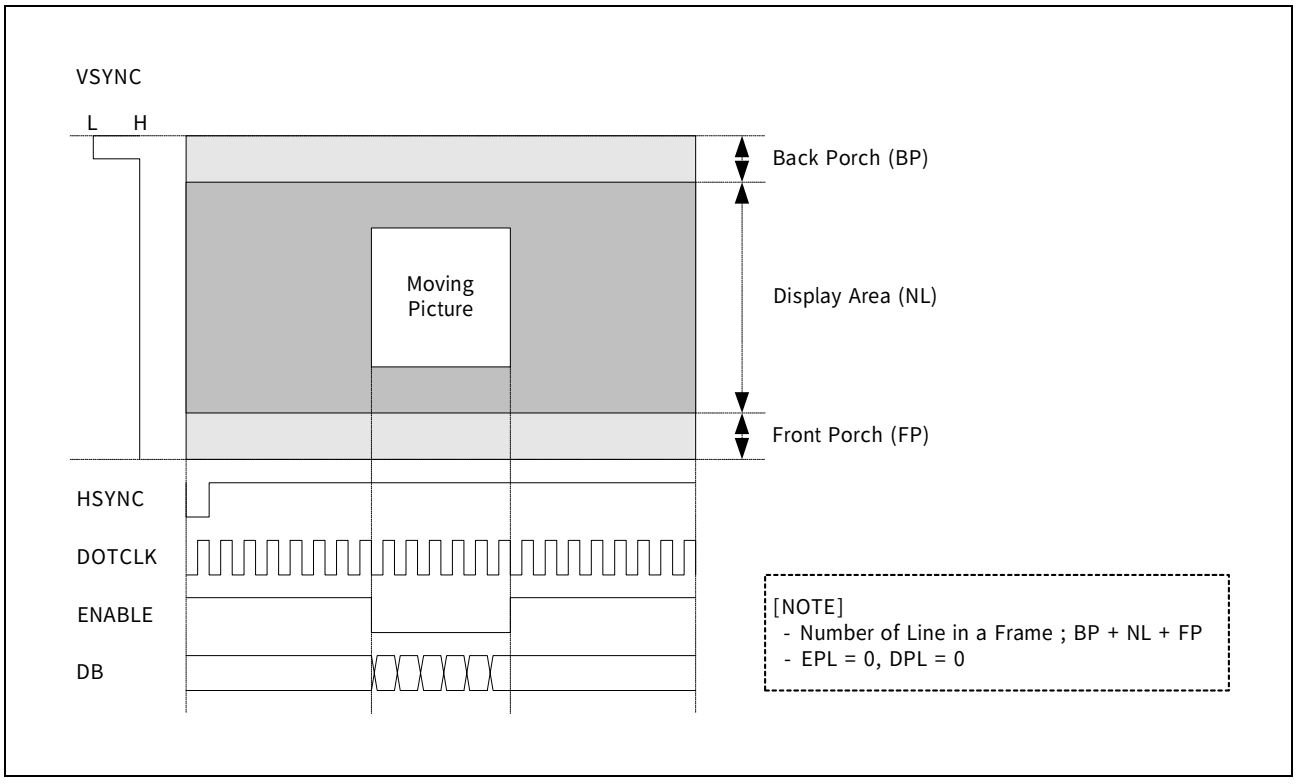


Figure 77. RGB Interface

Note. For RGB interface, VSYNC, HSYNC, DOTCLK should be supplied at much higher resolution than that of panel.

There are three timing conditions for RGB Interface that is determined according to RIM and each condition is described below.

12.2.2. 18BIT RGB INTERFACE

Bit Assignment

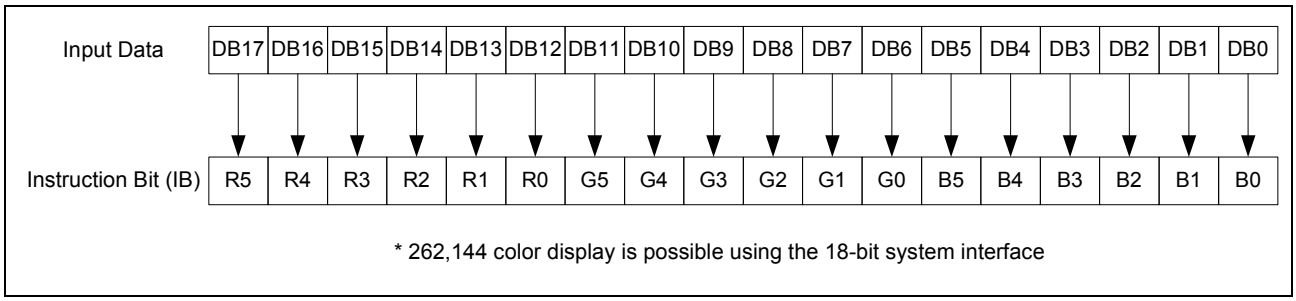


Figure 78. Bit Assignment of GRAM Data on 18bit RGB Interface

Timing Diagram

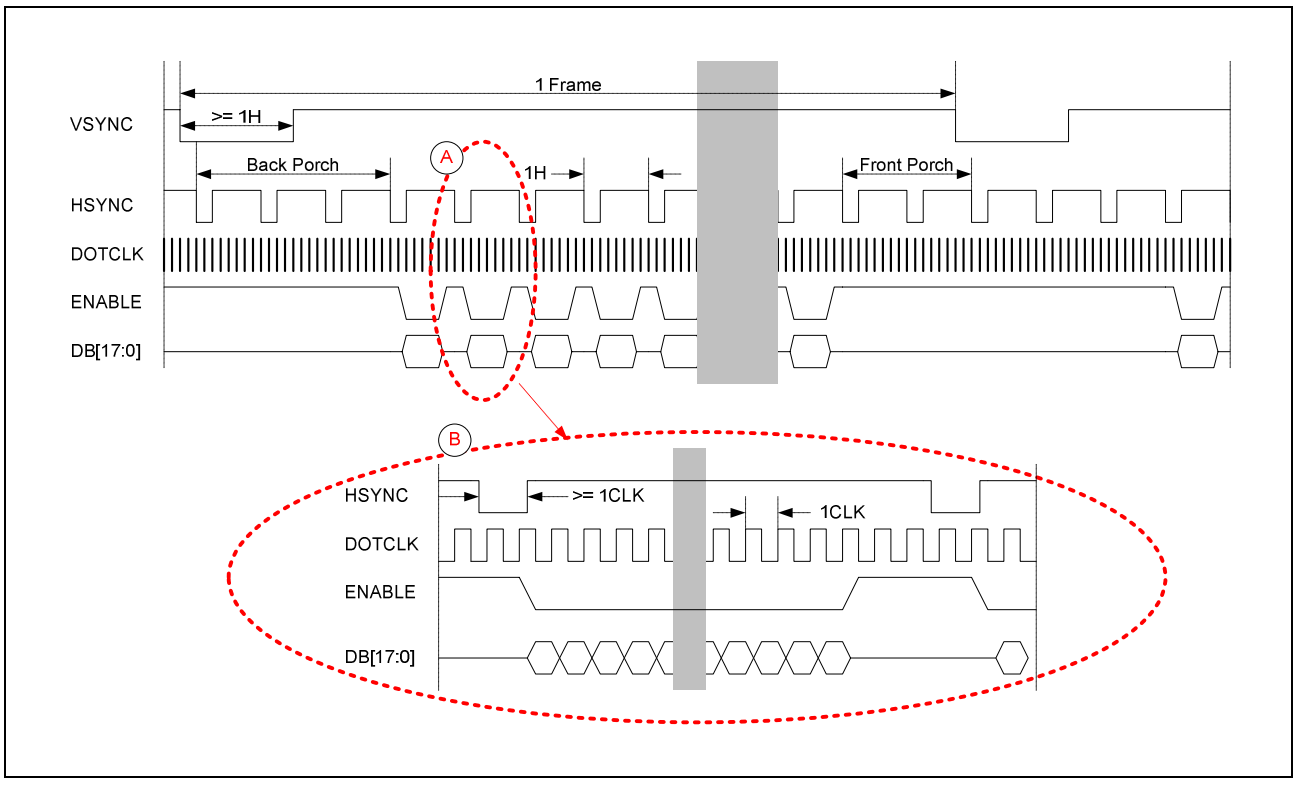


Figure 79. Timing Diagram of 18/16bit RGB Interface

12.2.3. 16BIT RGB INTERFACE

Bit Assignment

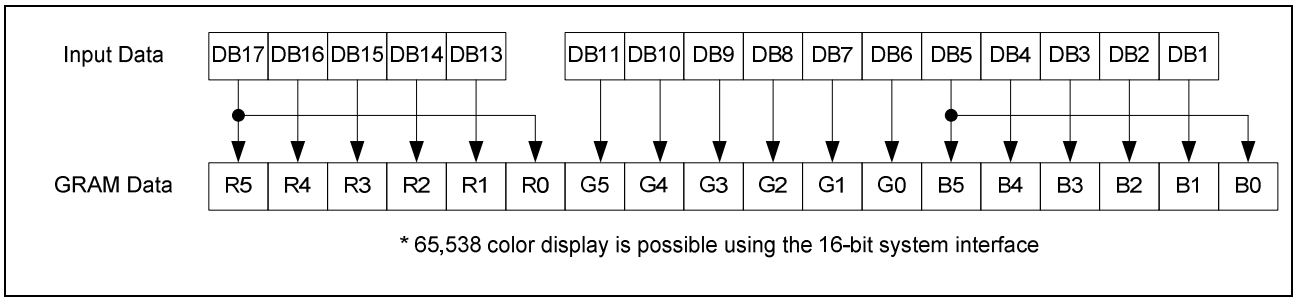


Figure 80. Bit Assignment of GRAM Data on 16bit RGB Interface

Timing Diagram

There are two timing conditions for RGB Interface that is determined according to RIM.

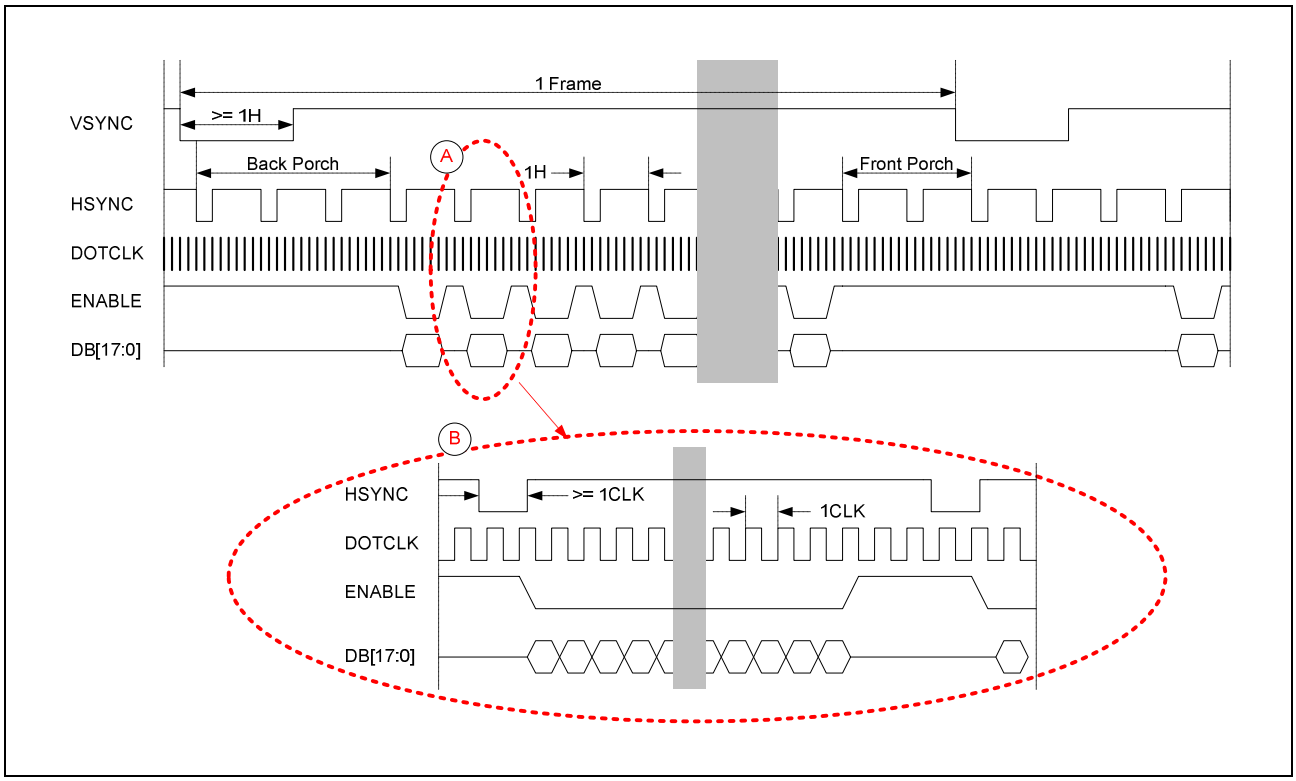


Figure 81. Timing Diagram of 18/16bit RGB Interface

12.2.4. 6BIT RGB INTERFACE

In order to transfer data on 6bit RGB Interface there should be three transfers.

Bit Assignment

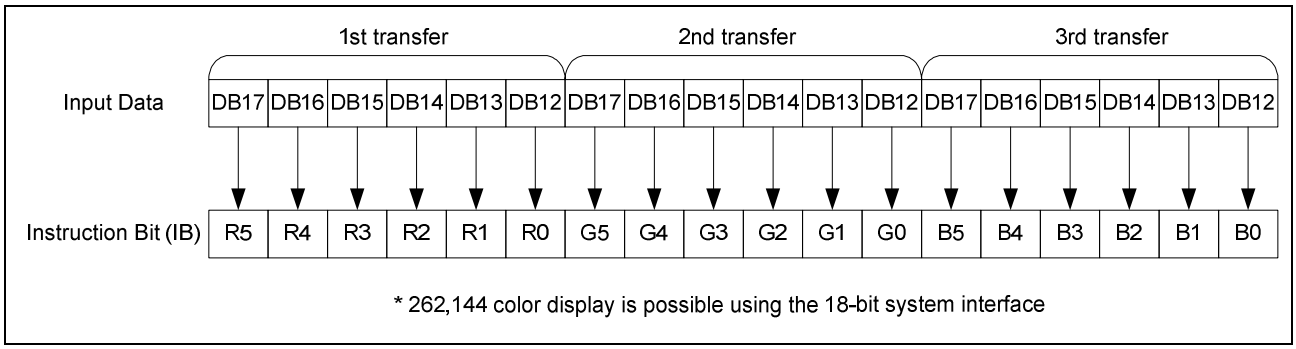


Figure 82. Bit Assignment of GRAM Data on 6bit RGB Interface

Timing Diagram

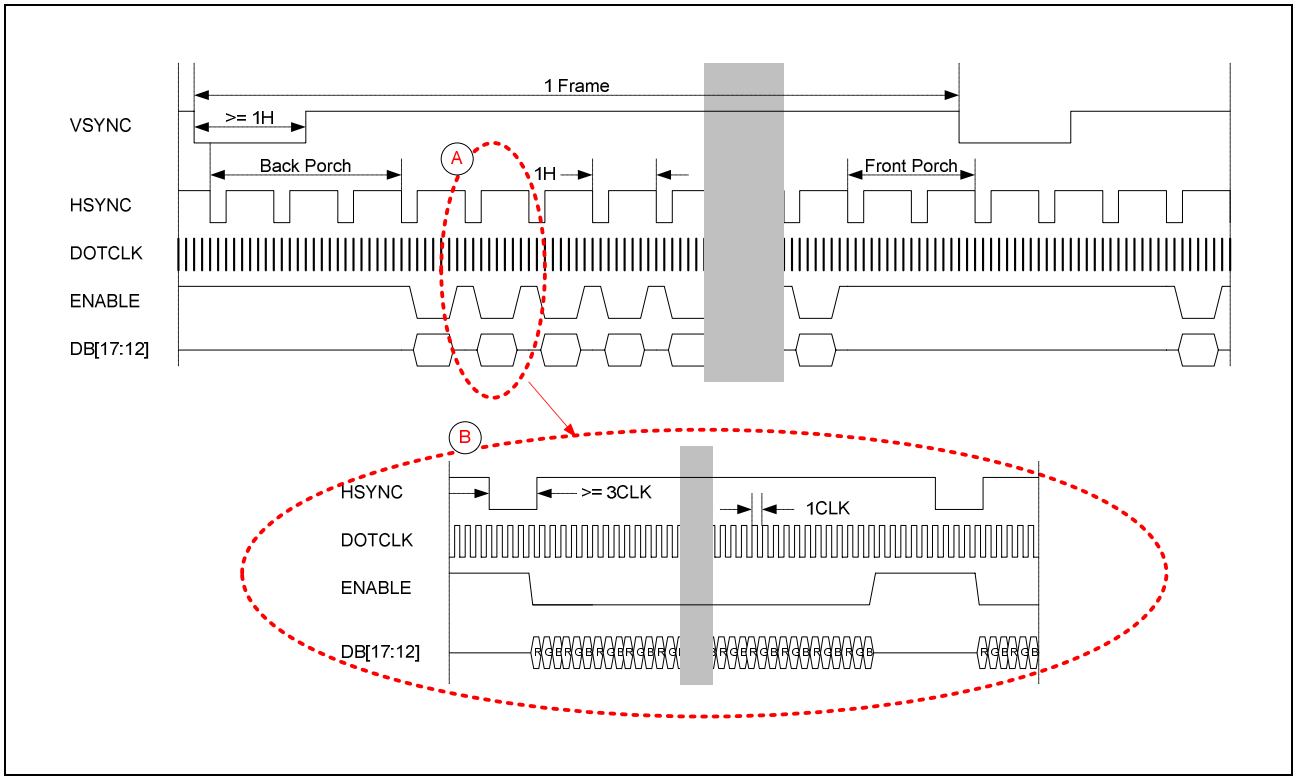


Figure 83. Timing Diagram of 6bit RGB Interface

Note.

Three clocks are regarded as one clock for transfer when data is transferred in 6-bit interface.

VSYNC, HSYNC, ENABLE, DOTCLK, and DB [17:12] should be transferred in units of three clocks.

Transfer Synchronization

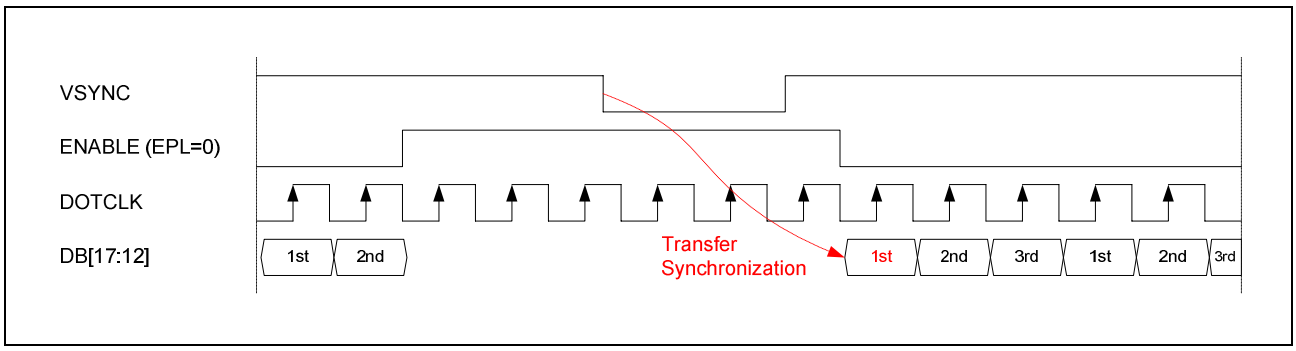


Figure 84. Transfer Synchronization Function in 6-bit RGB Interface mode

Note. The figure above shows Transfer Synchronization functions for 6bit RGB Interface. S6D0154 has a transfer counter internally to count 1st, 2nd and 3rd data transfer of 6bit RGB Interface. The transfer counter is reset on the falling edge of VSYNC and enters the 1st data transmission state. Transfer mismatch can be corrected at every VSYNC signal assertion. In this method, when data is consecutively transferred in for displaying motion pictures, the effect of transfer mismatch will be reduced and recovered by normal operation.

Note. The display is operated in units of three DOTCLKs. When DOTCLK is not input in units of pixels, clock mismatch occurs and the frame, which is operated, and the next frame are not displayed correctly.

12.3. INTERFACE SWAPPING FOR MEMORY ACCESS

12.3.1. DISPLAY MODES AND GRAM ACCESS CONTROL

Display mode and RAM Access is controlled as shown below. For each display status, display mode control and RAM Access control are combined properly.

Table 45. DISPLAY MODE & RAM ACCESS CONTROL

Display Status	GRAM Access (RM)	Display Mode (DM)
1. Still Picture Display	System Interface (RM = 0)	Internal Clock Operation (DM[1:0] = 00)
2. Motion Picture Display	RGB Interface mode 1 (RM = 1)	External Clock Operation (DM[1:0] = 01)
	RGB Interface mode 2 (RM = 1)	External Clock Operation (DM[1:0] = 11)
3. Rewrite Still Picture while Motion Picture is being displayed	System Interface (RM = 0)	External Clock Operation (DM[1:0] = 01 or 11)

Note.
Only system interface can set Instruction register.
When the RGB Interface is being operated, do not change the RGB Interface mode (RIM).

12.3.2. Internal Clock Operation mode with System Interface (1)

Every operation in Internal Clock Operation mode is done in synchronization with the internal clock which is generated by internal OSC. The signals input through RGB interface are all meaningless. Access to internal GRAM is done via system interface.

12.3.3. External Clock Operation mode with RGB Interface (2)

In External Clock Operation mode, frame sync signal (VSYNC), line sync signal (HSYNC) and DOTCLK are used for display operation. Display data is transferred in the unit of pixel through DB bus and saved to GRAM.

12.3.4. External Clock Operation mode with System Interface (3)

Write GRAM data via system interface even in External Clock Operation mode. There should not be any data transmission on RGB interface in this case. To restart data transmission on RGB interface, set RM to “1”, set memory address properly and write index of 22h for GRAM write operation.

With the combination of Window Address function, motion picture and still picture may be saved in separated GRAM regions respectively. In this case motion picture and still picture are displayed simultaneously.

12.3.5. GRAM ACCESS VIA RGB INTERFACE AND SPI

All the data for display is written to the internal GRAM in S6D0154 when RGB interface is in use. In this method, data, including motion picture and screen update frame, can only be transferred via RGB interface.

With Window Address function, power consumption can be reduced and high-speed access can be achieved while motion pictures are being displayed. Data for display that is not in the motion picture area or the screen update frame can be written via System Interface.

GRAM can be accessed via SPI even when RGB interface is in use. To do that ENABLE should be inactive state to stop data writing via RGB interface, because the write operation to GRAM is always performed in synchronization with DOTCLK while ENABLE is active state. Then you may write any data through SPI. After this access to GRAM via SPI, a waiting time is needed for a write/read bus cycle before the next RAM access starts via RGB interface. When a RAM write conflict occurs, data writing is not guaranteed.

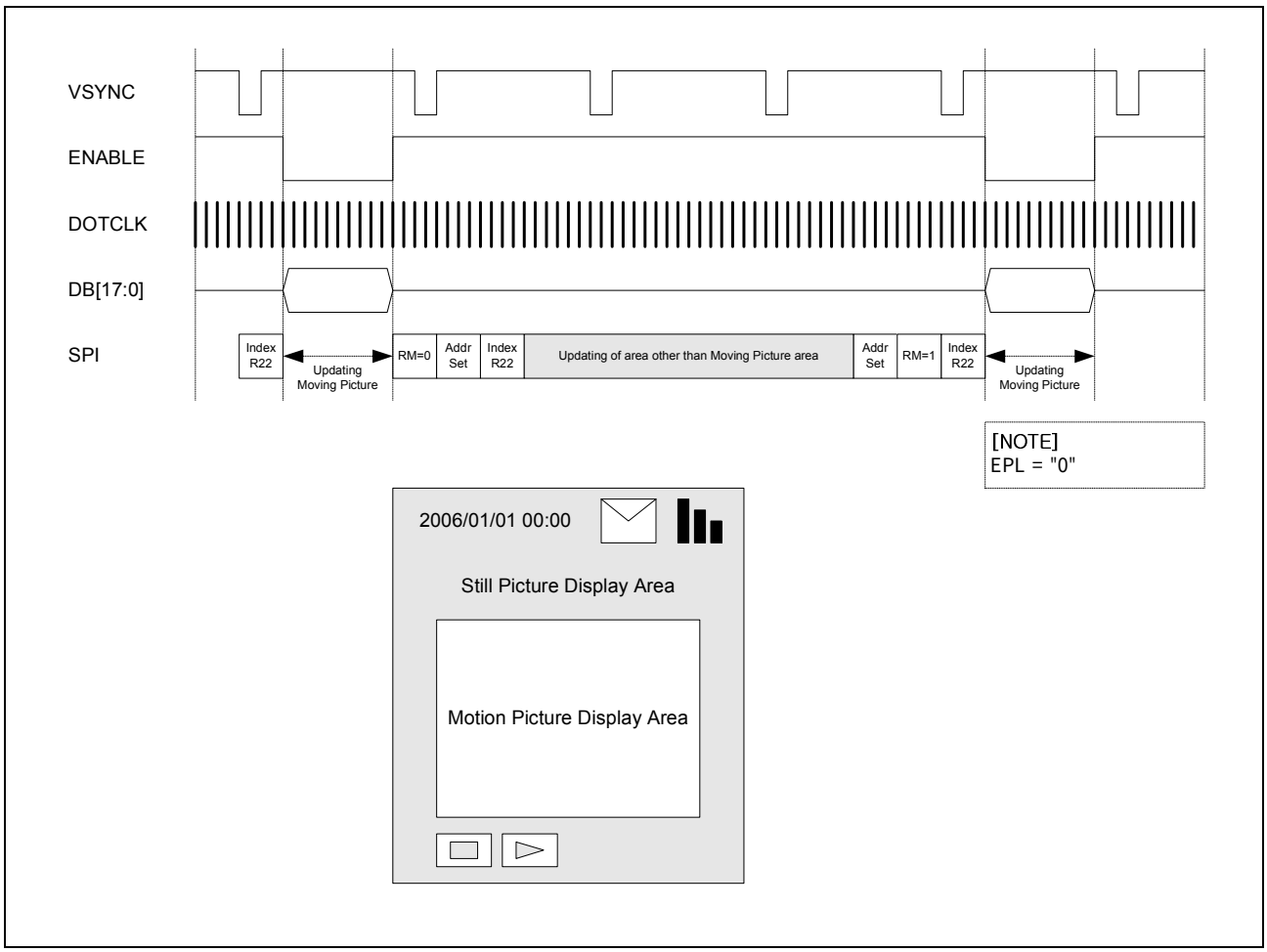


Figure 85. GRAM Access through RGB Interface and SPI

12.3.6. TRANSITION SEQUENCES BETWEEN DISPLAY MODES

Transitions between Internal Clock Operation mode and External Clock Operation mode should follow the mode transition sequence shown below.

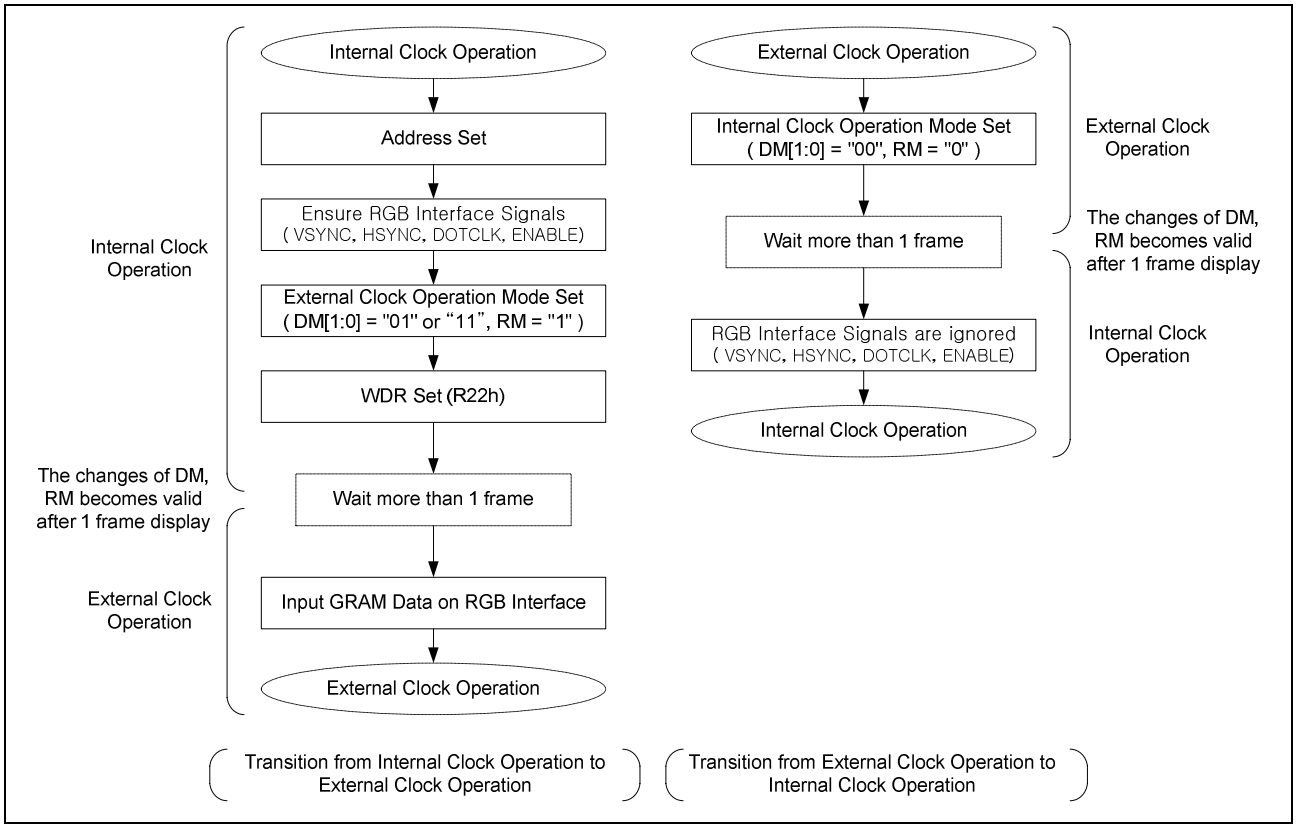


Figure 86. Transition between Internal Clock Operation Mode and External Clock Operation Mode

13. MDDI (Mobile Display Digital Interface)

13.1. Introduction to MDDI

The S6D0154 supports MDDI, mobile display driver interface. The physical layer of MDDI is based on a high-speed, differential serial interface. Both command and image data transfer can be achieved with MDDI. MDDI host & client are linked by Data and STB line. Through Data line, either command or image data is transferred from MDDI host to MDDI client, and vice versa. Data is transferred by packet unit.
Through STB line, strobe signal is transferred. When the link is in “FORWARD direction”, data is transferred from host to client; in “REVERSE direction”, client transfers data to MDDI host.

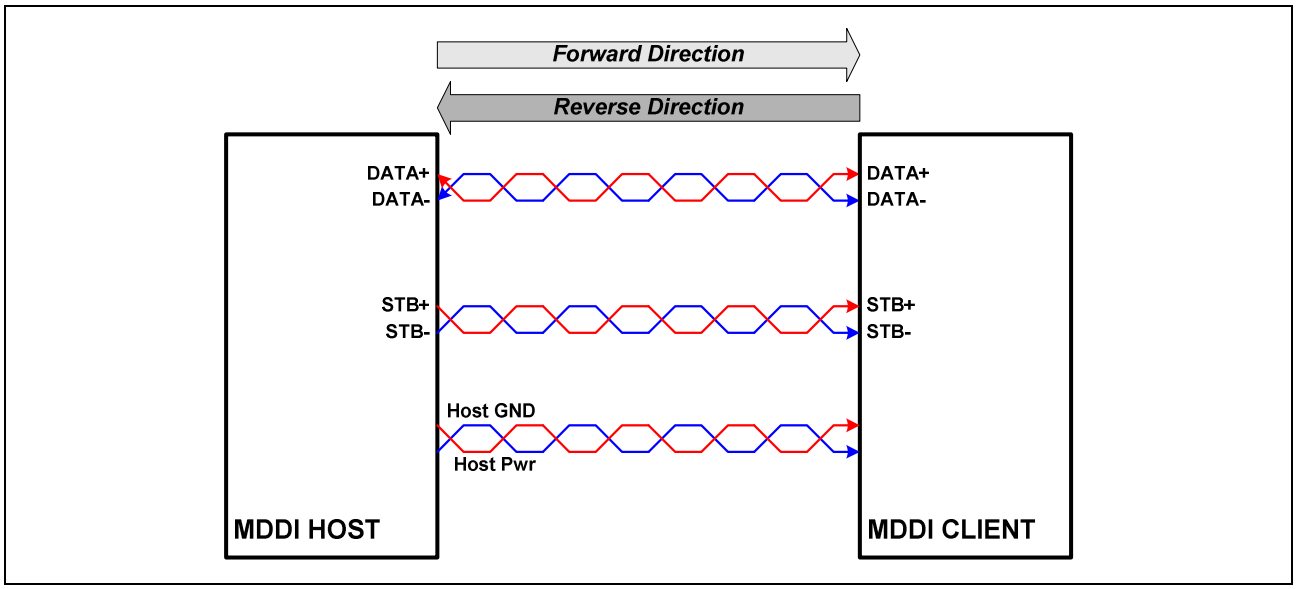


Figure 87. Physical connection of MDDI host and client

13.2. DATA-STB Encoding

Data is encoded using a DATA-STB method. Data signal is bi-directional over a pair of differential cable while STB signal is uni-directional over a pair of differential cable driven by a host as show in Figure 73. Figure below illustrates how the data sequence “1110001011” is transmitted using DATA-STB encoding.

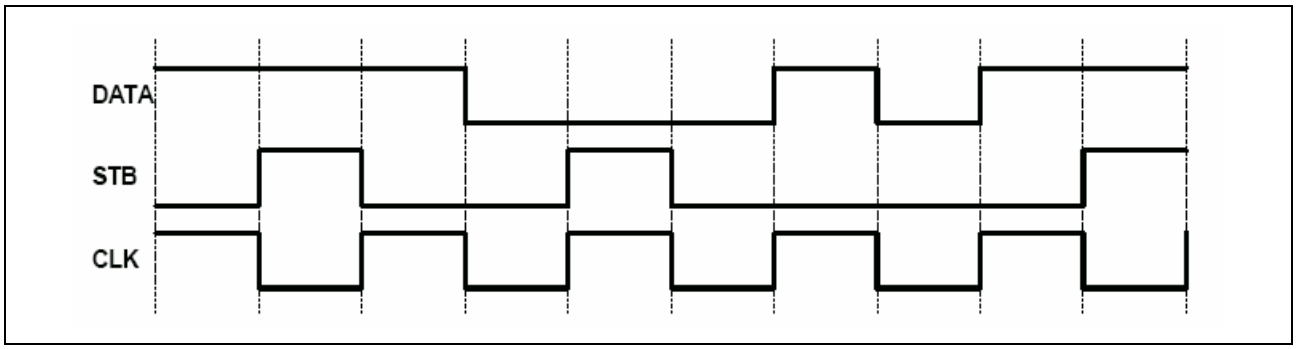


Figure 88. Data-STB encoding

The Following figure shows a sample circuit to generate DATA and STB from input data, and then recover the input data from DATA and STB.

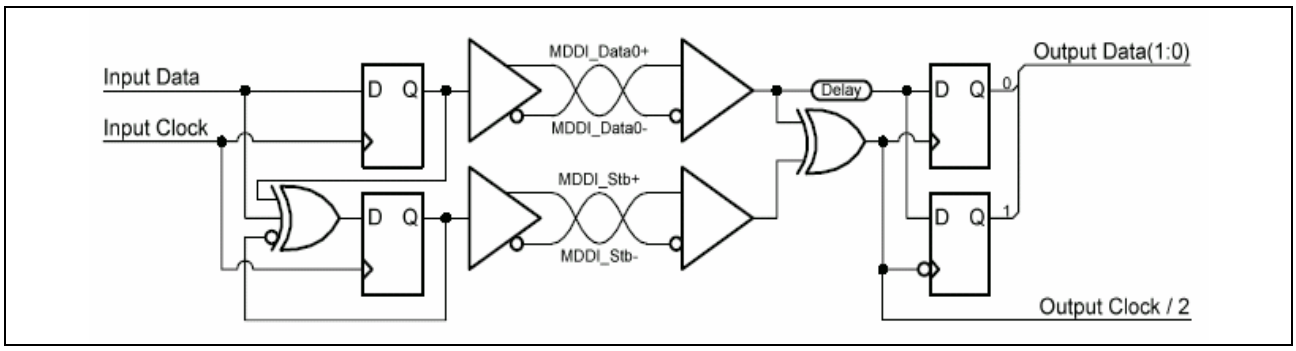


Figure 89. Data / STB Generation & Recovery circuit

13.3. MDDI Data & STB

The Data (MDP/MDN) and STB (MSP/MSN) signals are always operated in a differential mode to maximize noise immunity. Each differential pair is parallel-terminated with the characteristic impedance of the cable. Figure below illustrates the configuration of the drivers, receivers, and terminations. The driver of each signal pair has a differential current output. While receiving MDDI packets the MDDI_DATA and MDDI_STB pairs use a conventional differential receiver with a differential voltage threshold of zero volts. In the hibernation state the driver outputs are disabled and the parallel termination resistors pull the differential voltage on each signal pair to zero volts. During hibernation a special receiver on the MDDI_DATA pairs has an offset input differential voltage threshold of positive 125 mV, which causes the hibernation line receiver to interpret the un-driven signal pair as logic-zero level.

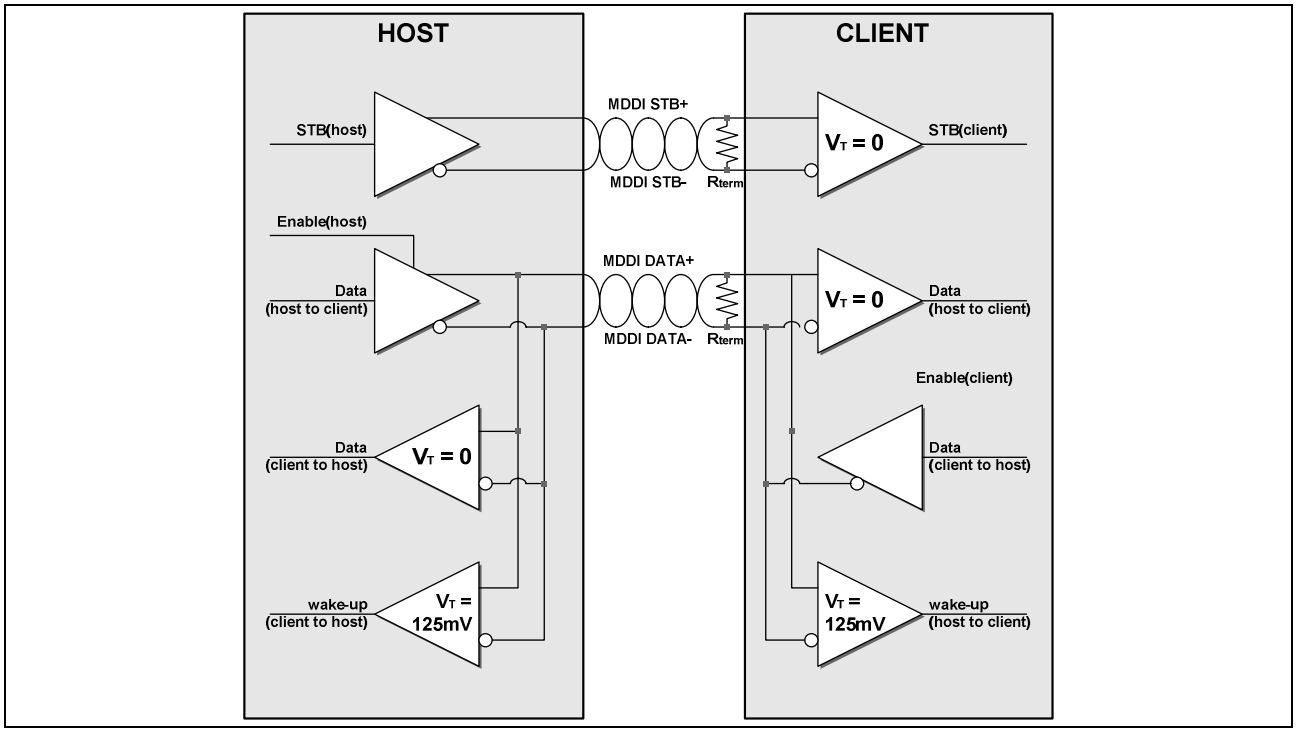


Figure 90. Differential connection between host and client

13.4. MDDI PACKET

MDDI transfer data in a packet format. MDDI host can generate and send packets.

In S6D0154, several packet formats are supported. Packets are transferred from MDDI host to client (forward direction); but reverse encapsulation packet is transferred from MDDI client to host (reverse direction).

A number of packets, started by sub-frame header packet, constructs 1 sub frame.

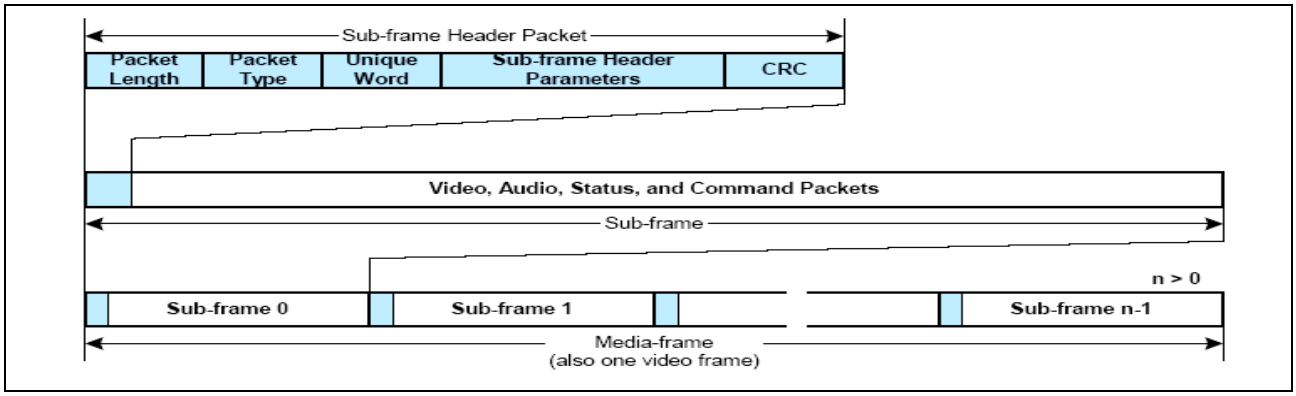


Figure 91. MDDI packet structure

Refer to MDDI packet structure, sub-frame header packet is placed in front of a sub-frame, and some sub-frame construct media-frame together.

The following table describes 9 types of packet which is supported in S6D0154.

Packet	Function	Direction
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Client request and status packet	Information about client status	Reverse
Link shutdown packet	End of frame	Forward

Sub-frame header packet

packet length	packet type = 3bffh	unique word = 005ah	reserved1	sub-frame length	protocol version	sub-frame conut	media frame count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type (sub-frame header packet is 3bffh)
unique word : Identify "This packet is sub-frame header packet"
reserved1 : not used (set zero)
sub-frame length : specifies number of bytes per sub-frame
protocol version : set all zero
sub-frame count : specifies number of sub-frame header packet
mddi frame count : specifies number of media frames
CRC : error check

Figure 92. Sub-frame header packet structure

Register access packet

packet length	packet type = 146	bClient ID	Read/Write Info	Register Address	Paramter CRC	Register Data List	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	4 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type(Register Access packet is 146(decimal))
bClient ID : set to all zero
Read/Write Info : to write register value, bits[15:14] = "00"
to request register value, bits[15:14] = "10"
bits[13:0] is all zero
Register Address : Register address is written here.
Parameter CRC : To check error from packet length to register address
Register Data List : Paramter data is written here.
CRC : To error check register data list.

Figure 93. Register access packet structure

Video Stream packet

packet length	packet type=16	bClientID	video data format descriptor	pixel data attributes	X left edge	Y top edge	X right edge	Y bottom edge	X start	Y start
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

pixel count	parameter CRC	pixel data	pixel data CRC
2 bytes	2 bytes	packet length - 26 bytes	2 bytes

packet length : packet length not including packatet length block
packet type : packet type(video stream packet is 16)
bClientID : reserved, set all 0
video data format descriptor : bits[15:13] = 010 : raw RGB format(fixed value)
bits[12] = 1 : Only packed type is available(fixed value)
bits[11:0] = 0110_0110_0110 : 18 bit pixel
bits[11:0] = 0101_0110_0101 : 16 bit pixel
pixel data attributes : bits[1:0] = 11 : displayed both eyes(fixed value)
bits[5] = 1 : X left edge .. Y start edge is not defined.(fixed value)
other bits are all zero.
X left edge : Not used in S6D0154, set all zero.
Y top edge : Not used in S6D0154, set all zero.
X right edge : Not used in S6D0154, set all zero.
Y bottom edge : Not used in S6D0154, set all zero.
X start : Not used in S6D0154, set all zero.
Y start : Not used in S6D0154, set all zero.
Pixel count ; Write number of pixel.
Paramter CRC : To error check from packet length to pixel count.
pixel data : pixel data info. number of pixel data must not be over 65509.
pixel data CRC : To pixel data error check.

Figure 94. Video stream packet structure

Filler packet

packet length	packet type = 0	filler bytes (all zero)	CRC
2 bytes	2 bytes	packet length - 4 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type(Filler packet is 0(decimal))
filler bytes : set to all zero(The size is under packet length availabe)
CRC : To error check

Figure 95. Filler packet structure

Link shutdown packet

packet length	packet type = 69	CRC	All zeros
2 bytes	2 bytes	2 bytes	16 bytes

packet length : packet length not including packet length block
packet type : packet type(Link shutdown packet is 69(decimal))
CRC : To error check
All zeros : write all zero (size is 16 bytes)

Figure 96. Link shutdown packet structure

: fixed value

For More information about MDDI packet, refer to VESA MDDI spec.

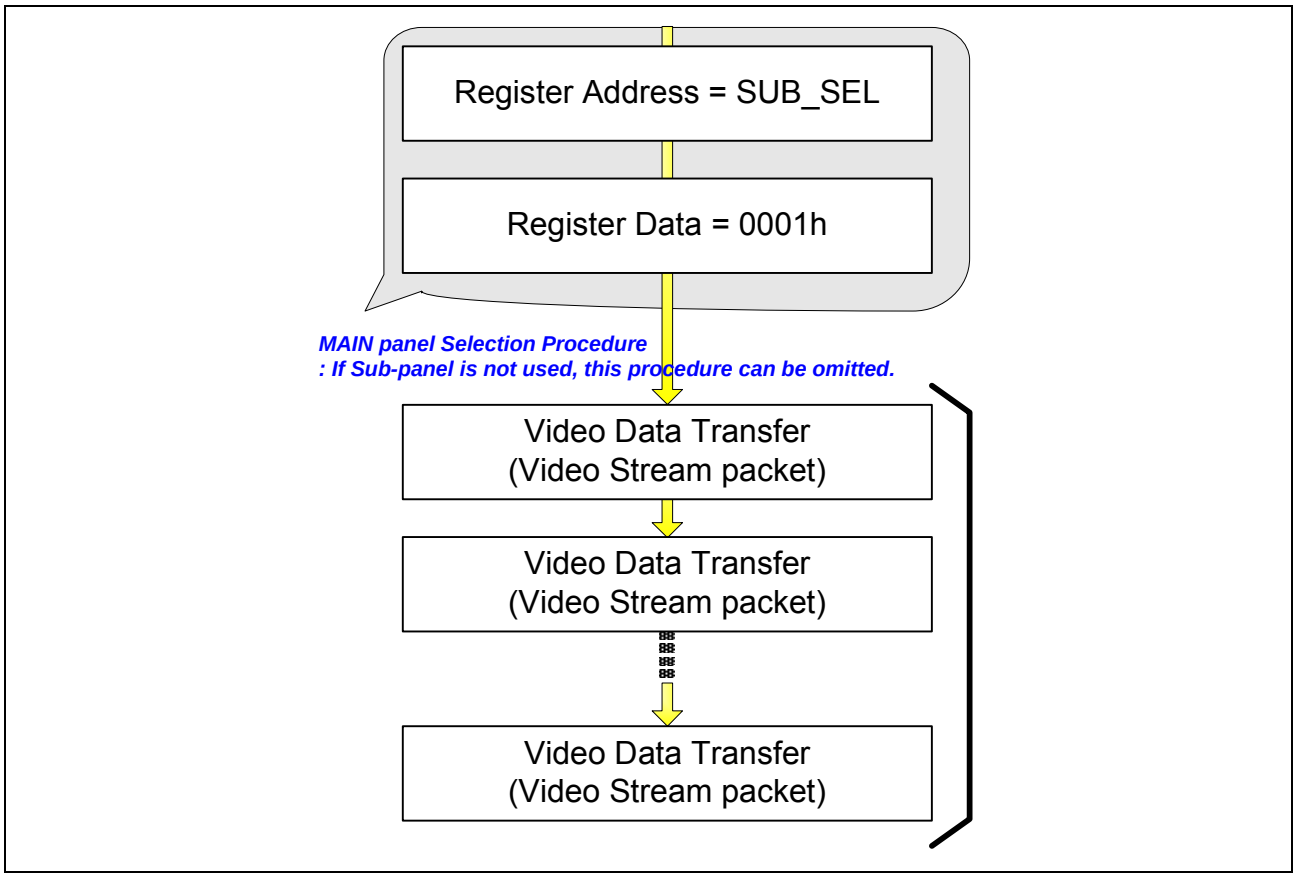
13.5. Main Panel Control

S6D0154 supports video stream packet for memory write and register access packet for register write/read. Followings are some examples of memory and register write/read sequence.

13.5.1. Writing video data to memory sequence

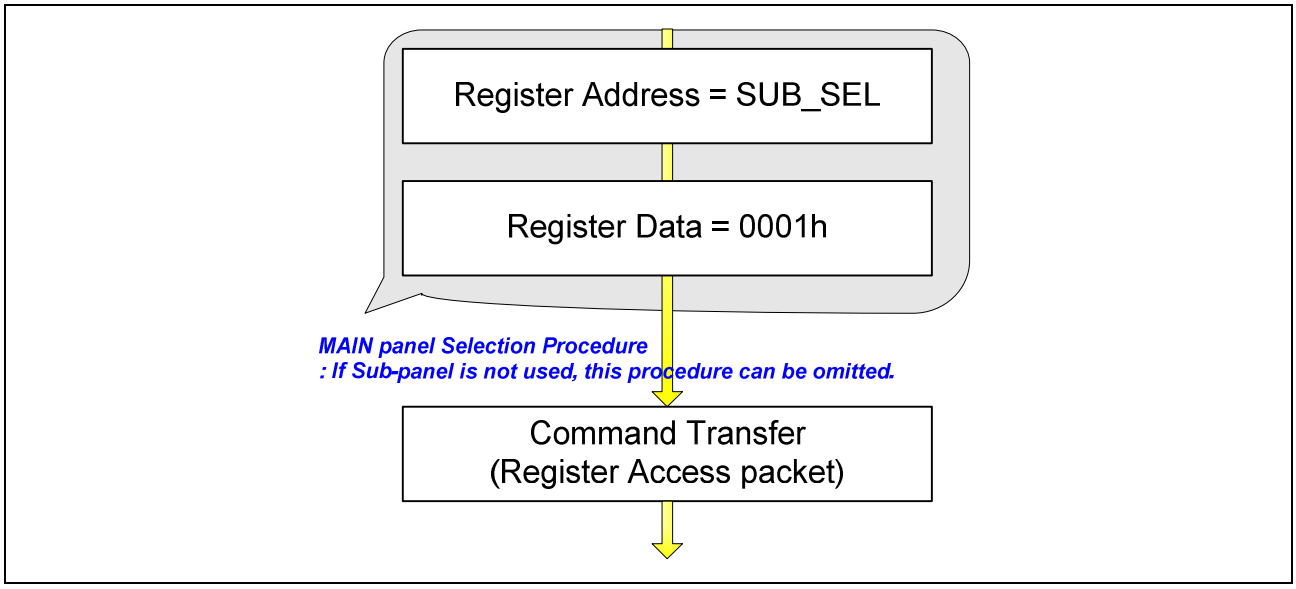
In order to write video data to memory, the following sequence should be programmed. First, main panel should be selected if sub-panel is controlled by MDDI interface. This procedure can be omitted if sub-panel is not used.

This packet should be followed by video stream packets.



13.5.2. Writing register sequence

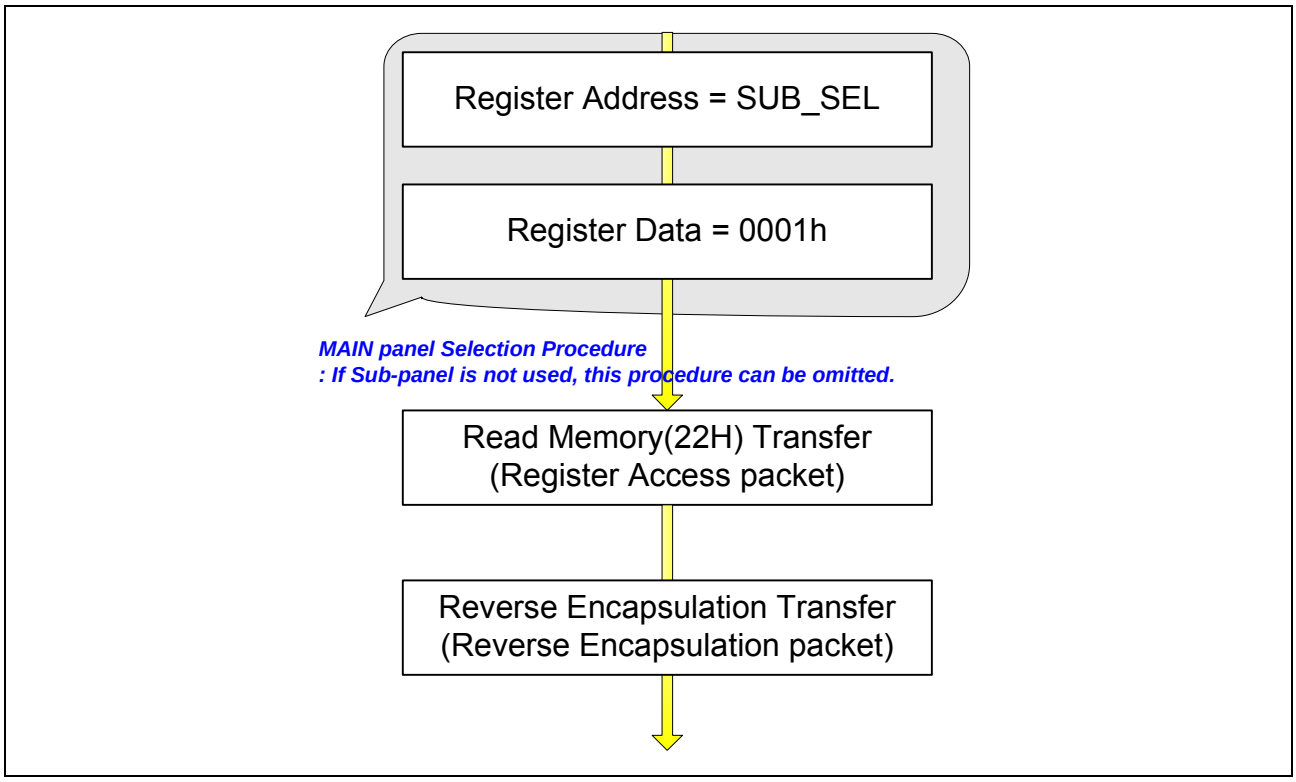
In order to write registers, register access packet should be used. First, main panel should be selected if sub-panel is controlled by MDDI interface. This procedure can be omitted if sub-panel is not used. Next, register access packet is used to write data to register.



13.5.3. Reading video data from memory sequence

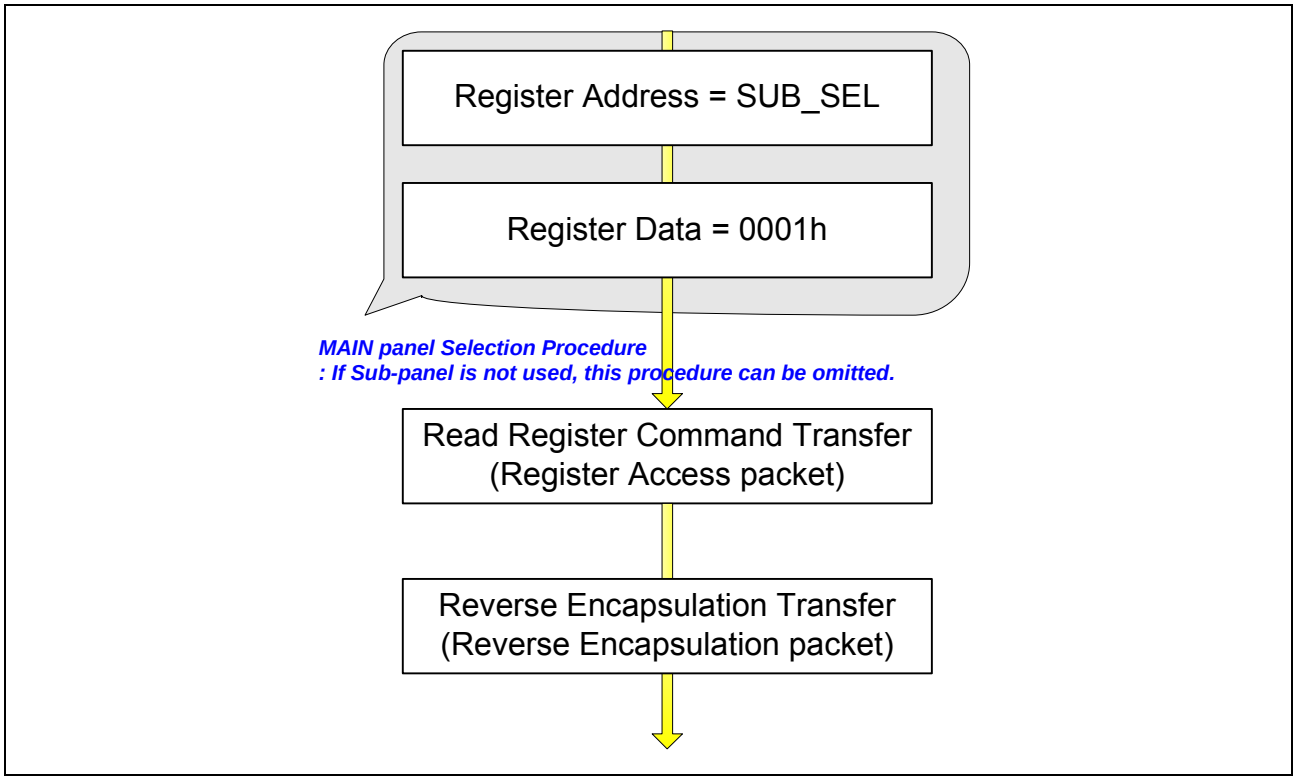
In order to read pixel data from memory, the following sequence should be programmed. First, main panel should be selected if sub-panel is controlled by MDDI interface. This procedure can be omitted if sub-panel is not used.

Next, memory read command (22H) is followed by reverse encapsulation packet. DDI transmits video pixel data through encapsulation packet. Please refer to VESA spec for detailed description.



13.5.4. Reading register sequence

In order to read registers, the following sequence should be programmed. First, main panel should be selected if sub-panel is controlled by MDDI interface. This procedure can be omitted if sub-panel is not used. Next, register read command is followed by reverse encapsulation packet. DDI transmits register data through encapsulation packet. Please refer to VESA spec for detailed description.



13.6. TEARING-LESS DISPLAY

In S6D0154, the matching between data writes timing and written data display timing is important. If timing is mismatched, tearing effect can occur.

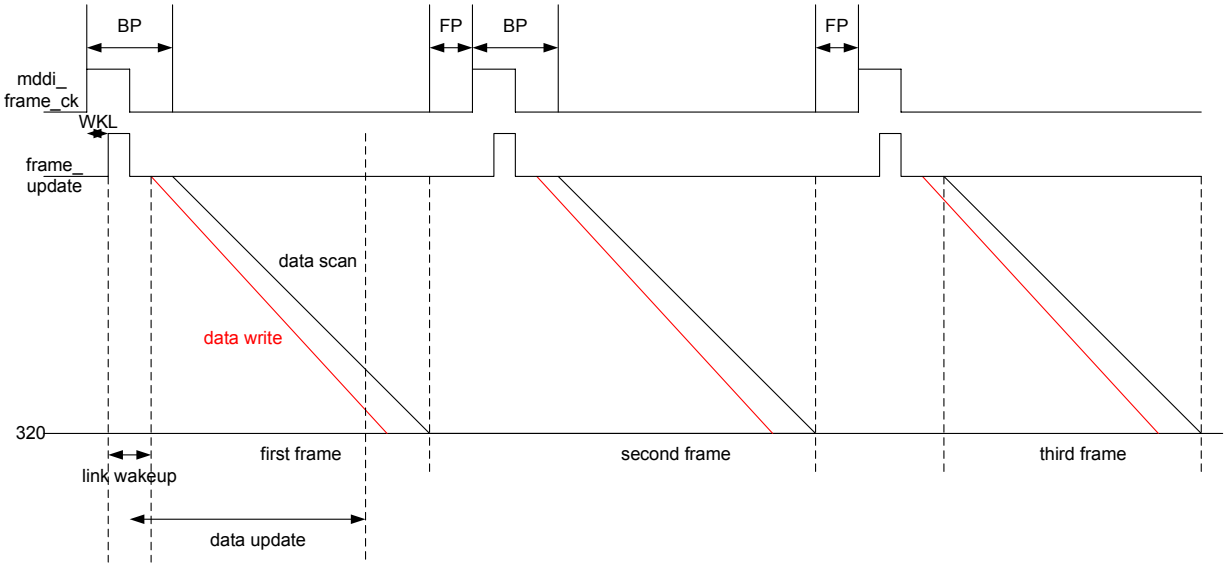
To avoid display tearing effect, two possible ways are suggested.

First case is that data write is slower than speed of displaying written data. In this case, data write speed is not critical, but current consumption in interface will be increased because data transfer time is long. Data write time is selected widely in this case.

Other case is that data write is faster than speed of displaying written data. In this case, data update speed is very high so that transfer time is short. So current consumption in interface can be minimized, but it requires fast data transfer. The most important thing is to avoid data scan conflicts with data update.

The following figures describe some examples to avoid display tearing phenomenon.

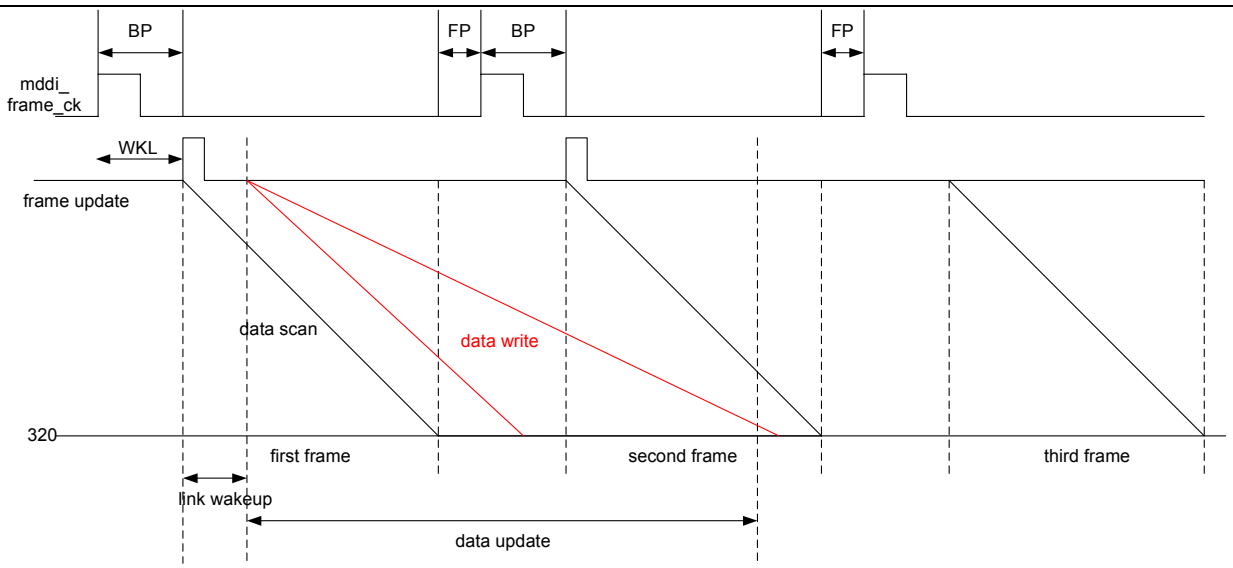
A. Display speed is slower than data write.



WKL is to set previously than data scan, and consider the time that reverse time from client to host to send request signal.

Figure 97. Tearing-less display: data write speed is faster than display

B. Display speed is faster than data write.



WKL is to set later than data scan, and consider that data write is to be completed before next data scan is completed.

Figure 98. Tearing-less display: display speed is faster than data write

13.7. HIBERNATION / WAKE-UP

S6D0154 support hibernation mode to save interface power consumption. MDDI link can enter the hibernation state quickly and wake up from hibernation quickly. This allows the system to force MDDI link into hibernation frequently to save power consumption.

During hibernation mode, hi-speed transmitters and receivers are disabled and low-speed & low-power receivers are enabled to detect wake-up sequence.

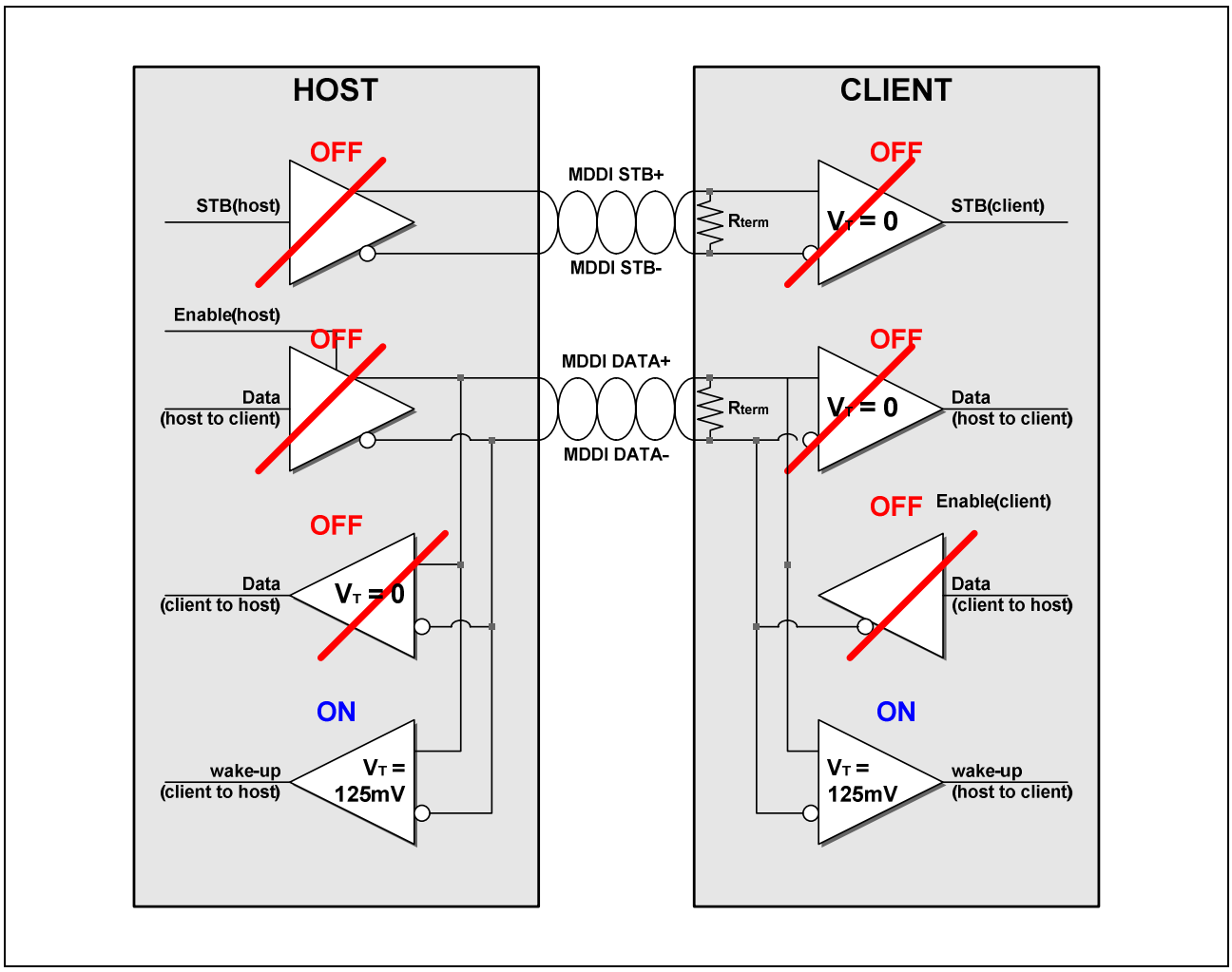


Figure 99. MDDI Transceiver / Receiver state in hibernation

When the link wakes up from hibernation the host and client exchange a sequence of pulses. These pulses can be detected using low-speed, low-power receivers that consume only a fraction of the current of the differential receivers required to receive the signals at the maximum link operating speed.

Either the client or the host can wake up the link; Host-initiated link wakeup and Client-initiated link wakeup.

13.8. MDDI LINK WAKE-UP Procedure

Host-initiated Link Wake-up Procedure

The simple case of a host-initiated wake-up is described below without contention from the client trying to wake up at the same time. The following sequence of events is illustrated in the following figure.

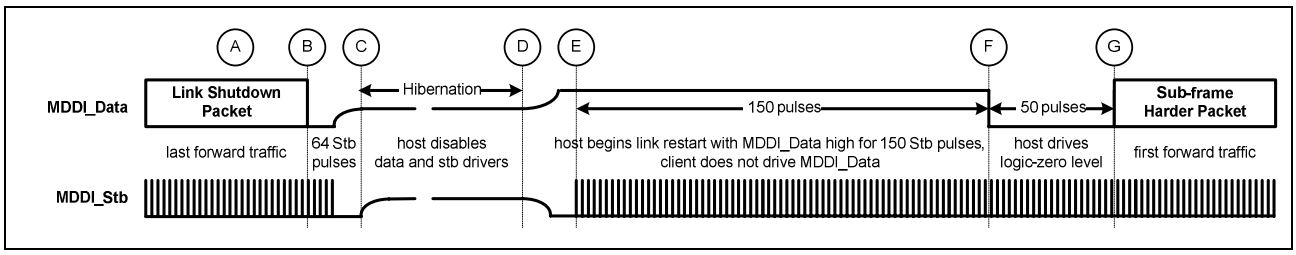


Figure 100. Host-initiated link wakeup sequence

The Detailed descriptions for labeled events are as follows:

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data to a logic-zero level, and then disables the MDDI_Data output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC.

It may be desirable for the client to place its high-speed receivers for MDDI_Data and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

C. The host enters the low-power hibernation state by disabling the MDDI_Data and MDDI_Stb drivers and by placing the host controller into a low-power hibernation state.

It is also allowable for MDDI_Stb to be driven to logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.

D. After a while, the host begins the link restart sequence by enabling the MDDI_Data and MDDI_Stb driver outputs. The host drives MDDI_Data to a logic-one level and MDDI_Stb to logic-zero level for at least the time it takes for the drivers to fully enable their outputs.

The host shall wait at least 200 nsec after MDDI_Data reaches a valid logic-one level and MDDI_Stb reaches a valid logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb. The client first detects the wake-up pulse using a low-power differential receiver having a +125mV input offset voltage.

E. The host drivers are fully enabled and MDDI_Data is being driven to a logic-one level. The host begins to toggle MDDI_Stb in a manner consistent with having logic-zero level on MDDI_Data for duration of 150 MDDI_Stb cycles.

F. The host drives MDDI_Data to logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data is at logic-zero level for 40 MDDI_Stb cycles.

G. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet. Beginning at point G the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data so that proper data-strobe encoding commences from point G.

Client-initiated Link Wake-up Procedure

An example of a typical client-initiated service request event with no contention is illustrated in the following figure.

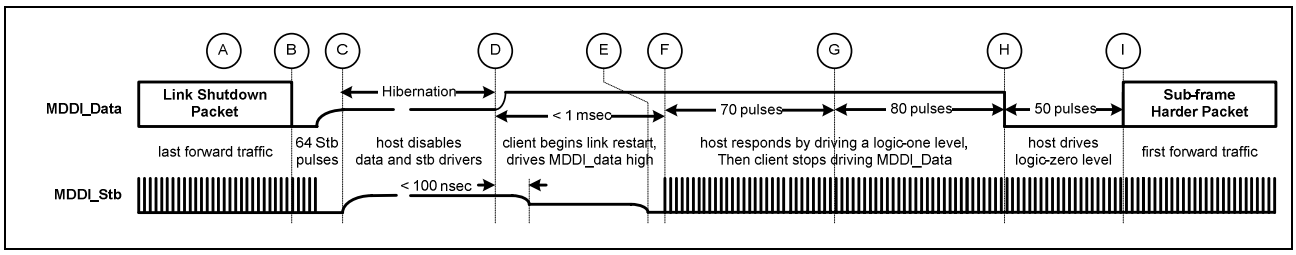


Figure 101. Client-initiated link wake-up sequence

The Detailed descriptions for labeled events are as follows:

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data to a logic-zero level, and then disables the MDDI_Data output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

C. The host enters the low-power hibernation state by disabling its MDDI_Data and MDDI_Stb driver outputs. It is also allowable for MDDI_Stb to be driven to logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.

D. After a while, the client begins the link restart sequence by enabling the MDDI_Stb receiver and also enabling an offset in its MDDI_Stb receiver to guarantee the state of the received version of MDDI_Stb is a logic-zero level in the client before the host enables its MDDI_Stb driver. The client will need to enable the offset in MDDI_Stb immediately before enabling its MDDI_Stb receiver to ensure that the MDDI_Stb receiver in the client is always receiving a valid differential signal and to prevent erroneous received signals from propagating into the client. After that, the client enables its MDDI_Data driver while driving MDDI_Data to a logic-one level. It is allowed for MDDI_Data and MDDI_Stb to be enabled simultaneously if the time to enable the offset and enable the standard MDDI_Stb differential receiver is less than 200 nsec.

E. Within 1 msec the host recognizes the service request pulse, and the host begins the link restart sequence by enabling the MDDI_Data and MDDI_Stb driver outputs. The host drives MDDI_Data to a logic-one level and MDDI_Stb to a logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_Data reaches a valid logic-one level and MDDI_Stb reaches a valid fully-driven logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb.

F. The host begins outputting pulses on MDDI_Stb and shall keep MDDI_Data at a logic-one level for a total duration of 150 MDDI_Stb pulses through point H. The host generates MDDI_Stb in a manner consistent with sending a logic-zero level on MDDI_Data. When the client recognizes the first pulse on MDDI_Stb it shall disable the offset in its MDDI_Stb receiver.

G. The client continues to drive MDDI_Data to a logic-one level for 70 MDDI_Stb pulses, and the client disables its MDDI_Data driver at point G. The host continues to drive MDDI_Data to a logic-one level for duration of 80 additional MDDI_Stb pulses, and at point H drives MDDI_Data to logic-zero level.

H. The host drives MDDI_Data to logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data is at logic-zero level for 40 MDDI_Stb cycles.

I. After asserting MDDI_Data to logic-zero level and driving MDDI_Stb for duration of 50 MDDI_Stb pulses the host begins to transmit data on the forward link at point I by sending a Sub-frame Header Packet.
The client begins to look for the Sub-frame Header Packet after MDDI_Data is at logic-zero level for 40 MDDI_Stb cycles.

13.9. GPIO CONTROL

S6D0154 offers up to 6 GPIOs that can be used as input or output independently.
User may control 6 GPIOs as input or output by use of simple register setting.

The following table shows several set of registers for GPIO.

Register	width	Description	Reset value	Register
GPIO (44h)	[5:0]	Write	For GPIO output mode: output GPIO register(44h) value to GPIO PAD	6'b000000
		Read	GPIO PAD status	
GPIO_CON (45h)	[5:0]	Write	GPIO PAD input/output mode control : (0 : input / 1 : output)	6'b000000
		Read	GPIO_CON (45h) register value	
GPCLR (46h)	[5:0]	Write	For GPIO input mode: clear specified GPIO interrupt (set by GPIO PAD input).	6'b000000
		Read	GPIO interrupt state (set by GPIO PAD input).	
GPIO_EN (47h)	[5:0]	Write	For GPIO input mode: enable specified GPIO interrupt	6'b000000
		Read	GPIO_EN (47h) register value.	
GPPOL (48h)	[5:0]	Write	For GPIO input mode: GPIO interrupt polarity setting	6'b111111
		Read	GPPOL (48h) register value.	

In GPIO output mode, the IC outputs GPIO (44h) register value to the designed PAD. Set GPIO_CON register as output mode before use GPIO output.

6 different GPIO outputs can be controlled simultaneously using 1-register access packet (44h register access) so that minimum access time for each GPIO output will be 1-register access time.

GPIO input mode can only be used as client-initiated link wake-up. For more information, refer to GPIO based link wake-up section.

13.10. Client-Initiated Link Wake-up

S6D0154 supports 2-types of client-initiated link wake-up: VSYNC based Link Wake-up & GPIO based Link Wake-up. As client-initiated wake-up action is executed in hibernation state only, register setting for each wake-up have to be set before link shut-down.

VSYNC Based Link Wake-up

In display-ON state, when the IC finishes displaying all internal GRAM data, data request must be transferred to MDDI host for new video data. As MDDI link is usually in hibernation for reducing interface power consumption, MDDI link wake-up must be done before internal GRAM update. In that case, client initiated link wake-up can be used as data request.

When VSYNC based link wake-up register (40h: VWAKE_EN) is set, client initiated wake-up is executed in synchronization with the vertical-sync signal which generated in S6D0154. Using VSYNC based link wake-up, tearing-less display can be accomplished if interface speed and wake-up time is well known.

The following figure shows detailed timing for VSYNC based link wake-up.

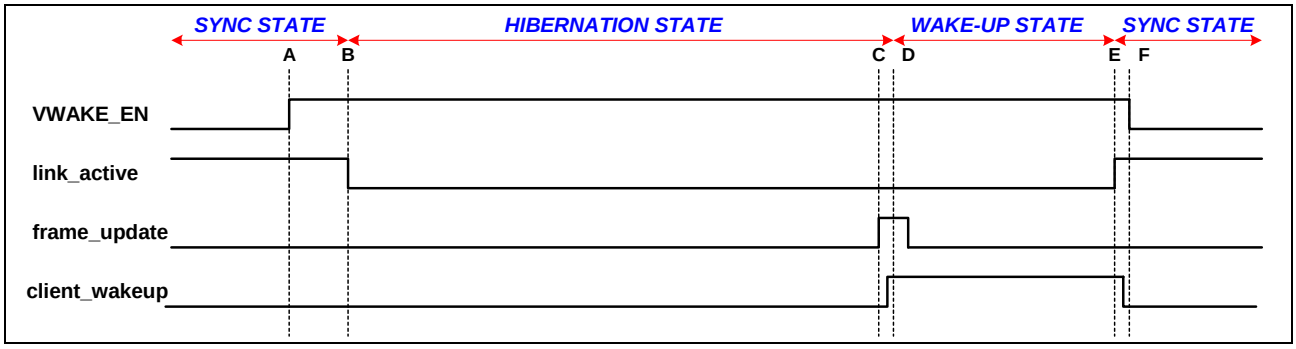


Figure 102. VSYNC based link wake-up procedure

The Detailed descriptions for labeled events are as follows:

A. MDDI host writes to the VSYNC based link wakeup register to enable a wake-up based on internal vertical-sync signal.

B. link_active goes low when the host puts in the link into hibernation after no more data needs to be sent to the S6D0154.

C. frame_update, the internal vertical-sync signal goes high indicating that update pointer has wrapped around and is now reading from the beginning of the frame buffer. Link wake-up can be set using WKF and WKL (41h) registers. WKF specifies the number of frame before wake-up; WKL specifies the number of lines before wake-up.

D. client_wakeup input to the MDDI client goes high to start the client initiated link wake-up.

E. link_active goes high after the host brings the link out of hibernation.

F. After link wake-up, client_wakeup signal and the VWAKE_EN register are cleared automatically.

13.11. GPIO Based Link Wake-up

In VSYNC-based link wake-up, wake-up enable register setting prior to link shut-down. GPIO based Link wake-up is enabled by interrupt from outside of the IC. For GPIO based link wake-up, GPIO interrupt enable and GPIO PAD mode (to input mode) setting must be set. Once S6D0154 receive interrupt, internal GPIO base link wake-up flag set to high, and the following procedure is similar to that of VSYNC based link wake-up.

The following figure shows detailed timing for GPIO based link wake-up.

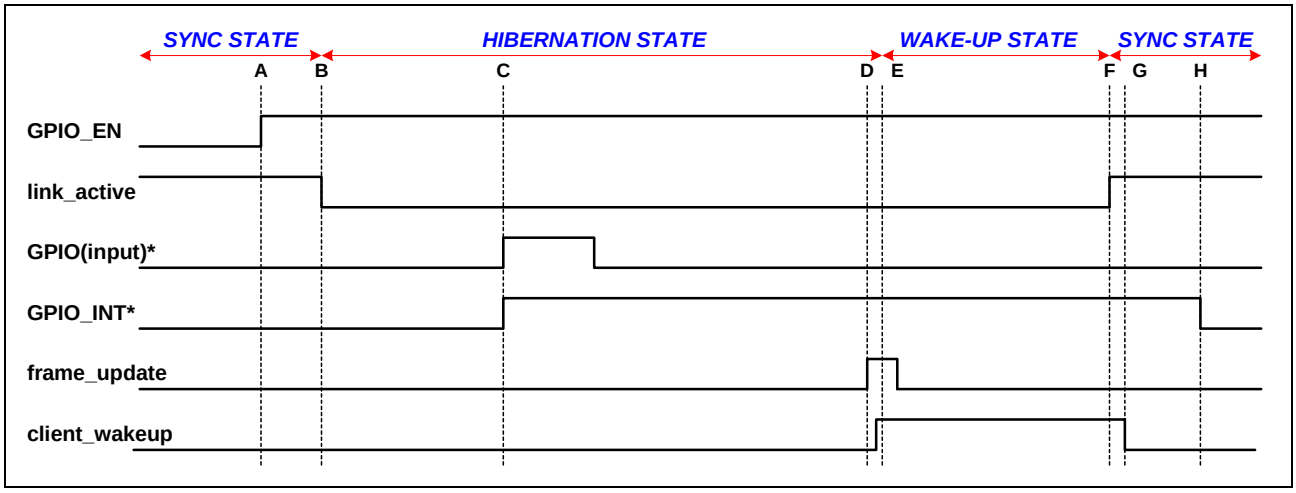


Figure 103. GPIO based link wake-up procedure

The detail descriptions for labeled events are as follows:

A. Host sets the GPIO interrupt enable register (47h: GPIO_EN) for a particular GPIO through register access packet.

B. Link goes into hibernation (and link_active goes low) when the host has no more data to send to the IC.

C. GPIO input goes high, and the GPIO interrupt (GPIO_INT) is latched.

D. Frame_update signal goes high indicating that the display has wrapped around. Link wake-up can be set using WKF and WKL (41h) registers.

E. Client_wakeup input to the MDDI client goes high to start the client initiated link wake-up.

F. Link_active goes high after the host brings the link out of hibernation.

G. After link wake-up, client_wakeup signal is reset to low.

H. MDDI host clears the interrupt by writing to the interrupt clear register with the bit set for that particular interrupt (GPCLR: 46h). Between point G and H the host will have read the GPIO_INT values to see what interrupts are active.

13.12. MDDI OPERATION

In MDDI, six operation modes are available. The following table describes six modes.

STATE	OSC	Step-up Circuit	Internal Logic status	MDDI I/O	Wake-up by
SLEEP	ON	Disabled	Display OFF /Internal Logic ON MDDI Link hibernation	Hibernation driver ON	Host – Initiated
WAIT	ON	Disabled	Display OFF /Internal Logic ON MDDI Link in SYNC	standard driver ON	-
Normal	ON	Enabled	Display ON /Internal Logic ON MDDI Link in SYNC	standard driver ON	-
NAP	ON	Disabled	Display OFF /Internal Logic ON MDDI Link in SYNC	standard driver ON	-
IDLE	ON	Enabled	Display ON /Internal Logic ON MDDI Link hibernation	Hibernation driver ON	Host – Initiated Client –Initiated (Vsync, GPIO)
STOP	OFF	Disabled	Display OFF /Internal Logic ON MDDI Link OFF	Driver All OFF	RESET

SLEEP: Initial status when external power is connected to the IC. In this state, internal oscillator is operating, and MDDI link is in hibernation state. As no command or signal is applied to the IC except RESET input and step-up circuit is OFF, and internal logic is ON.

WAIT: After the wake-up sequence, the IC is in WAIT state. MDDI link is in SYNC, and internal logic is ON, and step-up is still OFF because no other register access or video stream packet is transferred to the IC.

NORMAL: MDDI link, step-up circuit, and internal logic circuit is ON. Register access or Video data transfer is available in NORMAL state.

IDLE: When no more video data update is needed, MDDI link is in hibernation so that interface power can be reduced. Internal step-up & logic circuits are still operating. MDDI link wakeup will be accomplished when vsync wakeup register is set before hibernation or GPIO interrupt is set.

NAP: This state is set by register access. Step-up is OFF, but MDDI link is ON. MDDI link and internal logic have to be in SYNC because the IC must receive commands for power save or normal operation

STOP: STOP state is set by register access (10h). In this state, MDDI link, internal oscillator, step-up are all OFF and internal logic is still ON. To release STOP state, input reset signal. After reset, status is SLEEP state.

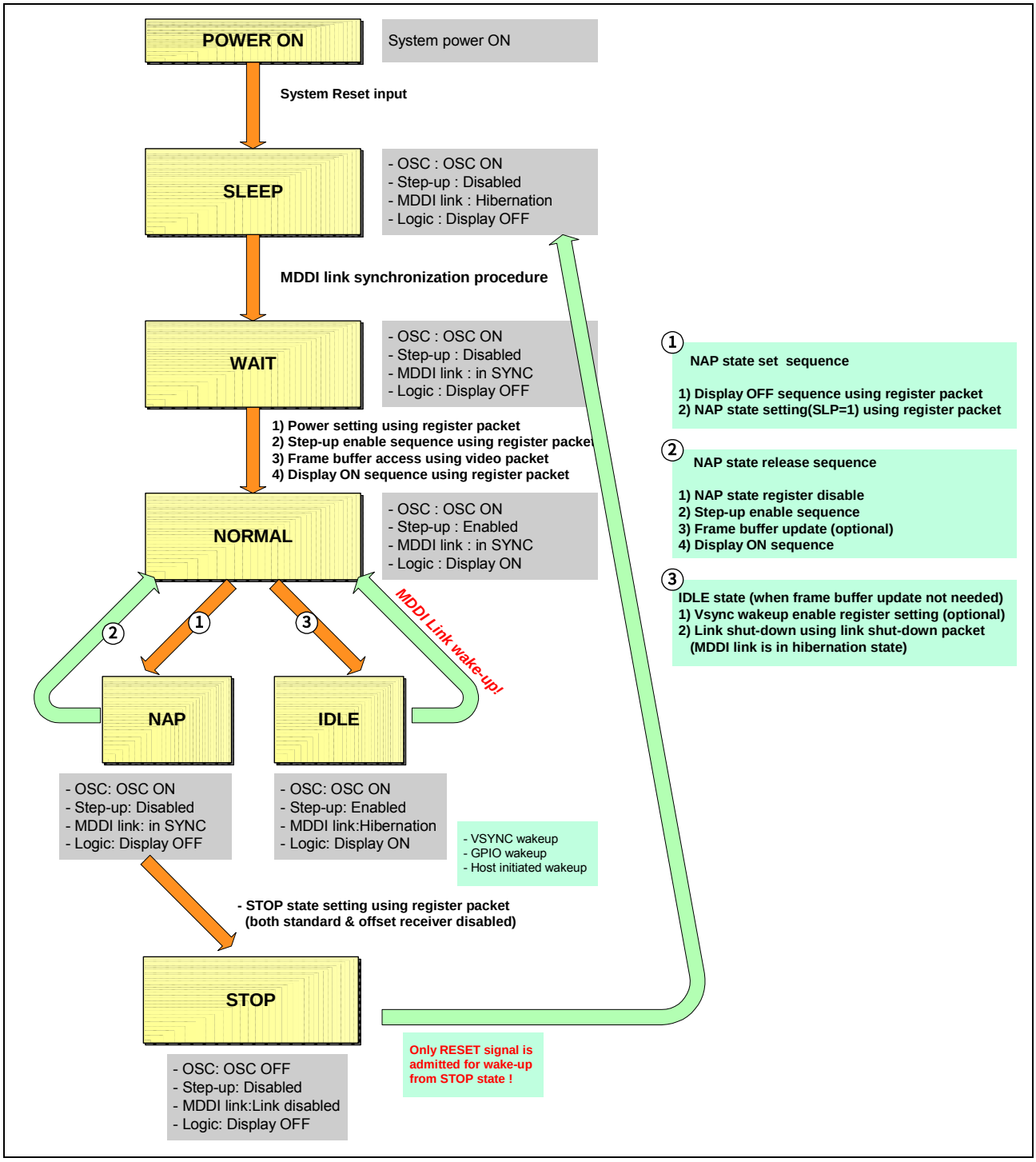


Figure 104. Operating state in MDDI mode

13.13. SUB PANEL CONTROL

S6D0154 supports sub panel control function which controls a sub panel driver IC using 80-Series protocol (CSB, RS, WRB & DB). When MDDI host (Base band modem) sends several packets to S6D0154, and the packet is for sub panel, the IC converts the packet to 80-Series protocol & sends them to sub panel driver IC. So separated interface line for sub panel control are not needed. After all, S6D0154 enables the sub panel driver IC which doesn't support MDDI to be applied to the system.

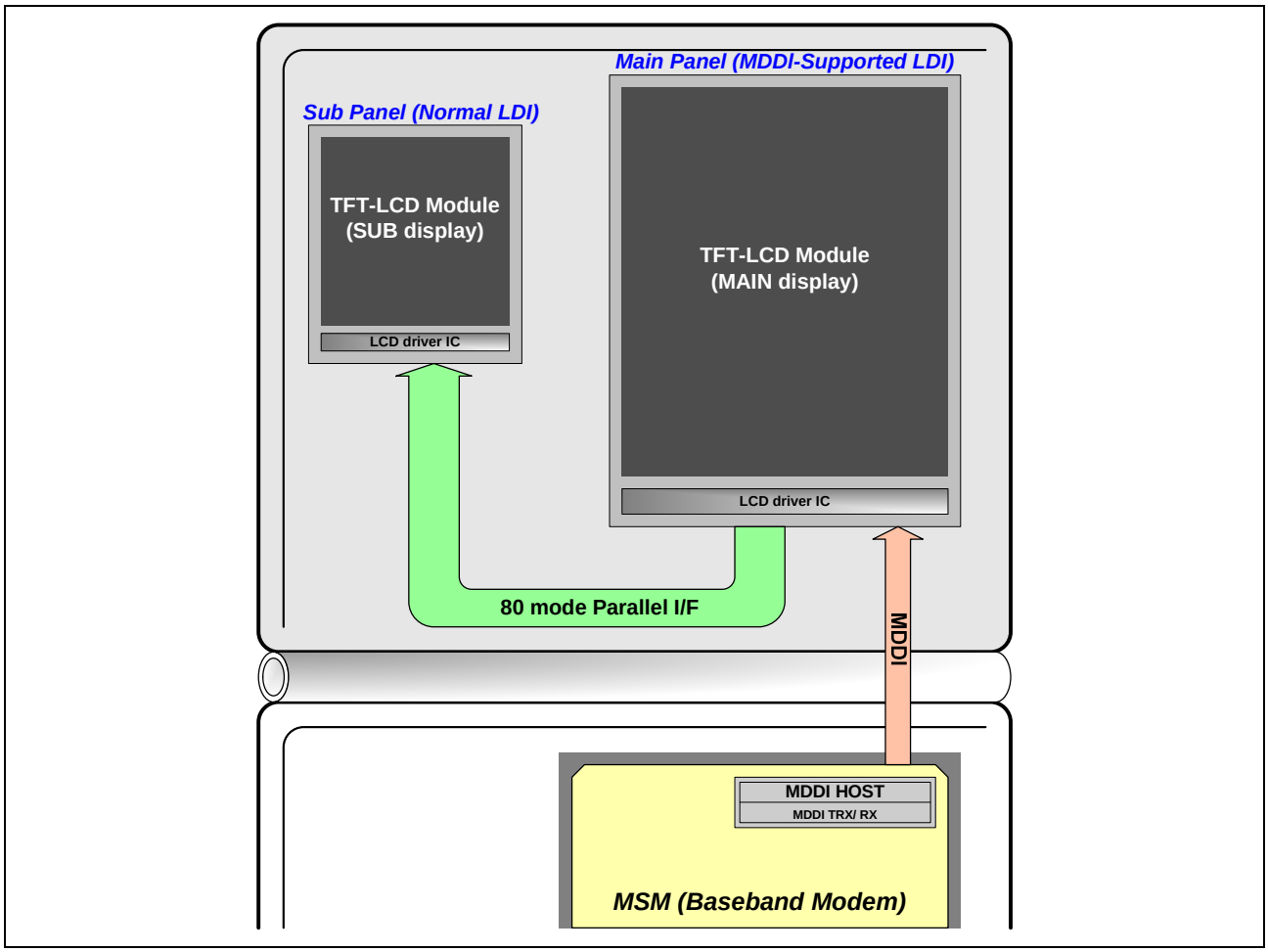


Figure 105. Schematic diagram of sub panel control function

13.14. Main / Sub panel Selection

Using 42h register (4Ah address can be changed using SUB_SEL register), main / sub panel data path can be selected. When S6D0154 receives register access packet (Initially 4Ah index) from MDDI host, it decodes the packet and checks the last bit of the register data field is '1' or '0'. If the last bit is '0', the following register access packet or video stream packet is transferred to the sub panel control signal generation block.

Sub panel selection address (Initially 4Ah) can be changed using SUB_SEL register. Do not change the SUB_SEL value to previously occupied address.

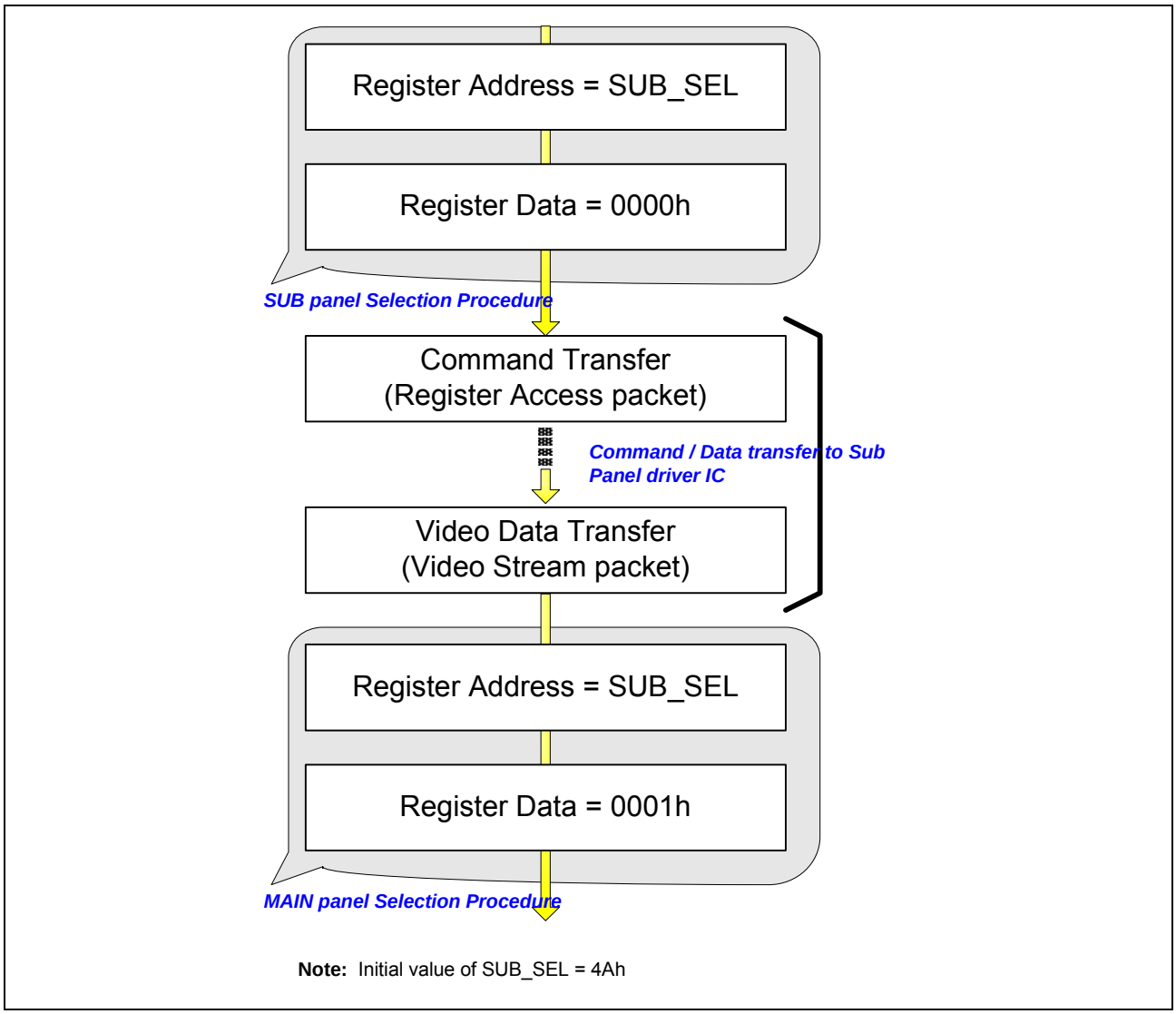


Figure 106. Main / Sub panel selection procedure

When video data is transferred to the sub panel driver IC via S6D0154, additional GRAM access command (normally 22h) is automatically generated in S6D0154.

13.15. Sub Panel Control Timing

13.15.1. TFT type sub panel timing

A. Register data transfer timing

If a sub panel is selected, and the sub panel type is TFT, register setting is executed as figure below.

Register data is transferred through S_DB[8:0] in 9/8 bit type. Refer to sub panel control (E0h index) section.

In this mode, data is transferred at twice. First transfer is MSB 8bit and second transfer is LSB 8bit.

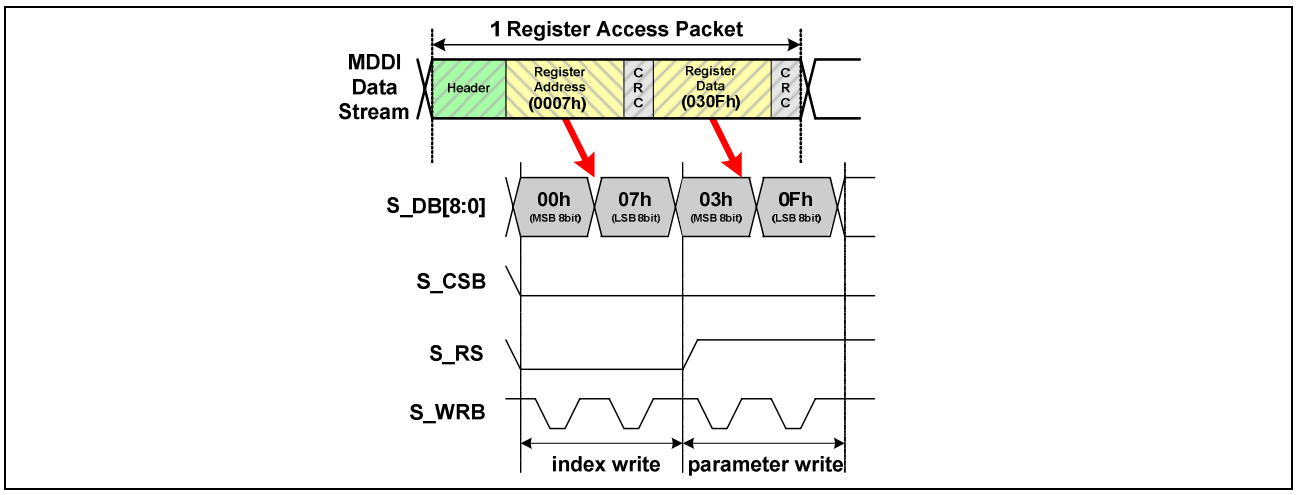


Figure 107. 80mode 9/8 bit type register access data transfer

B. Video data transfer timing

In a TFT type sub panel, STN_EN register in E0h index is “0”, and if user wants to use 68-Series interface protocol, then MPU_MODE is set to “1”. 9/8 mode is selected as setting SUB_IM register. Refer to E0h index description.

This figure shows 80-Series 9 bit Video data transfer.

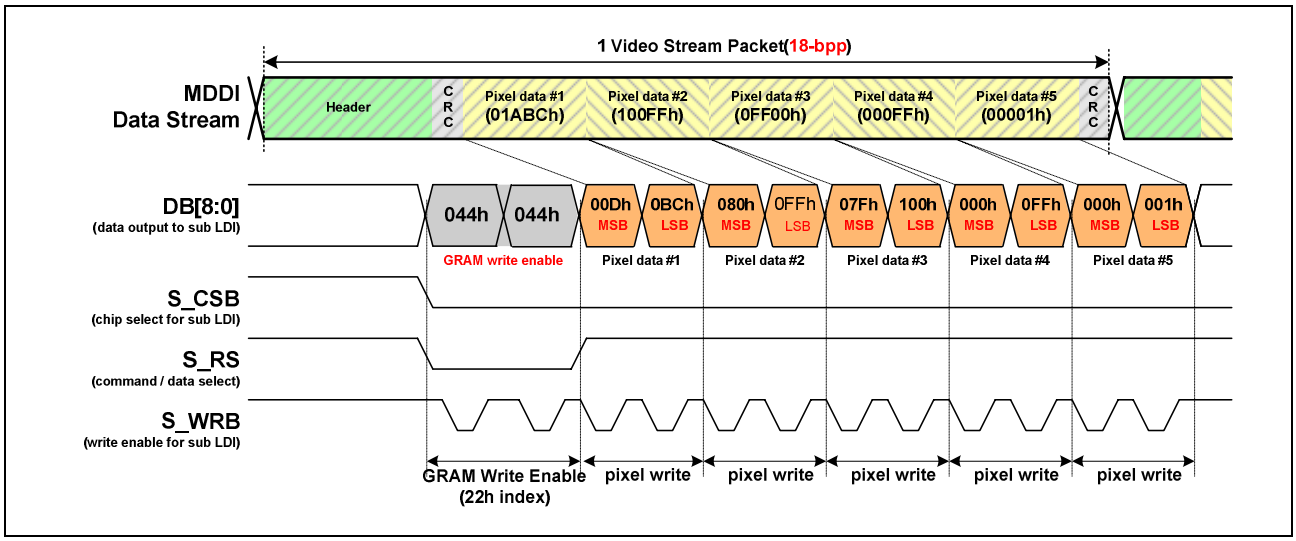


Figure 108. 80 mode 9 bit video data transfer

This figure shows 80-Series 8 bit Video data transfer.

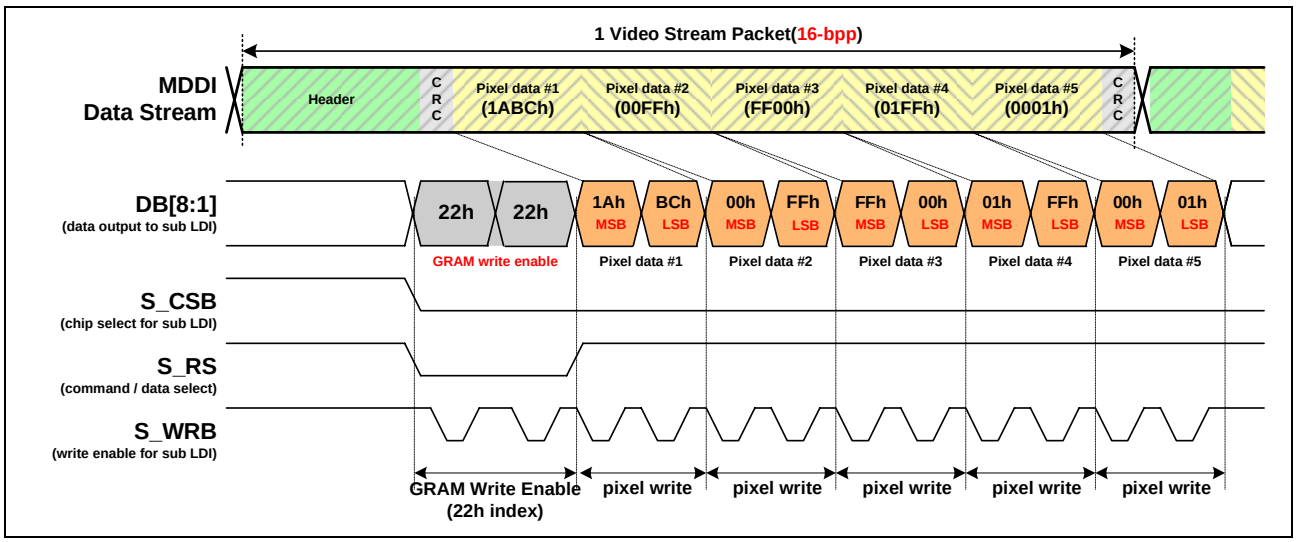


Figure 109. 80 mode 8 bit video data transfer

13.15.2. STN type sub panel timing

A. Register data transfer timing

This figure shows conventional type STN mode register data setting. Conventional type does not include parameter.

Instruction type is only 8bit. To use STN type, STN_EN is set to “1”. In STN type, S6D0154 controls S_RS pad using register address[0] in register access packet. Register address[0] is “0”, then S_RS is set to “0”, and register address[0] is “1”, S_RS is set to “1”. Refer to sub panel control(40h index) section.

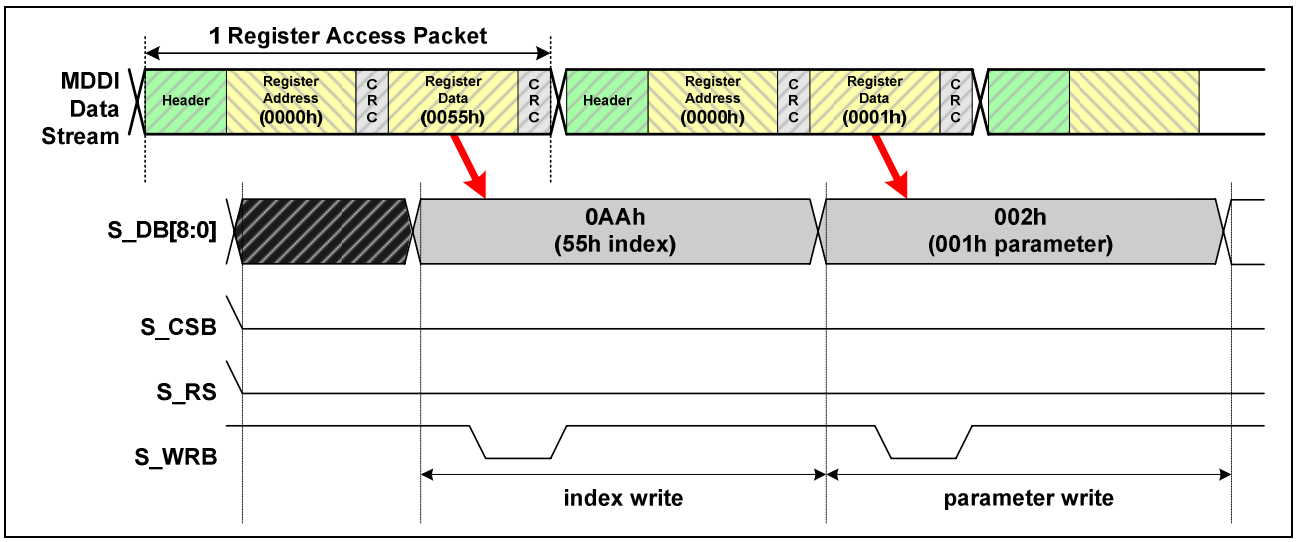


Figure 110. 80 mode STN type convetional register instruction

This type is used to include parameter. When instruction is transferred, S_RS is zero, and when parameter is transferred, S_RS is “1”. S_RS is controlled using register address[0] of register access packet.

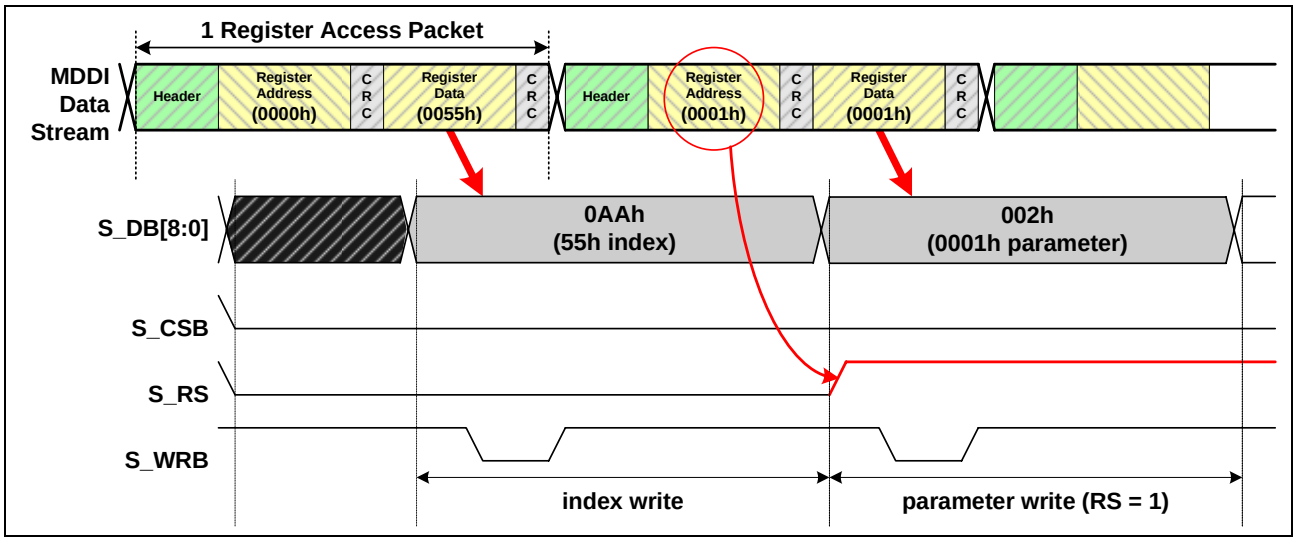


Figure 111. 80 mode STN type included parameter

B. Video data transfer timing

In STN mode, video data start register (like 22H in TFT mode) does not need generally. But some STN type needs video data start register. If those type STN DDI is used, user has to set the register index.

This figure shows STN 9 bit mode video data transfer.

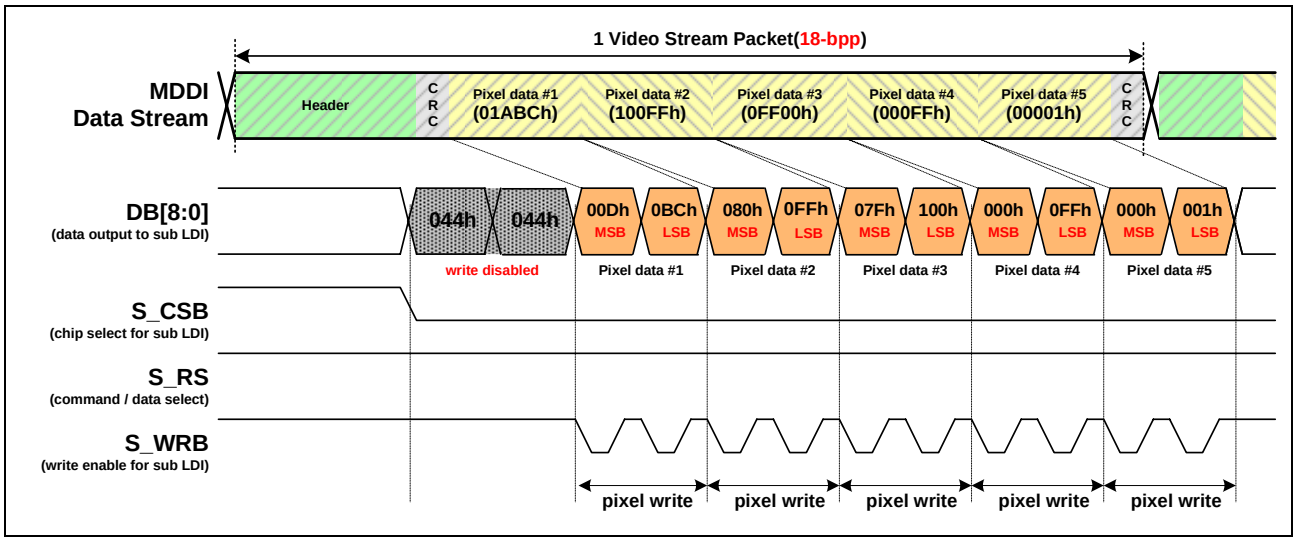


Figure 112. 80 mode STN type 9 bit video data transfer

This figure shows STN 8bit mode video data transfer. If STN video data is 16bit mode, data transfer is executed during 2 times. Fist transfer is MSB 8bits, and second is LSB 8bits.

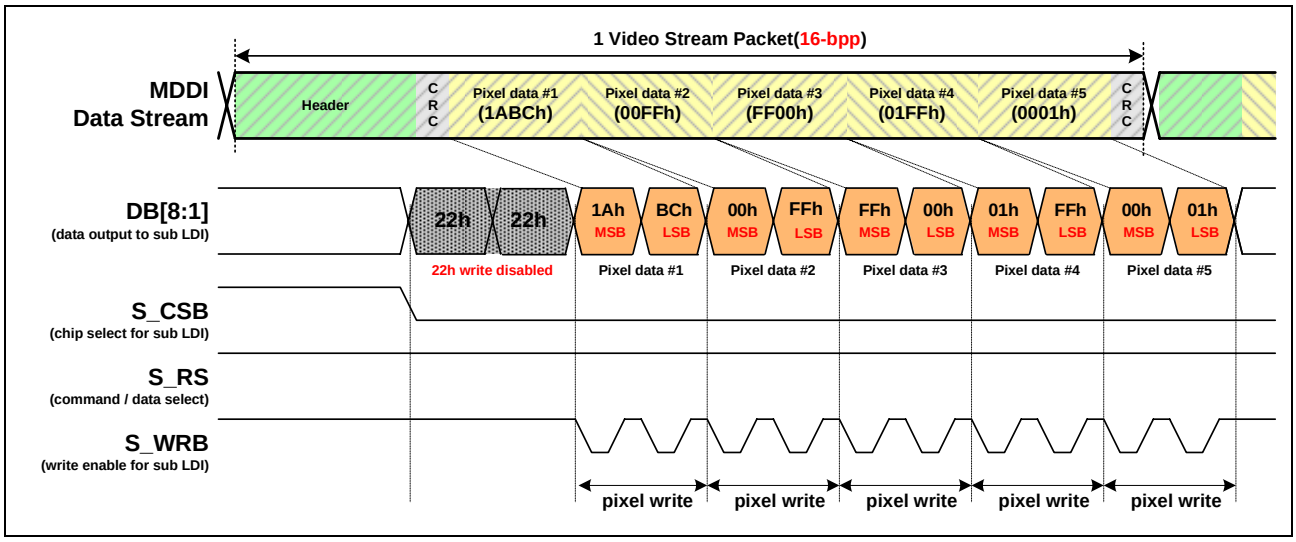


Figure 113. 80 mode STN type 8bit video data transfer

C. TFT-type Sub panel control signal speed

Sub panel timing is described below. Register writing packet and Memory writing packet have some differences.

Table 46. Sub panel signal characteristics

(k = MDDI speed (Mbps), 9bit 80mode)

Characteristic	Symbol	Specification (Register)		Specification (Video)		Unit
		Min.	Max.	Min.	Max.	
Cycle time	tCYCW80	5*(2000/k)	-	4*(2000/k)	-	ns
Pulse rise / fall time	**tR, tF	-	8	-	8	
Pulse width low	tWLW80	2*(2000/k) - 8	-	2*(2000/k) - 8	-	
Pulse width high	tWHW80	3*(2000/k) - 8	-	2*(2000/k) - 8	-	
RW, RS and CSB setup time	tAS80	3*(2000/k)	-	3*(2000/k)	-	
RW, RS and CSB hold time	tAH80	3*(2000/k)	-	3*(2000/k)	-	
Write data setup time	tWDS80	5*(2000/k)	-	5*(2000/k)	-	
Write data hold time	tWDH80	3*(2000/k)	-	3*(2000/k)	-	

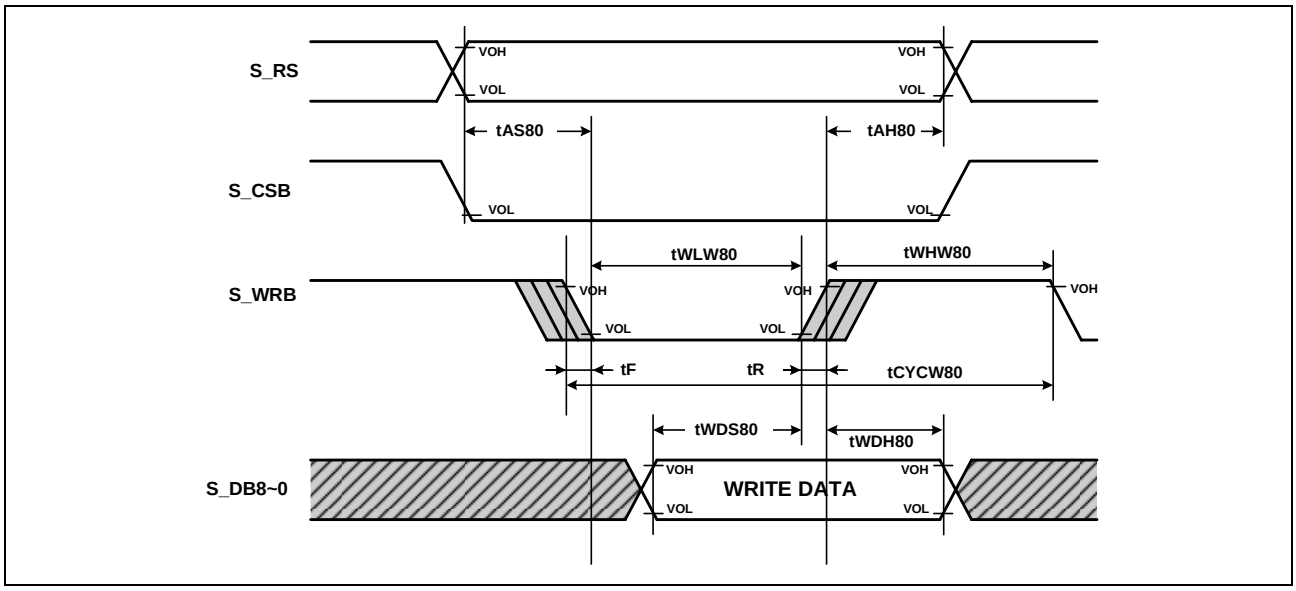


Figure 114. Sub panel signal timing(80 mode)

Note.

1. RL ≤ 200 Ω(CL ≤ 3pF)
2. PREGB = Low
3. VDD3 = 1.8 ~ 3.3V

Table 47. TFT-type Sub panel signal characteristics

(k = MDDI speed (Mbps), 9bit 68 mode)

Characteristic	Symbol	Specification (Register)		Specification (Memory)		Unit
		Min.	Max.	Min.	Max.	
Cycle time	tCYCW68	5*(2000/k)	-	4*(2000/k)	-	ns
Pulse rise / fall time	**tR, tF	-	8	-	8	
Pulse width low	tWLW68	3*(2000/k) - 8	-	2*(2000/k) - 8	-	
Pulse width high	tWHW68	2*(2000/k)-8	-	2*(2000/k) - 8	-	
RW, RS and CSB setup time	tAS68	3*(2000/k)	-	3*(2000/k)	-	
RW, RS and CSB hold time	tAH68	3*(2000/k)	-	3*(2000/k)	-	
Write data setup time	tWDS68	5*(2000/k)	-	5*(2000/k)	-	
Write data hold time	tWDH68	3*(2000/k)	-	3*(2000/k)	-	

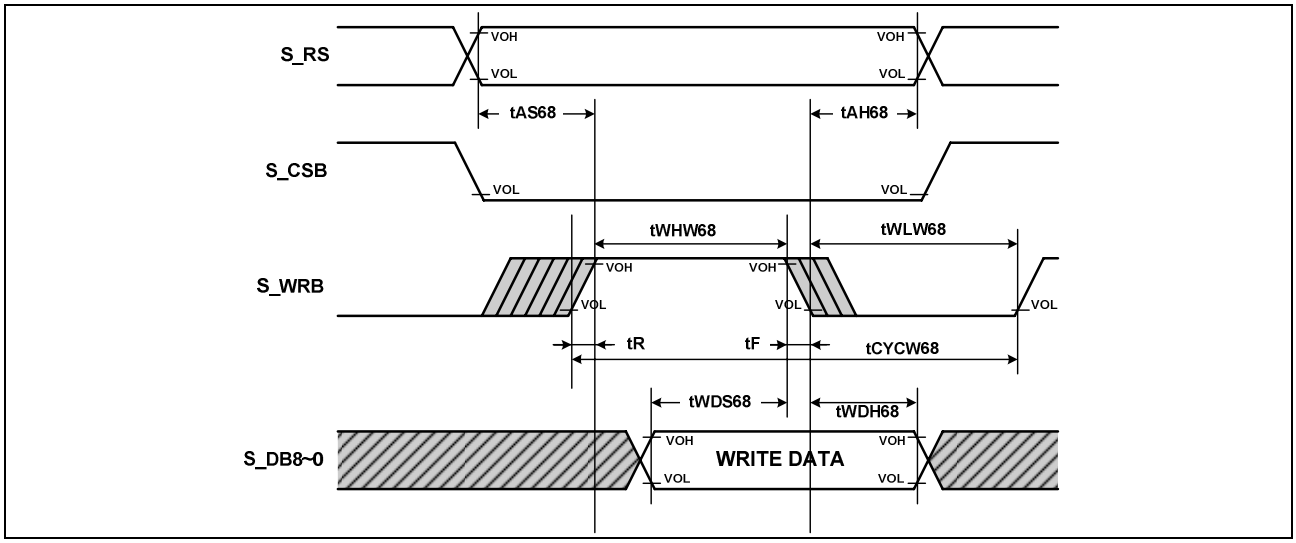


Figure 115. Sub panel signal timing(68 mode)

Note.

1. RL ≤ 200 Ω(CL ≤ 3pF)
2. PREGB = Low
3. VDD3 = 1.8 ~ 3.3V
4. TA = -40 ~ 85 ℃

13.16. Sub Panel Control Timing

A. Index/parameter write for a sub panel LDI

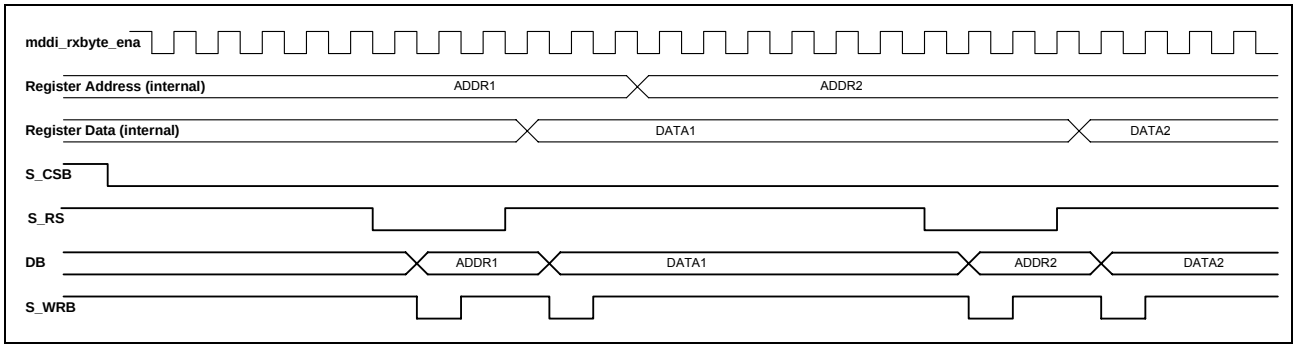


Figure 116. Index/parameter write timing diagram

B. Image data write for sub panel LDI

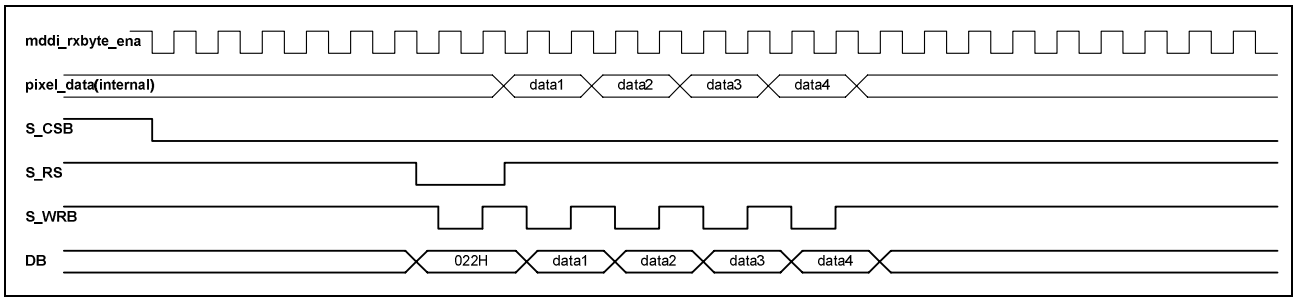


Figure 117. Image data write timing diagram

C. Change data path from sub panel to main panel

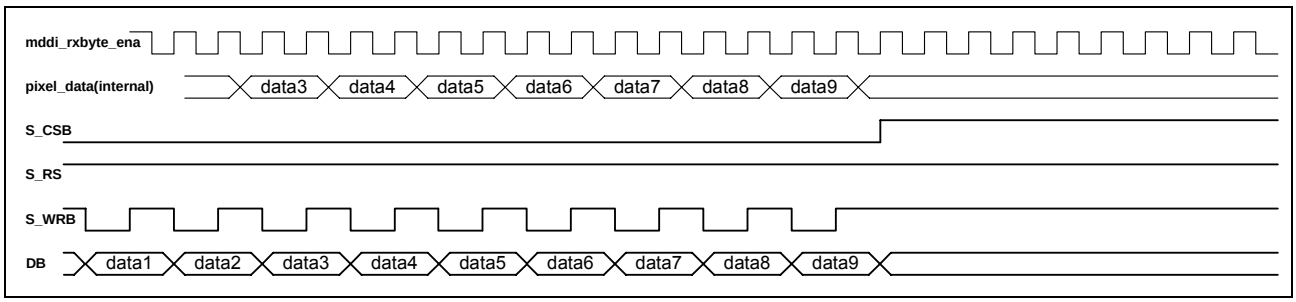


Figure 118. Change data path timing diagram

13.17. MDDI integrated system structure

MDDI support display system which incorporates GPIO and Sub panel control is shown below.
S6D0154 can display to a maximum of QVGA (240x320) resolution and sub panel resolution can be chosen according to the system requirement.

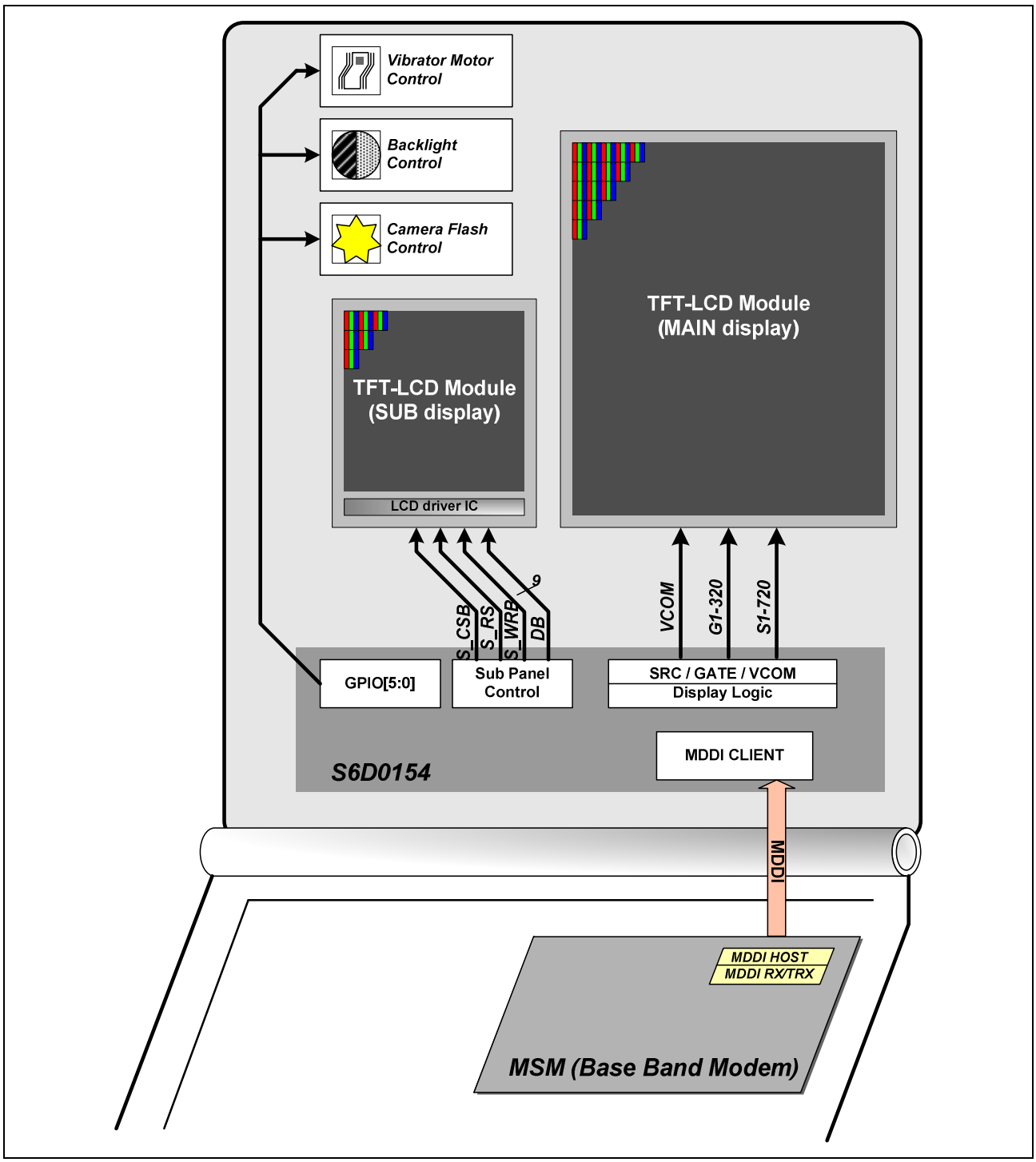


Figure 119. MDDI-integrated system structure

14. GAMMA ADJUSTMENT FUNCTION

S6D0154 provides the gamma adjustment function to display 262,144 colors simultaneously. The gamma adjustment is executed by the gradient adjustment register, the reference adjustment register, the amplitude adjustment resister and the micro-adjustment register that determine the 8 grayscale levels. Furthermore, since these registers have the positive polarities and negative polarities, adjust them to match LCD panel respectively.

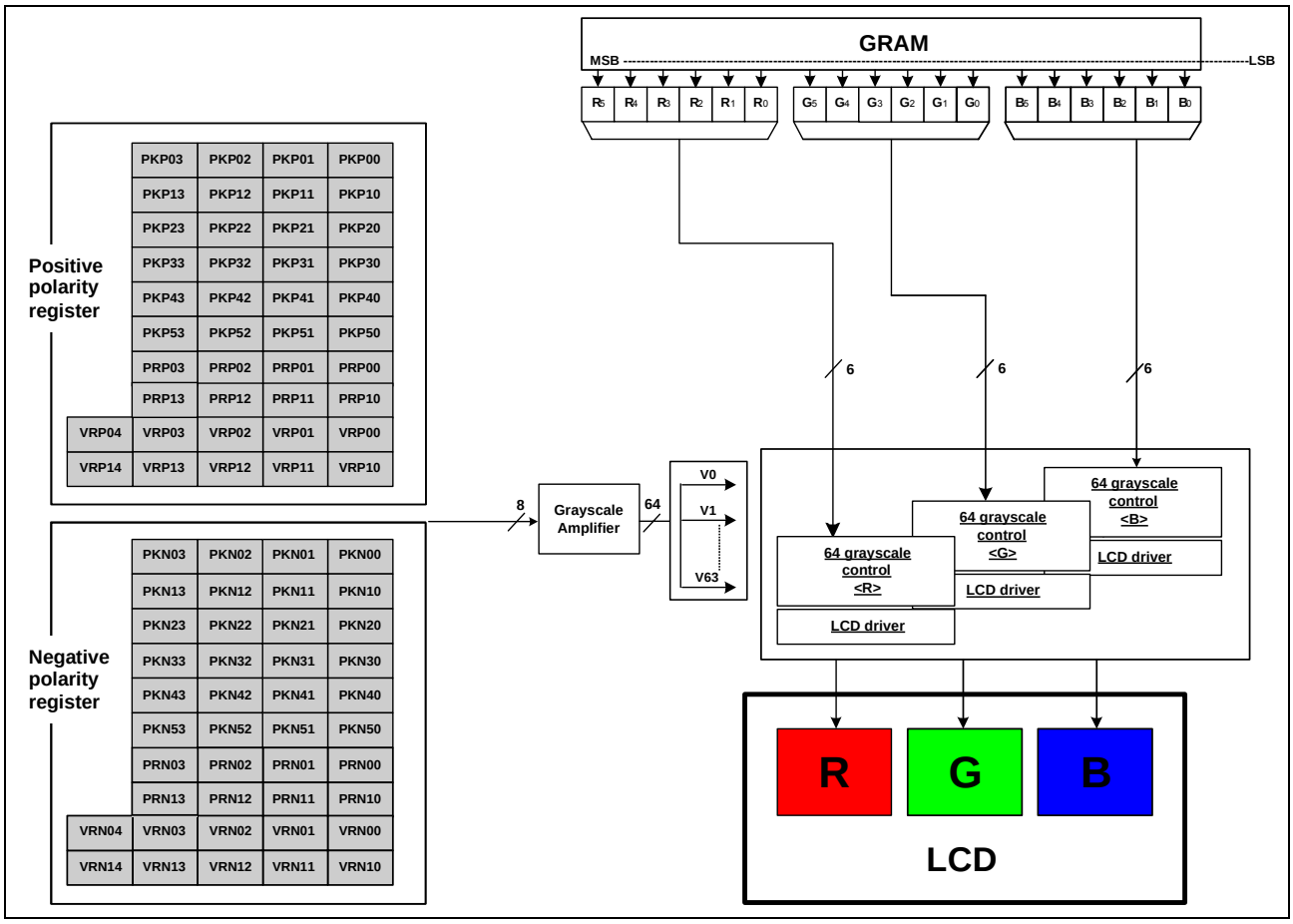


Figure 120. Grayscale Control

14.1. Structure of grayscale amplifier

The structure of grayscale amplifier is shown as below. The 8 voltage levels (VIN0-VIN7) between GVDD and VGS are determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment resister and the micro-adjustment register. Each level is split into 8 levels again by the internal ladder resistor network. As a result, grayscale amplifier generates 64 voltage levels ranging from V0 to V63.

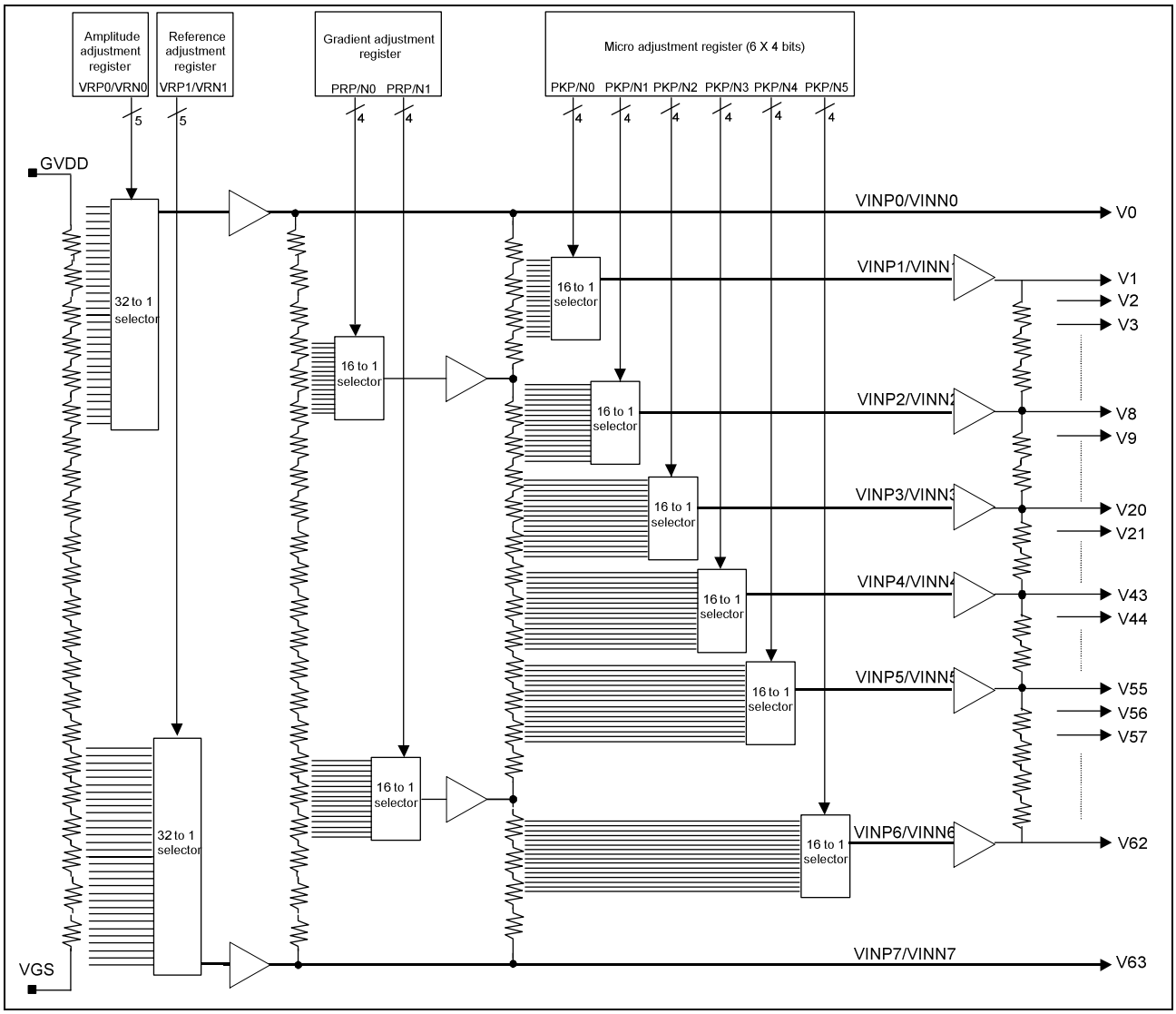


Figure 121. Structure of Grayscale Amplifier

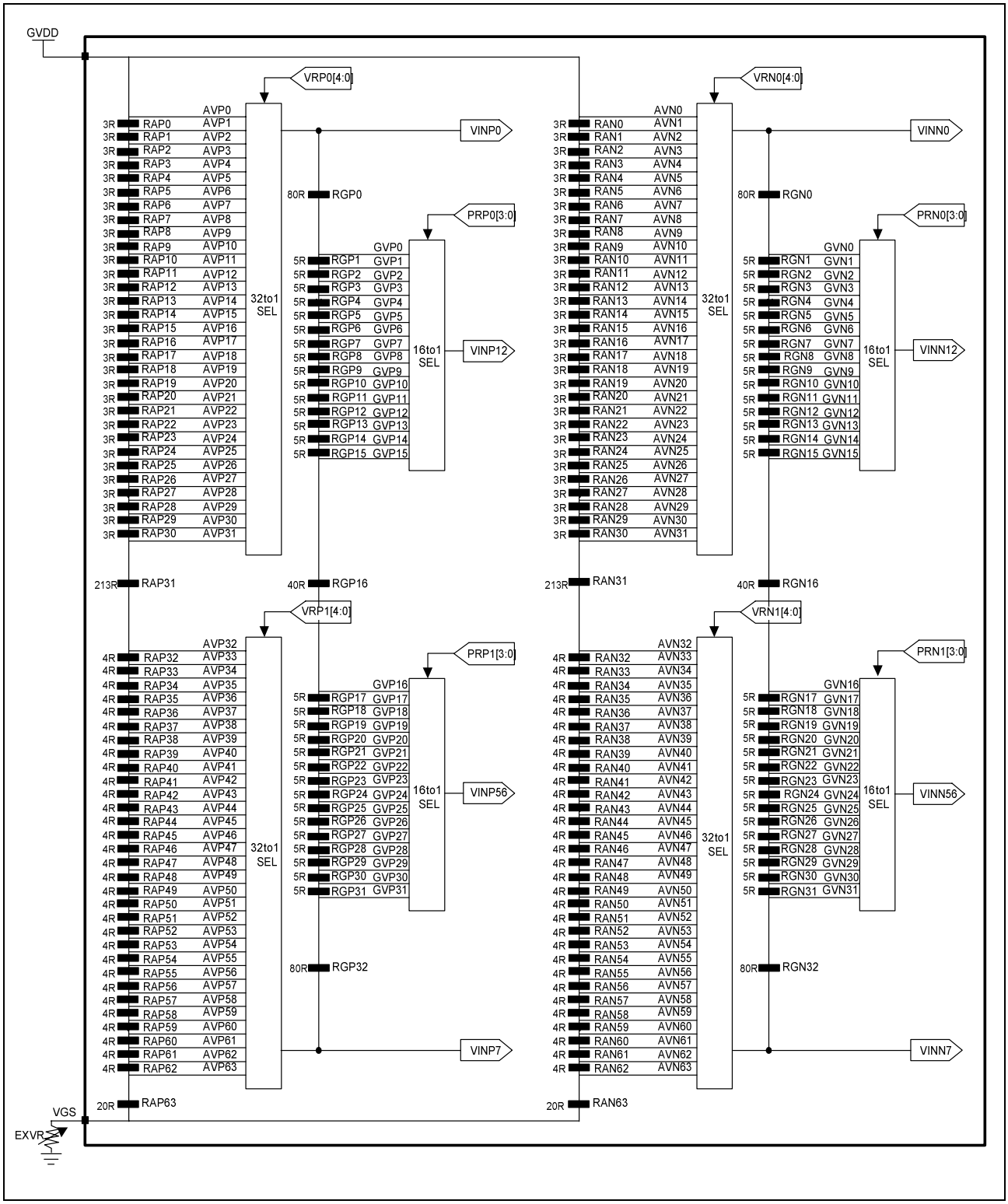


Figure 122. Structure of Resistor Ladder Network 1

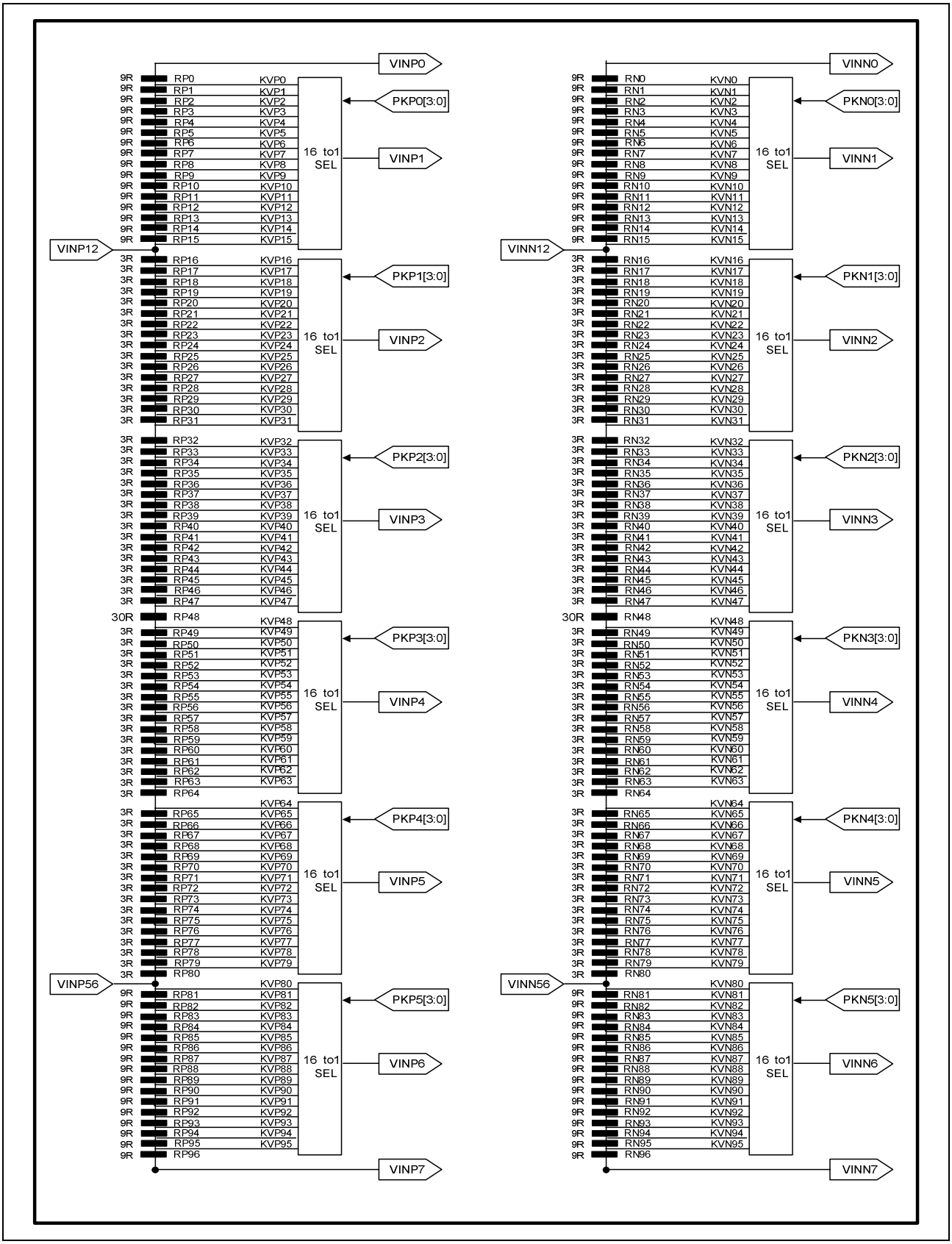


Figure 123. Structure of Resistor Ladder Network 2

14.2. gamma adjustment register

This block has registers to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. These registers can independently set up to positive/negative polarities and there are 4 types of register groups to adjust gradient and amplitude on number of the grayscale, characteristics of the grayscale voltage. The following figure indicates the operation of each adjustment register.

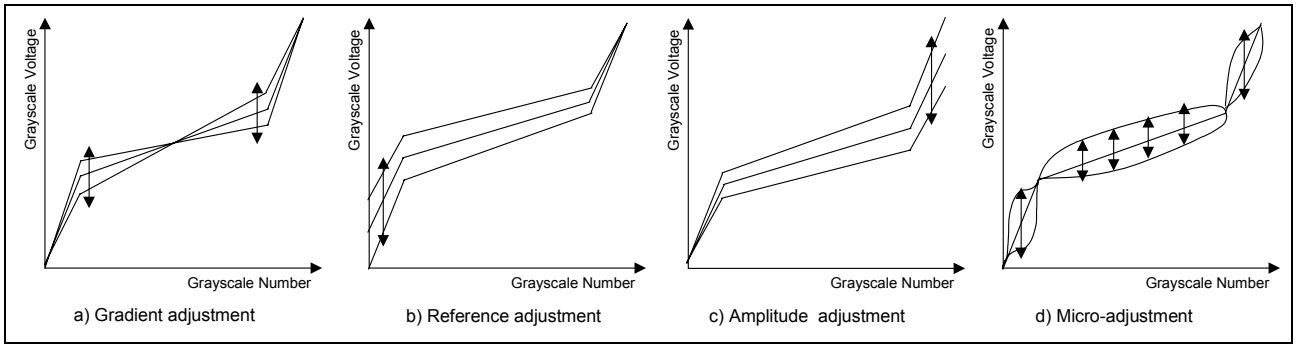


Figure 124. The Operation of Adjusting Register

Gradient adjusting register

The gradient adjustment register is to adjust the gradient in the middle of the grayscale characteristics for the voltage without changing the dynamic range. To accomplish the adjustment, it controls the VINP12/VINN12 and VINP56/VINN56 voltage level by the 16 to 1 selector towards the 16-leveled reference voltage generated from the resistor ladder between VINP0/VINN0 and VINP7/VINN7. Also, there is an independent register on the positive/negative polarities in order for corresponding to asymmetry drive.

Reference adjusting register

The Reference adjustment register is to adjust the reference of the grayscale voltage. To accomplish the adjustment, it controls the VINP7/VINN7 voltage level by 32 to 1 selector towards the 32-leveled reference voltage generated from the resistor ladder between GVDD and VGS.

Amplitude adjusting register

The Amplitude adjustment register is to adjust the amplitude of the grayscale voltage. To accomplish the adjustment, it controls the VINP0/VINN0 voltage level by 32 to 1 selector towards the 32-leveled reference voltage generated from the resistor ladder between GVDD and VGS.

Micro-adjusting register

The Micro adjustment register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls the each reference voltage level by the 16 to 1 selector towards the 16-leveled reference voltage generated from the resistor ladder. Also, there is an independent register on the positive/negative polarities as well as other adjustment registers.

Table 48. Gamma Adjustment Register

Register	Positive polarity	Negative polarity	Set-up contents
Gradient adjustment	PRP0[3:0]	PRN0[3:0]	The voltage of VINP12/VINN12 is selected by the 16 to 1 selector
	PRP1[3:0]	PRN1[3:0]	The voltage of VINP56/VINN56 is selected by the 16 to 1 selector
Reference adjustment	VRP1[4:0]	VRN1[4:0]	The voltage of VINP7/VINN7 is selected by the 32 to 1 selector
Amplitude adjustment	VRP0[4:0]	VRN0[4:0]	The voltage of VINP0/VINN0 is selected by the 32 to 1 selector
Micro adjustment	PKP0[3:0]	PKN0[3:0]	The voltage of grayscale number 1 is selected by the 16 to 1 selector
	PKP1[3:0]	PKN1[3:0]	The voltage of grayscale number 8 is selected by the 16 to 1 selector
	PKP2[3:0]	PKN2[3:0]	The voltage of grayscale number 20 is selected by the 16 to 1 selector
	PKP3[3:0]	PKN3[3:0]	The voltage of grayscale number 43 is selected by the 16 to 1 selector
	PKP4[3:0]	PKN4[3:0]	The voltage of grayscale number 55 is selected by the 16 to 1 selector
	PKP5[3:0]	PKN5[3:0]	The voltage of grayscale number 62 is selected by the 16 to 1 selector

14.3. Resistor ladder network / selector

This block outputs the reference voltage of the grayscale voltage. There are four ladder resistors including the 8 to 1 selector selecting voltage generated by the ladder resistance voltage. Also, there are pins that connect to the external volume resistor. In addition, it allows compensating the dispersion of length between one panel and another.

Resistor ladder network 1 / selector

There are 4 adjustments that are for the gradient adjustment (VRHP(N) / VRLP(N)) and for the reference / amplitude adjustment (VRP(N)1 / VRP(N)0). The voltage level is set by the gradient adjustment register and the reference / amplitude adjustment registers as below.

Table 49. Amplitude Adjustment

Register value VRP(N)0 [4:0]	Selected voltage VINP(N)0	Formula of VINP(N)0
00000	AVP(N)0	(450R/450R) * (GVDD-VGS) + VGS
00001	AVP(N)1	(447R/450R) * (GVDD-VGS) + VGS
00010	AVP(N)2	(444R/450R) * (GVDD-VGS) + VGS
00011	AVP(N)3	(441R/450R) * (GVDD-VGS) + VGS
00100	AVP(N)4	(438R/450R) * (GVDD-VGS) + VGS
00101	AVP(N)5	(435R/450R) * (GVDD-VGS) + VGS
00110	AVP(N)6	(432R/450R) * (GVDD-VGS) + VGS
00111	AVP(N)7	(429R/450R) * (GVDD-VGS) + VGS
01000	AVP(N)8	(426R/450R) * (GVDD-VGS) + VGS
01001	AVP(N)9	(423R/450R) * (GVDD-VGS) + VGS
01010	AVP(N)10	(420R/450R) * (GVDD-VGS) + VGS
01011	AVP(N)11	(417R/450R) * (GVDD-VGS) + VGS
01100	AVP(N)12	(414R/450R) * (GVDD-VGS) + VGS
01101	AVP(N)13	(411R/450R) * (GVDD-VGS) + VGS
01110	AVP(N)14	(408R/450R) * (GVDD-VGS) + VGS
01111	AVP(N)15	(405R/450R) * (GVDD-VGS) + VGS
10000	AVP(N)16	(402R/450R) * (GVDD-VGS) + VGS
10001	AVP(N)17	(399R/450R) * (GVDD-VGS) + VGS
10010	AVP(N)18	(396R/450R) * (GVDD-VGS) + VGS
10011	AVP(N)19	(393R/450R) * (GVDD-VGS) + VGS
10100	AVP(N)20	(390R/450R) * (GVDD-VGS) + VGS
10101	AVP(N)21	(387R/450R) * (GVDD-VGS) + VGS
10110	AVP(N)22	(384R/450R) * (GVDD-VGS) + VGS
10111	AVP(N)23	(381R/450R) * (GVDD-VGS) + VGS
11000	AVP(N)24	(378R/450R) * (GVDD-VGS) + VGS
11001	AVP(N)25	(375R/450R) * (GVDD-VGS) + VGS
11010	AVP(N)26	(372R/450R) * (GVDD-VGS) + VGS
11011	AVP(N)27	(369R/450R) * (GVDD-VGS) + VGS
11100	AVP(N)28	(366R/450R) * (GVDD-VGS) + VGS
11101	AVP(N)29	(363R/450R) * (GVDD-VGS) + VGS
11110	AVP(N)30	(360R/450R) * (GVDD-VGS) + VGS
11111	AVP(N)31	(357R/450R) * (GVDD-VGS) + VGS

Table 50. Reference Adjustment

Register value VRP(N)1 [4:0]	Selected voltage VINP(N)7	Formula of VINP(N)7
00000	AVP(N)63	(20R/450R) * (GVDD-VGS) + VGS
00001	AVP(N)62	(24R/450R) * (GVDD-VGS) + VGS
00010	AVP(N)61	(28R/450R) * (GVDD-VGS) + VGS
00011	AVP(N)60	(32R/450R) * (GVDD-VGS) + VGS
00100	AVP(N)59	(36R/450R) * (GVDD-VGS) + VGS
00101	AVP(N)58	(40R/450R) * (GVDD-VGS) + VGS
00110	AVP(N)57	(44R/450R) * (GVDD-VGS) + VGS
00111	AVP(N)56	(48R/450R) * (GVDD-VGS) + VGS
01000	AVP(N)55	(52R/450R) * (GVDD-VGS) + VGS
01001	AVP(N)54	(56R/450R) * (GVDD-VGS) + VGS
01010	AVP(N)53	(60R/450R) * (GVDD-VGS) + VGS
01011	AVP(N)52	(64R/450R) * (GVDD-VGS) + VGS
01100	AVP(N)51	(68R/450R) * (GVDD-VGS) + VGS
01101	AVP(N)50	(72R/450R) * (GVDD-VGS) + VGS
01110	AVP(N)49	(76R/450R) * (GVDD-VGS) + VGS
01111	AVP(N)48	(80R/450R) * (GVDD-VGS) + VGS
10000	AVP(N)47	(84R/450R) * (GVDD-VGS) + VGS
10001	AVP(N)46	(88R/450R) * (GVDD-VGS) + VGS
10010	AVP(N)45	(92R/450R) * (GVDD-VGS) + VGS
10011	AVP(N)44	(96R/450R) * (GVDD-VGS) + VGS
10100	AVP(N)43	(100R/450R) * (GVDD-VGS) + VGS
10101	AVP(N)42	(104R/450R) * (GVDD-VGS) + VGS
10110	AVP(N)41	(108R/450R) * (GVDD-VGS) + VGS
10111	AVP(N)40	(112R/450R) * (GVDD-VGS) + VGS
11000	AVP(N)39	(116R/450R) * (GVDD-VGS) + VGS
11001	AVP(N)38	(120R/450R) * (GVDD-VGS) + VGS
11010	AVP(N)37	(124R/450R) * (GVDD-VGS) + VGS
11011	AVP(N)36	(128R/450R) * (GVDD-VGS) + VGS
11100	AVP(N)35	(132R/450R) * (GVDD-VGS) + VGS
11101	AVP(N)34	(136R/450R) * (GVDD-VGS) + VGS
11110	AVP(N)33	(140R/450R) * (GVDD-VGS) + VGS
11111	AVP(N)32	(144R/450R) * (GVDD-VGS) + VGS

Table 51. Gradient Adjustment (1)

Register value PRP(N)0 [3:0]	Selected voltage VINP(N)12	Formula of VINP(N)12
0000	GVP(N)0	(270R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
0001	GVP(N)1	(265R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
0010	GVP(N)2	(260R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
0011	GVP(N)3	(255R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
0100	GVP(N)4	(250R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
0101	GVP(N)5	(245R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
0110	GVP(N)6	(240R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
0111	GVP(N)7	(235R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1000	GVP(N)8	(230R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1001	GVP(N)9	(225R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1010	GVP(N)10	(220R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1011	GVP(N)11	(215R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1100	GVP(N)12	(210R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1101	GVP(N)13	(205R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1110	GVP(N)14	(200R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1111	GVP(N)15	(195R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7

Table 52. Gradient Adjustment (2)

Register value PRP(N)1 [3:0]	Selected voltage VINP(N)56	Formula of VINP(N)56
0000	GVP(N)31	(80R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
0001	GVP(N)30	(85R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
0010	GVP(N)29	(90R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
0011	GVP(N)28	(95R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
0100	GVP(N)27	(100R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
0101	GVP(N)26	(105R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
0110	GVP(N)25	(110R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
0111	GVP(N)24	(115R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1000	GVP(N)23	(120R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1001	GVP(N)22	(125R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1010	GVP(N)21	(130R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1011	GVP(N)20	(135R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1100	GVP(N)19	(140R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1101	GVP(N)18	(145R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1110	GVP(N)17	(150R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7
1111	GVP(N)16	(155R/350R) * (VINP(N)0-VINP(N)7) + VINP(N)7

Resistor ladder network 2 / selector

In the 16-to-1 selector, the voltage level must be selected by the given ladder resistance and the micro-adjustment register and output the six types of the reference voltage, VIN1 to VIN6.

Following figure explains the relationship between the micro-adjustment register and the selected voltage.

Table 53. Relationship between Micro-adjustment Register and Selected Voltage

Register value PKP(N) [3:0]	Selected voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
0000	KVP(N)0	KVP(N)16	KVP(N)32	KVP(N)63	KVP(N)79	KVP(N)95
0001	KVP(N)1	KVP(N)17	KVP(N)33	KVP(N)62	KVP(N)78	KVP(N)94
0010	KVP(N)2	KVP(N)18	KVP(N)34	KVP(N)61	KVP(N)77	KVP(N)93
0011	KVP(N)3	KVP(N)19	KVP(N)35	KVP(N)60	KVP(N)76	KVP(N)92
0100	KVP(N)4	KVP(N)20	KVP(N)36	KVP(N)59	KVP(N)75	KVP(N)91
0101	KVP(N)5	KVP(N)21	KVP(N)37	KVP(N)58	KVP(N)74	KVP(N)90
0110	KVP(N)6	KVP(N)22	KVP(N)38	KVP(N)57	KVP(N)73	KVP(N)89
0111	KVP(N)7	KVP(N)23	KVP(N)39	KVP(N)56	KVP(N)72	KVP(N)88
1000	KVP(N)8	KVP(N)24	KVP(N)40	KVP(N)55	KVP(N)71	KVP(N)87
1001	KVP(N)9	KVP(N)25	KVP(N)41	KVP(N)54	KVP(N)70	KVP(N)86
1010	KVP(N)10	KVP(N)26	KVP(N)42	KVP(N)53	KVP(N)69	KVP(N)85
1011	KVP(N)11	KVP(N)27	KVP(N)43	KVP(N)52	KVP(N)68	KVP(N)84
1100	KVP(N)12	KVP(N)28	KVP(N)44	KVP(N)51	KVP(N)67	KVP(N)83
1101	KVP(N)13	KVP(N)29	KVP(N)45	KVP(N)50	KVP(N)66	KVP(N)82
1110	KVP(N)14	KVP(N)30	KVP(N)46	KVP(N)49	KVP(N)65	KVP(N)81
1111	KVP(N)15	KVP(N)31	KVP(N)47	KVP(N)48	KVP(N)64	KVP(N)80

Note. The grayscale levels are determined by the following formulas listed in the next pages.

Table 54. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1

Pins	Formula	Micro-adjusting register value	Reference voltage
KVP0	(45R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0000”	VINP1
KVP1	(42R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0001”	
KVP2	(39R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0010”	
KVP3	(36R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0011”	
KVP4	(33R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0100”	
KVP5	(30R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0101”	
KVP6	(27R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0110”	
KVP7	(24R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0111”	
KVP8	(21R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1000”	
KVP9	(18R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1001”	
KVP10	(15R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1010”	
KVP11	(12R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1011”	
KVP12	(9R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1100”	
KVP13	(6R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1101”	
KVP14	(3R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1110”	
KVP15	VINP12	PKP0[3:0] = “1111”	
KVP16	(219R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0000”	VINP2
KVP17	(216R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0001”	
KVP18	(213R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0010”	
KVP19	(210R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0011”	
KVP20	(207R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0100”	
KVP21	(204R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0101”	
KVP22	(201R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0110”	
KVP23	(198R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0111”	
KVP24	(195R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1000”	
KVP25	(192R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1001”	
KVP26	(189R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1010”	
KVP27	(186R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1011”	
KVP28	(183R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1100”	
KVP29	(180R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1101”	
KVP30	(177R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1110”	
KVP31	(174R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1111”	
KVP32	(171R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0000”	VINP3
KVP33	(168R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0001”	
KVP34	(165R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0010”	
KVP35	(162R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0011”	
KVP36	(159R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0100”	
KVP37	(156R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0101”	
KVP38	(153R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0110”	
KVP39	(150R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0111”	
KVP40	(147R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1000”	
KVP41	(144R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1001”	
KVP42	(141R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1010”	
KVP43	(138R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1011”	
KVP44	(135R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1100”	
KVP45	(132R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1101”	
KVP46	(129R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1110”	
KVP47	(126R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1111”	

Pins	Formula	Micro-adjusting register value	Reference voltage
KVP48	(96R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “1111”	VINP4
KVP49	(93R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “1110”	
KVP50	(90R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “1101”	
KVP51	(87R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “1100”	
KVP52	(84R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “1011”	
KVP53	(81R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “1010”	
KVP54	(78R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “1001”	
KVP55	(75R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “1000”	
KVP56	(72R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “0111”	
KVP57	(69R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “0110”	
KVP58	(66R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “0101”	
KVP59	(63R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “0100”	
KVP60	(60R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “0011”	
KVP61	(57R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “0010”	
KVP62	(54R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “0001”	
KVP63	(51R/222R) * (VINP12-VINP56) + VINP56	PKP3[3:0] = “0000”	
KVP64	(48R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “1111”	VINP5
KVP65	(45R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “1110”	
KVP66	(42R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “1101”	
KVP67	(39R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “1100”	
KVP68	(36R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “1011”	
KVP69	(33R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “1010”	
KVP70	(30R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “1001”	
KVP71	(27R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “1000”	
KVP72	(24R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “0111”	
KVP73	(21R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “0110”	
KVP74	(18R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “0101”	
KVP75	(15R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “0100”	
KVP76	(12R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “0011”	
KVP77	(9R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “0010”	
KVP78	(6R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “0001”	
KVP79	(3R/222R) * (VINP12-VINP56) + VINP56	PKP4[3:0] = “0000”	
KVP80	VINP56	PKP5[3:0] = “1111”	VINP6
KVP81	(45R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “1110”	
KVP82	(42R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “1101”	
KVP83	(39R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “1100”	
KVP84	(36R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “1011”	
KVP85	(33R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “1010”	
KVP86	(30R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “1001”	
KVP87	(27R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “1000”	
KVP88	(24R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “0111”	
KVP89	(21R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “0110”	
KVP90	(18R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “0101”	
KVP91	(15R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “0100”	
KVP92	(12R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “0011”	
KVP93	(9R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “0010”	
KVP94	(6R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “0001”	
KVP95	(3R/48R) * (VINP56 – VINP7) + VINP7	PKP5[3:0] = “0000”	

Table 55. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	V20-(V20-V43)*(12/23)
V1	VINP1	V33	V20-(V20-V43)*(13/23)
V2	V1-(V1-V8)*(28/96)	V34	V20-(V20-V43)*(14/23)
V3	V1-(V1-V8)*(42/96)	V35	V20-(V20-V43)*(15/23)
V4	V1-(V1-V8)*(60/96)	V36	V20-(V20-V43)*(16/23)
V5	V1-(V1-V8)*(69/96)	V37	V20-(V20-V43)*(17/23)
V6	V1-(V1-V8)*(78/96)	V38	V20-(V20-V43)*(18/23)
V7	V1-(V1-V8)*(87/96)	V39	V20-(V20-V43)*(19/23)
V8	VINP2	V40	V20-(V20-V43)*(20/23)
V9	V8-(V8-V20)*(2/24)	V41	V20-(V20-V43)*(21/23)
V10	V8-(V8-V20)*(4/24)	V42	V20-(V20-V43)*(22/23)
V11	V8-(V8-V20)*(6/24)	V43	VINP4
V12	V8-(V8-V20)*(8/24)	V44	V43-(V43-V55)*(2/24)
V13	V8-(V8-V20)*(10/24)	V45	V43-(V43-V55)*(4/24)
V14	V8-(V8-V20)*(12/24)	V46	V43-(V43-V55)*(6/24)
V15	V8-(V8-V20)*(14/24)	V47	V43-(V43-V55)*(8/24)
V16	V8-(V8-V20)*(16/24)	V48	V43-(V43-V55)*(10/24)
V17	V8-(V8-V20)*(18/24)	V49	V43-(V43-V55)*(12/24)
V18	V8-(V8-V20)*(20/24)	V50	V43-(V43-V55)*(14/24)
V19	V8-(V8-V20)*(22/24)	V51	V43-(V43-V55)*(16/24)
V20	VINP3	V52	V43-(V43-V55)*(18/24)
V21	V20-(V20-V43)*(1/23)	V53	V43-(V43-V55)*(20/24)
V22	V20-(V20-V43)*(2/23)	V54	V43-(V43-V55)*(22/24)
V23	V20-(V20-V43)*(3/23)	V55	VINP5
V24	V20-(V20-V43)*(4/23)	V56	V55-(V55-V62)*(9/96)
V25	V20-(V20-V43)*(5/23)	V57	V55-(V55-V62)*(18/96)
V26	V20-(V20-V43)*(6/23)	V58	V55-(V55-V62)*(27/96)
V27	V20-(V20-V43)*(7/23)	V59	V55-(V55-V62)*(36/96)
V28	V20-(V20-V43)*(8/23)	V60	V55-(V55-V62)*(54/96)
V29	V20-(V20-V43)*(9/23)	V61	V55-(V55-V62)*(68/96)
V30	V20-(V20-V43)*(10/23)	V62	VINP6
V31	V20-(V20-V43)*(11/23)	V63	VINP7

Table 56. Formulas for Calculating Gamma Adjusting Voltage (Negative Polarity) 1

Pins	Formula	Micro-adjusting register value	Reference voltage
KVN0	(45R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0000”	VINN1
KVN1	(42R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0001”	
KVN2	(39R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0010”	
KVN3	(36R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0011”	
KVN4	(33R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0100”	
KVN5	(30R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0101”	
KVN6	(27R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0110”	
KVN7	(24R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0111”	
KVN8	(21R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1000”	
KVN9	(18R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1001”	
KVN10	(15R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1010”	
KVN11	(12R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1011”	
KVN12	(9R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1100”	
KVN13	(6R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1101”	
KVN14	(3R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1110”	
KVN15	VINN12	PKN0[3:0] = “1111”	
KVN16	(219R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0000”	VINN2
KVN17	(216R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0001”	
KVN18	(213R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0010”	
KVN19	(210R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0011”	
KVN20	(207R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0100”	
KVN21	(204R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0101”	
KVN22	(201R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0110”	
KVN23	(198R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0111”	
KVN24	(195R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1000”	
KVN25	(192R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1001”	
KVN26	(189R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1010”	
KVN27	(186R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1011”	
KVN28	(183R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1100”	
KVN29	(180R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1101”	
KVN30	(177R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1110”	
KVN31	(174R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1111”	
KVN32	(171R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0000”	VINN3
KVN33	(168R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0001”	
KVN34	(165R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0010”	
KVN35	(162R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0011”	
KVN36	(159R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0100”	
KVN37	(156R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0101”	
KVN38	(153R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0110”	
KVN39	(150R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0111”	
KVN40	(147R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1000”	
KVN41	(144R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1001”	
KVN42	(141R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1010”	
KVN43	(138R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1011”	
KVN44	(135R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1100”	
KVN45	(132R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1101”	
KVN46	(129R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1110”	
KVN47	(126R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1111”	

Pins	Formula	Micro-adjusting register value	Reference voltage
KVN48	(96R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “1111”	VINN4
KVN49	(93R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “1110”	
KVN50	(90R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “1101”	
KVN51	(87R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “1100”	
KVN52	(84R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “1011”	
KVN53	(81R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “1010”	
KVN54	(78R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “1001”	
KVN55	(75R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “1000”	
KVN56	(72R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “0111”	
KVN57	(69R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “0110”	
KVN58	(66R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “0101”	
KVN59	(63R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “0100”	
KVN60	(60R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “0011”	
KVN61	(57R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “0010”	
KVN62	(54R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “0001”	
KVN63	(51R/222R) * (VINN12-VINN56) + VINN56	PKN3[3:0] = “0000”	
KVN64	(48R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “1111”	VINN5
KVN65	(45R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “1110”	
KVN66	(42R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “1101”	
KVN67	(39R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “1100”	
KVN68	(36R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “1011”	
KVN69	(33R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “1010”	
KVN70	(30R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “1001”	
KVN71	(27R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “1000”	
KVN72	(24R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “0111”	
KVN73	(21R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “0110”	
KVN74	(18R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “0101”	
KVN75	(15R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “0100”	
KVN76	(12R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “0011”	
KVN77	(9R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “0010”	
KVN78	(6R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “0001”	
KVN79	(3R/222R) * (VINN12-VINN56) + VINN56	PKN4[3:0] = “0000”	
KVN80	VINN56	PKN5[3:0] = “1111”	VINN6
KVN81	(45R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “1110”	
KVN82	(42R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “1101”	
KVN83	(39R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “1100”	
KVN84	(36R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “1011”	
KVN85	(33R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “1010”	
KVN86	(30R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “1001”	
KVN87	(27R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “1000”	
KVN88	(24R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “0111”	
KVN89	(21R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “0110”	
KVN90	(18R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “0101”	
KVN91	(15R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “0100”	
KVN92	(12R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “0011”	
KVN93	(9R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “0010”	
KVN94	(6R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “0001”	
KVN95	(3R/48R) * (VINN56 – VINN7) + VINN7	PKN5[3:0] = “0000”	

Table 57. Formulas for Calculating Gamma Adjusting Voltage (Negative Polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINN0	V32	V20-(V20-V43)*(12/23)
V1	VINN1	V33	V20-(V20-V43)*(13/23)
V2	V1-(V1-V8)*(28/96)	V34	V20-(V20-V43)*(14/23)
V3	V1-(V1-V8)*(42/96)	V35	V20-(V20-V43)*(15/23)
V4	V1-(V1-V8)*(60/96)	V36	V20-(V20-V43)*(16/23)
V5	V1-(V1-V8)*(69/96)	V37	V20-(V20-V43)*(17/23)
V6	V1-(V1-V8)*(78/96)	V38	V20-(V20-V43)*(18/23)
V7	V1-(V1-V8)*(87/96)	V39	V20-(V20-V43)*(19/23)
V8	VINN2	V40	V20-(V20-V43)*(20/23)
V9	V8-(V8-V20)*(2/24)	V41	V20-(V20-V43)*(21/23)
V10	V8-(V8-V20)*(4/24)	V42	V20-(V20-V43)*(22/23)
V11	V8-(V8-V20)*(6/24)	V43	VINN4
V12	V8-(V8-V20)*(8/24)	V44	V43-(V43-V55)*(2/24)
V13	V8-(V8-V20)*(10/24)	V45	V43-(V43-V55)*(4/24)
V14	V8-(V8-V20)*(12/24)	V46	V43-(V43-V55)*(6/24)
V15	V8-(V8-V20)*(14/24)	V47	V43-(V43-V55)*(8/24)
V16	V8-(V8-V20)*(16/24)	V48	V43-(V43-V55)*(10/24)
V17	V8-(V8-V20)*(18/24)	V49	V43-(V43-V55)*(12/24)
V18	V8-(V8-V20)*(20/24)	V50	V43-(V43-V55)*(14/24)
V19	V8-(V8-V20)*(22/24)	V51	V43-(V43-V55)*(16/24)
V20	VINN3	V52	V43-(V43-V55)*(18/24)
V21	V20-(V20-V43)*(1/23)	V53	V43-(V43-V55)*(20/24)
V22	V20-(V20-V43)*(2/23)	V54	V43-(V43-V55)*(22/24)
V23	V20-(V20-V43)*(3/23)	V55	VINN5
V24	V20-(V20-V43)*(4/23)	V56	V55-(V55-V62)*(9/96)
V25	V20-(V20-V43)*(5/23)	V57	V55-(V55-V62)*(18/96)
V26	V20-(V20-V43)*(6/23)	V58	V55-(V55-V62)*(27/96)
V27	V20-(V20-V43)*(7/23)	V59	V55-(V55-V62)*(36/96)
V28	V20-(V20-V43)*(8/23)	V60	V55-(V55-V62)*(54/96)
V29	V20-(V20-V43)*(9/23)	V61	V55-(V55-V62)*(68/96)
V30	V20-(V20-V43)*(10/23)	V62	VINN6
V31	V20-(V20-V43)*(11/23)	V63	VINN7

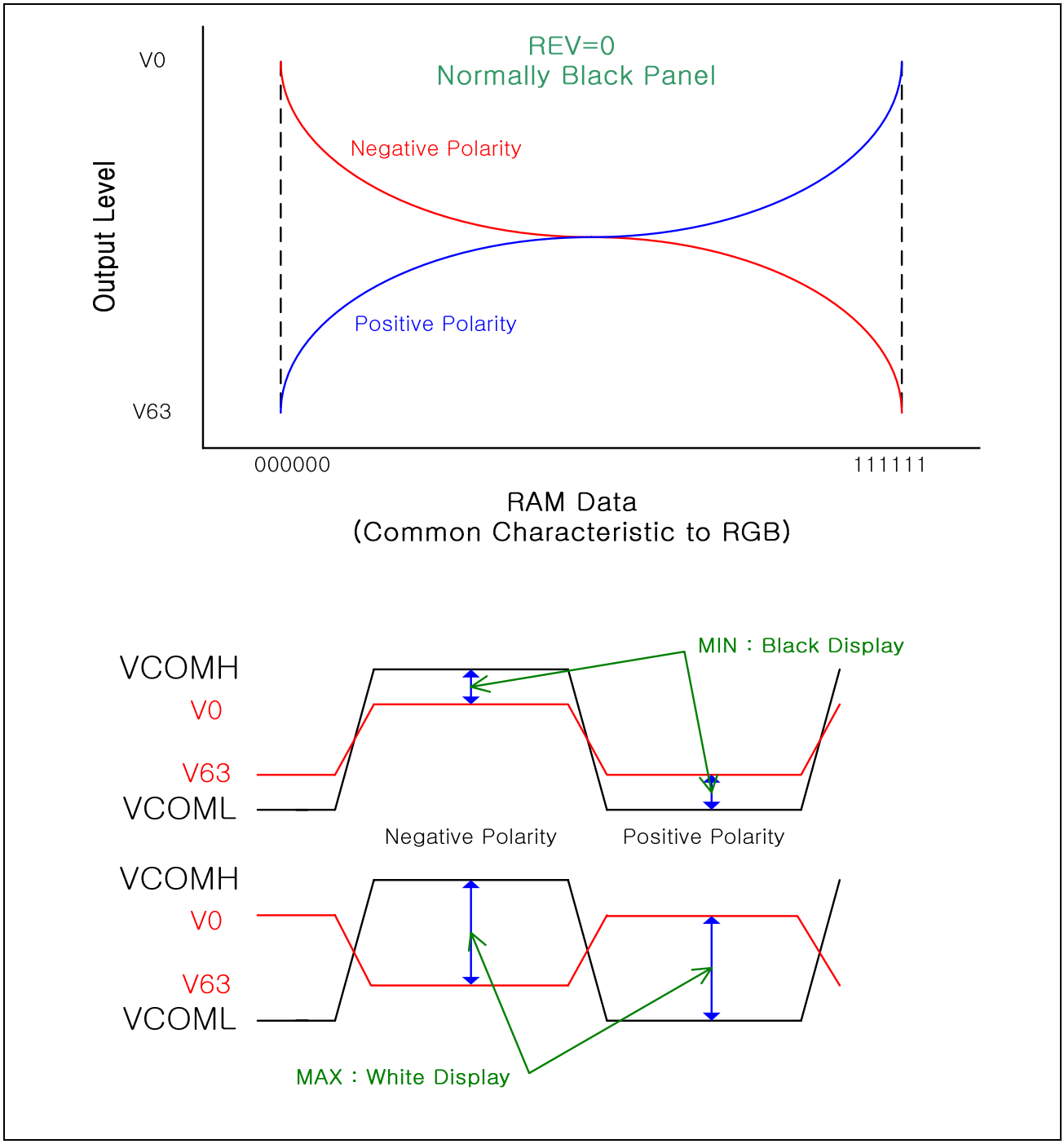


Figure 125. Relationship Between RAM Data , Source Output Voltage and VCOM (REV=0)

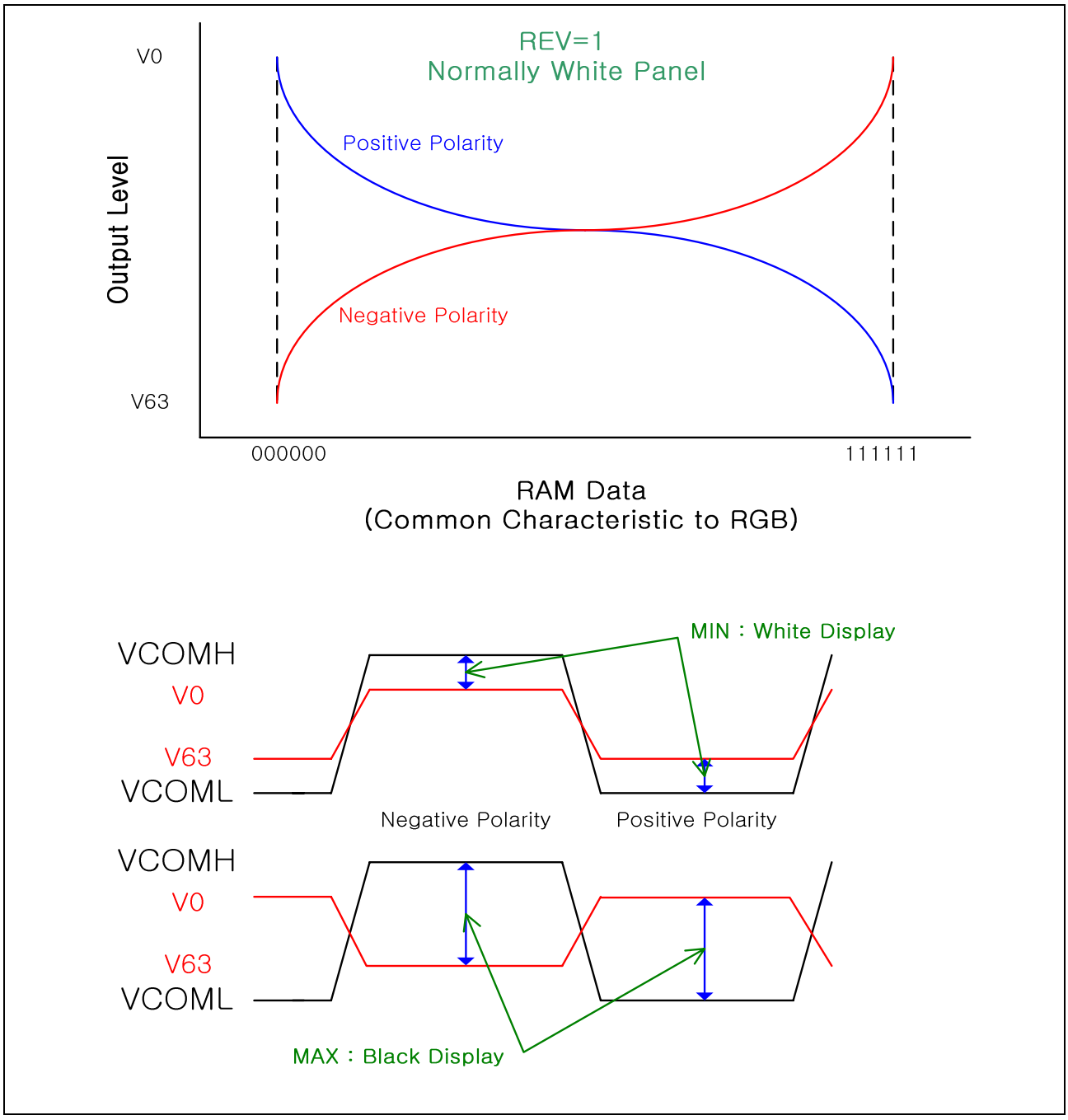


Figure 126. Relationship Between RAM Data , Source Output Voltage and VCOM (REV=1)

15. THE 8-COLOR DISPLAY MODE

The S6D0154 incorporates 8-color display mode. The grayscale levels to be used are V0 (GVDD) and V63 (AVSS) and all the other levels (V1~V62) are halt. So that it attempts to lower power consumption.

During the 8-color mode, the Gamma micro adjustment register, PKP00-PKP52 and PKN00-PKN52 are invalid.

The grayscale levels (V1-V62) are in OFF condition in order to select V0/V63.

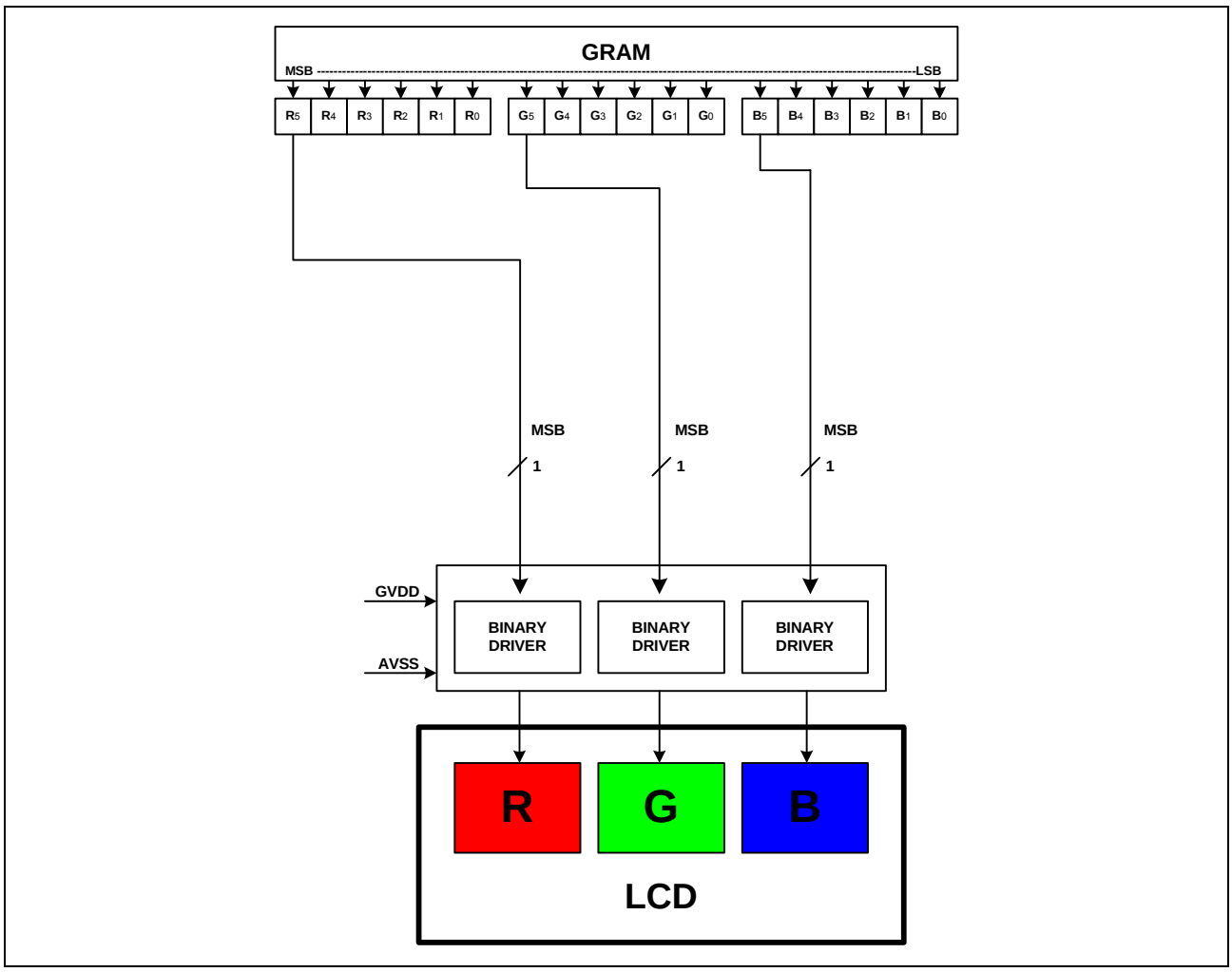


Figure 127. 8-Color Display Control

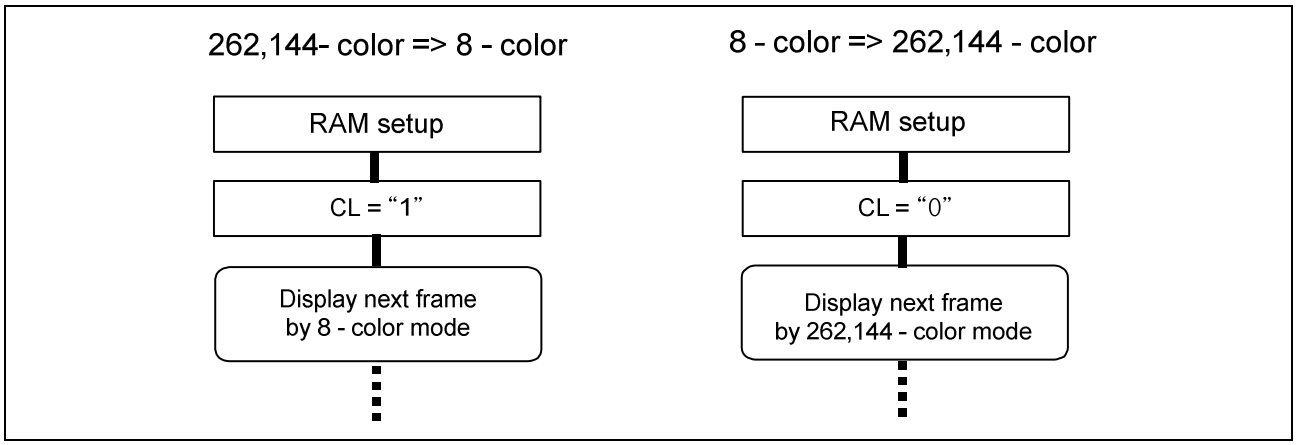


Figure 128. Setup Procedure For The 8-Color Mode

16. INSTRUCTION SET UP FLOW

16.1. DISPLAY ON / OFF SEQUENCE

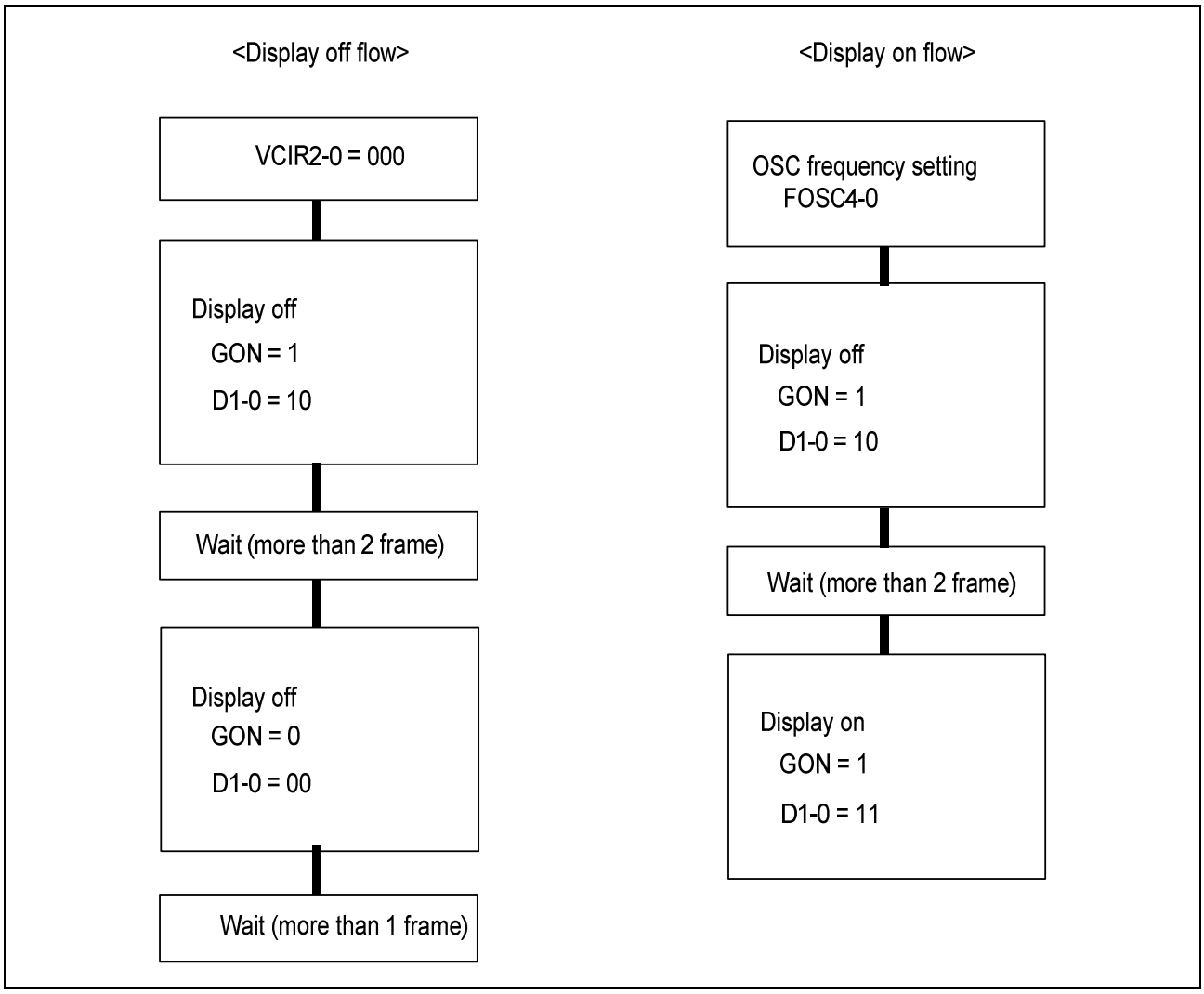


Figure 129. DISPLAY ON / OFF SEQUENCE

16.2. D-STAND-BY / STAND-BY SEQUENCE

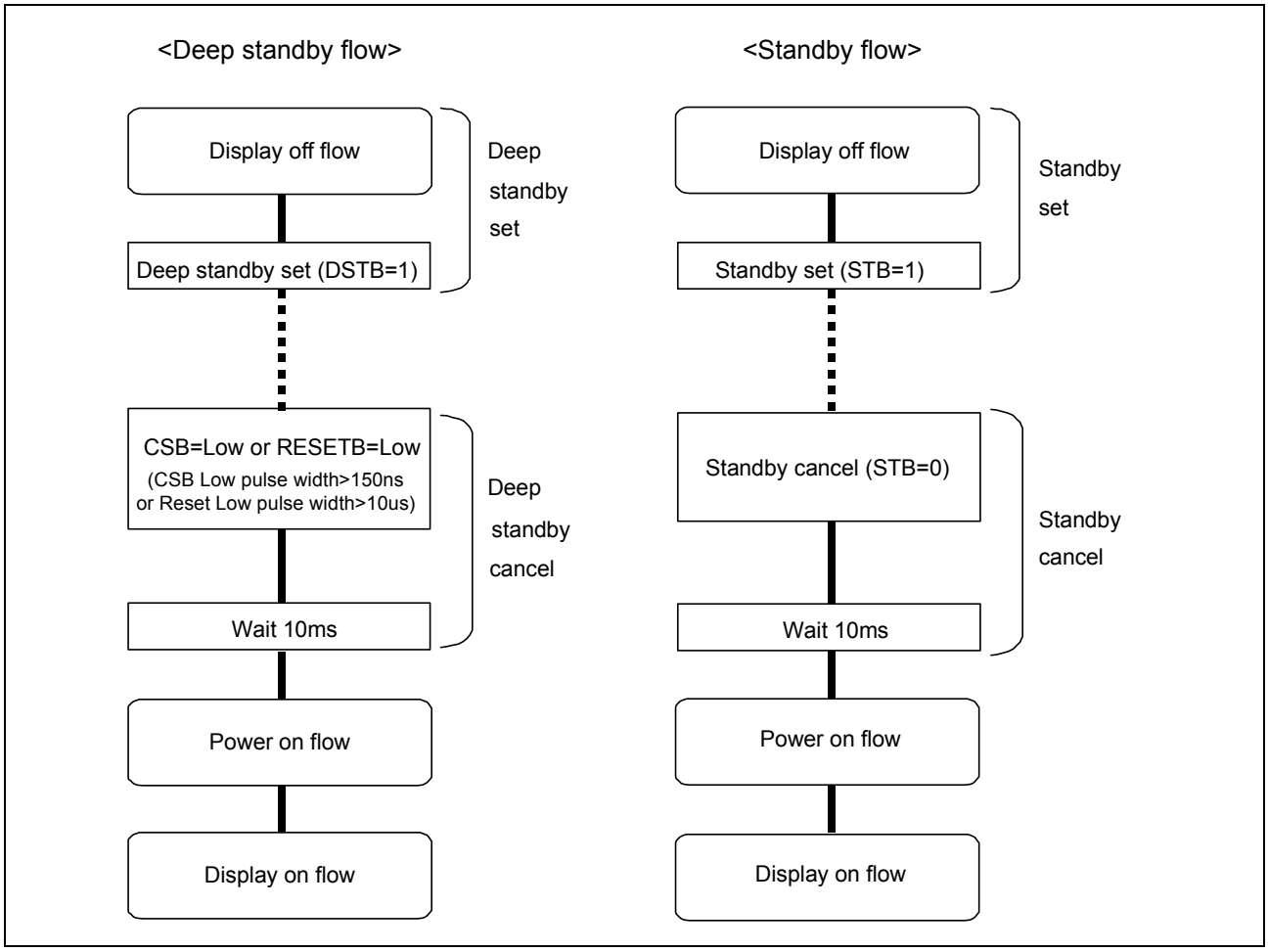


Figure 130. D-STAND-BY/STAND-BY SEQUENCE

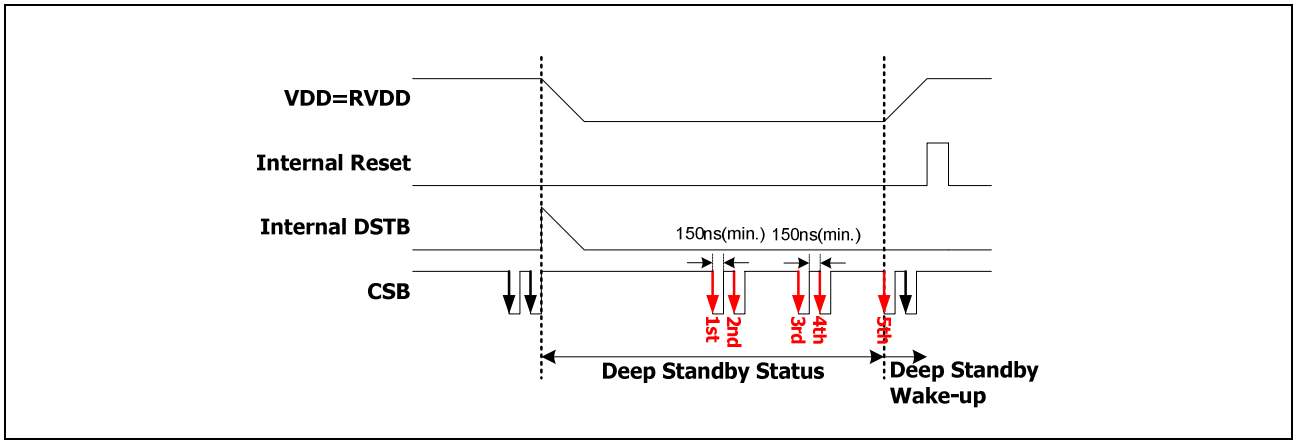


Figure 131. DEEP STAND-BY EXIT FLOW

17. OSCILLATION CIRCUIT

The S6D0154 can provide R-C oscillation. S6D0154 internal oscillator does not need to attach the external resistor. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the oscillator frequency control register setting. Since R-C oscillation stops during the standby mode, power consumption can be reduced.

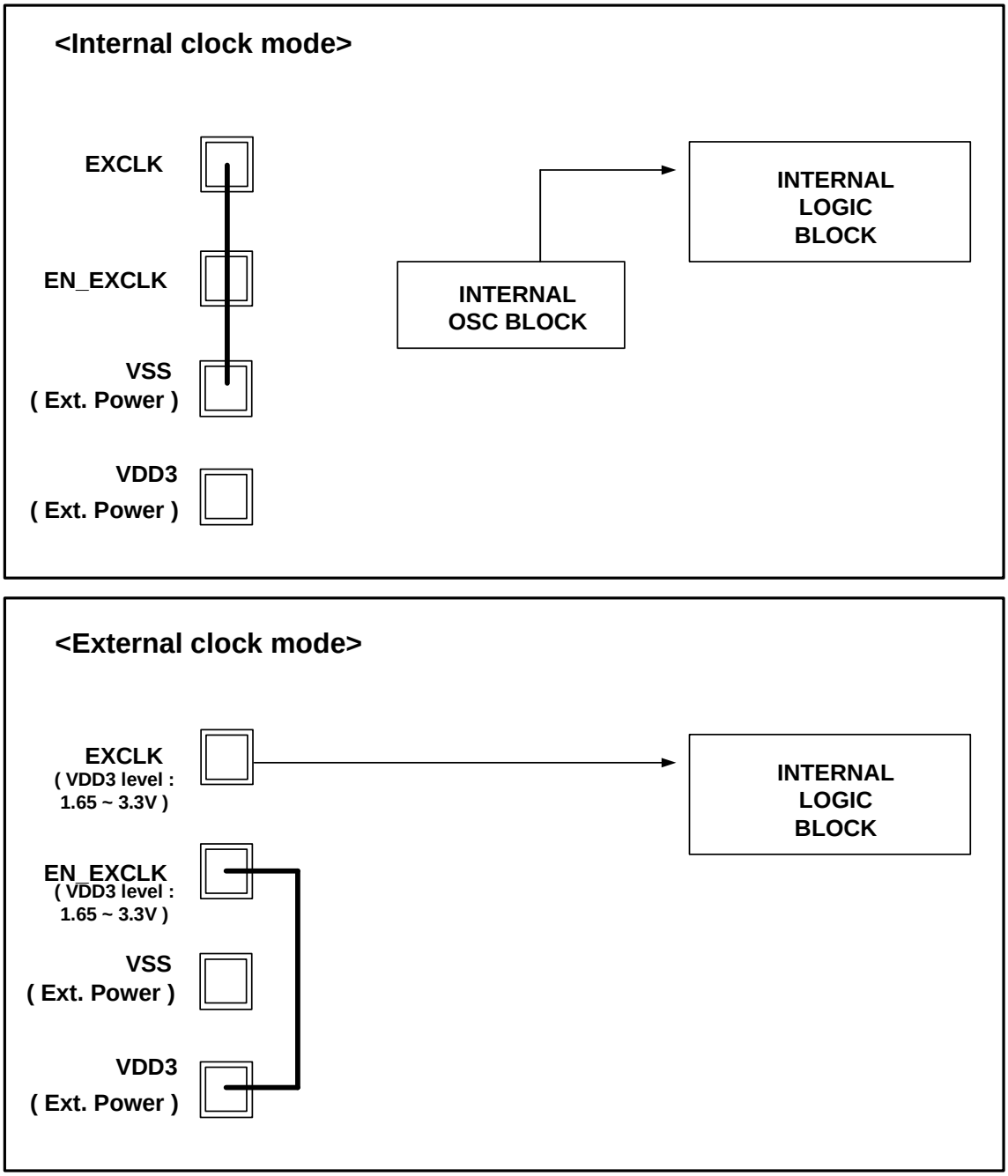


Figure 132. Oscillation Circuit

18. FRAME FREQUENCY ADJUSTING FUNCTION

The S6D0154 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (RTN) during the LCD driver as the oscillation frequency is always same.
If the oscillation frequency is set to high, animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching for an animated display, etc. is required, the frame frequency can be set high.

18.1. Relationship between LCD drive duty and frame frequency

The relationships between the LCD drive duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the 1H period adjusting bit (RTN).

$$\text{Frame Frequency} = \frac{f_{osc}}{\text{Clock cycles per raster-row x (Line+B)}} \text{ [Hz]}$$

f_{osc}: R-C oscillation frequency
Line: Number of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
B: Blank period(Back porch + Front Porch)

Figure 133. Formula for the Frame Frequency

Calculation Example:

Driver raster-rows: 320
1H period: 16 clock (RTN2 to 0 = 000)
B: Blank period (BP + FP): 16

f_osc = 60Hz x 16 clock x (320 + 16) lines = 323 [kHz]

The calculation result says that the required oscillation frequency in the display condition listed above is 323 kHz. So the external resistance value of the R-C oscillator should be selected to make oscillation frequency 323 kHz.

19. Appendices

19.1. PAD COORDINATES

Table 58. Pad Center Coordinates

No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y
1	DUMMY<1>	-9065	-385	51	VCI1	-6065	-385	101	C31M	-3065	-385
2	DUMMY<2>	-9005	-385	52	VCI1	-6005	-385	102	C31M	-3005	-385
3	VCOM	-8945	-385	53	VCI1	-5945	-385	103	C31M	-2945	-385
4	VCOM	-8885	-385	54	VCI1	-5885	-385	104	C31M	-2885	-385
5	VCOM	-8825	-385	55	VCI1	-5825	-385	105	C31M	-2825	-385
6	VCOM	-8765	-385	56	VCI1	-5765	-385	106	C31M	-2765	-385
7	VCOM	-8705	-385	57	VCI1	-5705	-385	107	VCL	-2705	-385
8	VCOM	-8645	-385	58	VCI1	-5645	-385	108	VCL	-2645	-385
9	VCOM	-8585	-385	59	C11P	-5585	-385	109	VCL	-2585	-385
10	VCOM	-8525	-385	60	C11P	-5525	-385	110	VCL	-2525	-385
11	DUMMY<3>	-8465	-385	61	C11P	-5465	-385	111	VCL	-2465	-385
12	VGH	-8405	-385	62	C11P	-5405	-385	112	VCL	-2405	-385
13	VGH	-8345	-385	63	C11P	-5345	-385	113	VCL	-2345	-385
14	VGH	-8285	-385	64	C11P	-5285	-385	114	VCL	-2285	-385
15	VGH	-8225	-385	65	C11P	-5225	-385	115	VCI	-2225	-385
16	VGH	-8165	-385	66	C11P	-5165	-385	116	VCI	-2165	-385
17	DUMMY<4>	-8105	-385	67	C11M	-5105	-385	117	VCI	-2105	-385
18	VGL	-8045	-385	68	C11M	-5045	-385	118	VCI	-2045	-385
19	VGL	-7985	-385	69	C11M	-4985	-385	119	VCI	-1985	-385
20	VGL	-7925	-385	70	C11M	-4925	-385	120	VCI	-1925	-385
21	VGL	-7865	-385	71	C11M	-4865	-385	121	VCI	-1865	-385
22	VGL	-7805	-385	72	C11M	-4805	-385	122	VCI	-1805	-385
23	DUMMY<5>	-7745	-385	73	C11M	-4745	-385	123	VCI	-1745	-385
24	C22P	-7685	-385	74	C11M	-4685	-385	124	VCI	-1685	-385
25	C22P	-7625	-385	75	C12P	-4625	-385	125	AVDD	-1625	-385
26	C22P	-7565	-385	76	C12P	-4565	-385	126	AVDD	-1565	-385
27	DUMMY<6>	-7505	-385	77	C12P	-4505	-385	127	AVDD	-1505	-385
28	C22M	-7445	-385	78	C12P	-4445	-385	128	AVDD	-1445	-385
29	C22M	-7385	-385	79	C12P	-4385	-385	129	AVDD	-1385	-385
30	C22M	-7325	-385	80	C12P	-4325	-385	130	AVDD	-1325	-385
31	DUMMY<7>	-7265	-385	81	C12P	-4265	-385	131	AVDD	-1265	-385
32	C21P	-7205	-385	82	C12P	-4205	-385	132	AVDD	-1205	-385
33	C21P	-7145	-385	83	C12M	-4145	-385	133	AVDD	-1145	-385
34	C21P	-7085	-385	84	C12M	-4085	-385	134	AVDD	-1085	-385
35	DUMMY<8>	-7025	-385	85	C12M	-4025	-385	135	DUMMY<11>	-1025	-385
36	C21M	-6965	-385	86	C12M	-3965	-385	136	RS	-965	-385
37	C21M	-6905	-385	87	C12M	-3905	-385	137	CSB	-905	-385
38	C21M	-6845	-385	88	C12M	-3845	-385	138	VSYNC	-845	-385
39	DUMMY<9>	-6785	-385	89	C12M	-3785	-385	139	HSYNC	-785	-385
40	DUMMY<10>	-6725	-385	90	C12M	-3725	-385	140	DOTCLK	-725	-385
41	VSSC	-6665	-385	91	C31P	-3665	-385	141	ENABLE	-665	-385
42	VSSC	-6605	-385	92	C31P	-3605	-385	142	RESETB	-605	-385
43	VSSC	-6545	-385	93	C31P	-3545	-385	143	SDI	-545	-385
44	VSSC	-6485	-385	94	C31P	-3485	-385	144	E_RDB	-485	-385
45	VSSC	-6425	-385	95	C31P	-3425	-385	145	RW_WRB	-425	-385
46	VSSC	-6365	-385	96	C31P	-3365	-385	146	IM<3>	-365	-385
47	VSSC	-6305	-385	97	C31P	-3305	-385	147	IM<2>	-305	-385
48	VSSC	-6245	-385	98	C31P	-3245	-385	148	IM<1>	-245	-385
49	VSSC	-6185	-385	99	C31M	-3185	-385	149	IM<0>	-185	-385
50	VSSC	-6125	-385	100	C31M	-3125	-385	150	DB<17>	-125	-385

Table 59. Pad Center Coordinates

No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y
151	DB<16>	-40	-385	201	VSS	3485	-385	251	VSS_MDDI	6485	-385
152	DB<15>	45	-385	202	VSS	3545	-385	252	MDP	6545	-385
153	DB<14>	130	-385	203	VSS	3605	-385	253	MDP	6605	-385
154	DB<13>	215	-385	204	VSS	3665	-385	254	MDP	6665	-385
155	DB<12>	300	-385	205	VSS	3725	-385	255	MDN	6725	-385
156	DB<11>	385	-385	206	VSS	3785	-385	256	MDN	6785	-385
157	DB<10>	470	-385	207	VSS	3845	-385	257	MDN	6845	-385
158	DB<9>	555	-385	208	VSS	3905	-385	258	MSP	6905	-385
159	DB<8>	640	-385	209	VSS	3965	-385	259	MSP	6965	-385
160	DB<7>	725	-385	210	VSS	4025	-385	260	MSP	7025	-385
161	DB<6>	810	-385	211	VSS	4085	-385	261	MSN	7085	-385
162	DB<5>	895	-385	212	VSS	4145	-385	262	MSN	7145	-385
163	DB<4>	980	-385	213	VSS	4205	-385	263	MSN	7205	-385
164	DB<3>	1065	-385	214	VSS	4265	-385	264	DUMMY<12>	7265	-385
165	DB<2>	1150	-385	215	VSS	4325	-385	265	VREFI	7325	-385
166	DB<1>	1235	-385	216	VSS	4385	-385	266	GVDD	7385	-385
167	DB<0>	1320	-385	217	VSS	4445	-385	267	GVDD	7445	-385
168	SDO	1405	-385	218	VSS	4505	-385	268	GVDD	7505	-385
169	M	1490	-385	219	VDD	4565	-385	269	GVDD	7565	-385
170	FLM	1575	-385	220	VDD	4625	-385	270	GVDD	7625	-385
171	CL1	1660	-385	221	VDD	4685	-385	271	VCOMH	7685	-385
172	TEST_MODE<2>	1745	-385	222	VDD	4745	-385	272	VCOMH	7745	-385
173	TEST_MODE<1>	1805	-385	223	VDD	4805	-385	273	VCOMH	7805	-385
174	TEST_MODE<0>	1865	-385	224	VDD	4865	-385	274	VCOMH	7865	-385
175	SD	1925	-385	225	RVDD	4925	-385	275	VCOMH	7925	-385
176	CM	1985	-385	226	RVDD	4985	-385	276	VCOML	7985	-385
177	BGR	2045	-385	227	RVDD	5045	-385	277	VCOML	8045	-385
178	RL	2105	-385	228	RVDD	5105	-385	278	VCOML	8105	-385
179	TB	2165	-385	229	RVDD	5165	-385	279	VCOML	8165	-385
180	PNP_EN	2225	-385	230	RVDD	5225	-385	280	VCOML	8225	-385
181	EN_EXCLK	2285	-385	231	VDD3	5285	-385	281	VCOMR	8285	-385
182	EXCLK	2345	-385	232	VDD3	5345	-385	282	*CONTACT<1>	8345	-385
183	VGS	2405	-385	233	VDD3	5405	-385	283	*CONTACT<2>	8405	-385
184	VGS	2465	-385	234	VDD3	5465	-385	284	DUMMY<13>	8465	-385
185	VGS	2525	-385	235	VDD3	5525	-385	285	VCOM	8525	-385
186	AVSS	2585	-385	236	VDD3	5585	-385	286	VCOM	8585	-385
187	AVSS	2645	-385	237	VDD3	5645	-385	287	VCOM	8645	-385
188	AVSS	2705	-385	238	VDD3	5705	-385	288	VCOM	8705	-385
189	AVSS	2765	-385	239	VCI_MDDI	5765	-385	289	VCOM	8765	-385
190	AVSS	2825	-385	240	VCI_MDDI	5825	-385	290	VCOM	8825	-385
191	AVSS	2885	-385	241	VCI_MDDI	5885	-385	291	VCOM	8885	-385
192	AVSS	2945	-385	242	VCI_MDDI	5945	-385	292	VCOM	8945	-385
193	AVSS	3005	-385	243	VCI_MDDI	6005	-385	293	DUMMY<14>	9005	-385
194	AVSS	3065	-385	244	VCI_MDDI	6065	-385	294	DUMMY<15>	9065	-385
195	AVSS	3125	-385	245	VSS_MDDI	6125	-385	295	DUMMY<16>	9123	354
196	AVSS	3185	-385	246	VSS_MDDI	6185	-385	296	DUMMY<17>	9107	201
197	AVSS	3245	-385	247	VSS_MDDI	6245	-385	297	DUMMY<18>	9091	354
198	AVSS	3305	-385	248	VSS_MDDI	6305	-385	298	DUMMY<19>	9075	201
199	AVSS	3365	-385	249	VSS_MDDI	6365	-385	299	G<2>	9059	354
200	AVSS	3425	-385	250	VSS_MDDI	6425	-385	300	G<4>	9043	201

Note. CONTACT<1> and CONTACT<2> pads are VSS level.

Table 60. Pad Center Coordinates

No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y
301	G<6>	9027	354	351	G<106>	8227	354	401	G<206>	7427	354
302	G<8>	9011	201	352	G<108>	8211	201	402	G<208>	7411	201
303	G<10>	8995	354	353	G<110>	8195	354	403	G<210>	7395	354
304	G<12>	8979	201	354	G<112>	8179	201	404	G<212>	7379	201
305	G<14>	8963	354	355	G<114>	8163	354	405	G<214>	7363	354
306	G<16>	8947	201	356	G<116>	8147	201	406	G<216>	7347	201
307	G<18>	8931	354	357	G<118>	8131	354	407	G<218>	7331	354
308	G<20>	8915	201	358	G<120>	8115	201	408	G<220>	7315	201
309	G<22>	8899	354	359	G<122>	8099	354	409	G<222>	7299	354
310	G<24>	8883	201	360	G<124>	8083	201	410	G<224>	7283	201
311	G<26>	8867	354	361	G<126>	8067	354	411	G<226>	7267	354
312	G<28>	8851	201	362	G<128>	8051	201	412	G<228>	7251	201
313	G<30>	8835	354	363	G<130>	8035	354	413	G<230>	7235	354
314	G<32>	8819	201	364	G<132>	8019	201	414	G<232>	7219	201
315	G<34>	8803	354	365	G<134>	8003	354	415	G<234>	7203	354
316	G<36>	8787	201	366	G<136>	7987	201	416	G<236>	7187	201
317	G<38>	8771	354	367	G<138>	7971	354	417	G<238>	7171	354
318	G<40>	8755	201	368	G<140>	7955	201	418	G<240>	7155	201
319	G<42>	8739	354	369	G<142>	7939	354	419	G<242>	7139	354
320	G<44>	8723	201	370	G<144>	7923	201	420	G<244>	7123	201
321	G<46>	8707	354	371	G<146>	7907	354	421	G<246>	7107	354
322	G<48>	8691	201	372	G<148>	7891	201	422	G<248>	7091	201
323	G<50>	8675	354	373	G<150>	7875	354	423	G<250>	7075	354
324	G<52>	8659	201	374	G<152>	7859	201	424	G<252>	7059	201
325	G<54>	8643	354	375	G<154>	7843	354	425	G<254>	7043	354
326	G<56>	8627	201	376	G<156>	7827	201	426	G<256>	7027	201
327	G<58>	8611	354	377	G<158>	7811	354	427	G<258>	7011	354
328	G<60>	8595	201	378	G<160>	7795	201	428	G<260>	6995	201
329	G<62>	8579	354	379	G<162>	7779	354	429	G<262>	6979	354
330	G<64>	8563	201	380	G<164>	7763	201	430	G<264>	6963	201
331	G<66>	8547	354	381	G<166>	7747	354	431	G<266>	6947	354
332	G<68>	8531	201	382	G<168>	7731	201	432	G<268>	6931	201
333	G<70>	8515	354	383	G<170>	7715	354	433	G<270>	6915	354
334	G<72>	8499	201	384	G<172>	7699	201	434	G<272>	6899	201
335	G<74>	8483	354	385	G<174>	7683	354	435	G<274>	6883	354
336	G<76>	8467	201	386	G<176>	7667	201	436	G<276>	6867	201
337	G<78>	8451	354	387	G<178>	7651	354	437	G<278>	6851	354
338	G<80>	8435	201	388	G<180>	7635	201	438	G<280>	6835	201
339	G<82>	8419	354	389	G<182>	7619	354	439	G<282>	6819	354
340	G<84>	8403	201	390	G<184>	7603	201	440	G<284>	6803	201
341	G<86>	8387	354	391	G<186>	7587	354	441	G<286>	6787	354
342	G<88>	8371	201	392	G<188>	7571	201	442	G<288>	6771	201
343	G<90>	8355	354	393	G<190>	7555	354	443	G<290>	6755	354
344	G<92>	8339	201	394	G<192>	7539	201	444	G<292>	6739	201
345	G<94>	8323	354	395	G<194>	7523	354	445	G<294>	6723	354
346	G<96>	8307	201	396	G<196>	7507	201	446	G<296>	6707	201
347	G<98>	8291	354	397	G<198>	7491	354	447	G<298>	6691	354
348	G<100>	8275	201	398	G<200>	7475	201	448	G<300>	6675	201
349	G<102>	8259	354	399	G<202>	7459	354	449	G<302>	6659	354
350	G<104>	8243	201	400	G<204>	7443	201	450	G<304>	6643	201

Table 61. Pad Center Coordinates

No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y
451	G<306>	6627	354	501	S<687>	5827	354	551	S<637>	5027	354
452	G<308>	6611	201	502	S<686>	5811	201	552	S<636>	5011	201
453	G<310>	6595	354	503	S<685>	5795	354	553	S<635>	4995	354
454	G<312>	6579	201	504	S<684>	5779	201	554	S<634>	4979	201
455	G<314>	6563	354	505	S<683>	5763	354	555	S<633>	4963	354
456	G<316>	6547	201	506	S<682>	5747	201	556	S<632>	4947	201
457	G<318>	6531	354	507	S<681>	5731	354	557	S<631>	4931	354
458	G<320>	6515	201	508	S<680>	5715	201	558	S<630>	4915	201
459	DUMMY<20>	6499	354	509	S<679>	5699	354	559	S<629>	4899	354
460	DUMMY<21>	6483	201	510	S<678>	5683	201	560	S<628>	4883	201
461	DUMMY<22>	6467	354	511	S<677>	5667	354	561	S<627>	4867	354
462	DUMMY<23>	6451	201	512	S<676>	5651	201	562	S<626>	4851	201
463	DUMMY<24>	6435	354	513	S<675>	5635	354	563	S<625>	4835	354
464	DUMMY<25>	6419	201	514	S<674>	5619	201	564	S<624>	4819	201
465	DUMMY<26>	6403	354	515	S<673>	5603	354	565	S<623>	4803	354
466	DUMMY<27>	6387	201	516	S<672>	5587	201	566	S<622>	4787	201
467	DUMMY<28>	6371	354	517	S<671>	5571	354	567	S<621>	4771	354
468	S<720>	6355	201	518	S<670>	5555	201	568	S<620>	4755	201
469	S<719>	6339	354	519	S<669>	5539	354	569	S<619>	4739	354
470	S<718>	6323	201	520	S<668>	5523	201	570	S<618>	4723	201
471	S<717>	6307	354	521	S<667>	5507	354	571	S<617>	4707	354
472	S<716>	6291	201	522	S<666>	5491	201	572	S<616>	4691	201
473	S<715>	6275	354	523	S<665>	5475	354	573	S<615>	4675	354
474	S<714>	6259	201	524	S<664>	5459	201	574	S<614>	4659	201
475	S<713>	6243	354	525	S<663>	5443	354	575	S<613>	4643	354
476	S<712>	6227	201	526	S<662>	5427	201	576	S<612>	4627	201
477	S<711>	6211	354	527	S<661>	5411	354	577	S<611>	4611	354
478	S<710>	6195	201	528	S<660>	5395	201	578	S<610>	4595	201
479	S<709>	6179	354	529	S<659>	5379	354	579	S<609>	4579	354
480	S<708>	6163	201	530	S<658>	5363	201	580	S<608>	4563	201
481	S<707>	6147	354	531	S<657>	5347	354	581	S<607>	4547	354
482	S<706>	6131	201	532	S<656>	5331	201	582	S<606>	4531	201
483	S<705>	6115	354	533	S<655>	5315	354	583	S<605>	4515	354
484	S<704>	6099	201	534	S<654>	5299	201	584	S<604>	4499	201
485	S<703>	6083	354	535	S<653>	5283	354	585	S<603>	4483	354
486	S<702>	6067	201	536	S<652>	5267	201	586	S<602>	4467	201
487	S<701>	6051	354	537	S<651>	5251	354	587	S<601>	4451	354
488	S<700>	6035	201	538	S<650>	5235	201	588	S<600>	4435	201
489	S<699>	6019	354	539	S<649>	5219	354	589	S<599>	4419	354
490	S<698>	6003	201	540	S<648>	5203	201	590	S<598>	4403	201
491	S<697>	5987	354	541	S<647>	5187	354	591	S<597>	4387	354
492	S<696>	5971	201	542	S<646>	5171	201	592	S<596>	4371	201
493	S<695>	5955	354	543	S<645>	5155	354	593	S<595>	4355	354
494	S<694>	5939	201	544	S<644>	5139	201	594	S<594>	4339	201
495	S<693>	5923	354	545	S<643>	5123	354	595	S<593>	4323	354
496	S<692>	5907	201	546	S<642>	5107	201	596	S<592>	4307	201
497	S<691>	5891	354	547	S<641>	5091	354	597	S<591>	4291	354
498	S<690>	5875	201	548	S<640>	5075	201	598	S<590>	4275	201
499	S<689>	5859	354	549	S<639>	5059	354	599	S<589>	4259	354
500	S<688>	5843	201	550	S<638>	5043	201	600	S<588>	4243	201

Table 62. Pad Center Coordinates

No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y
601	S<587>	4227	354	651	S<537>	3377	354	701	S<487>	2577	354
602	S<586>	4211	201	652	S<536>	3361	201	702	S<486>	2561	201
603	S<585>	4195	354	653	S<535>	3345	354	703	S<485>	2545	354
604	S<584>	4179	201	654	S<534>	3329	201	704	S<484>	2529	201
605	S<583>	4163	354	655	S<533>	3313	354	705	S<483>	2513	354
606	S<582>	4147	201	656	S<532>	3297	201	706	S<482>	2497	201
607	S<581>	4131	354	657	S<531>	3281	354	707	S<481>	2481	354
608	S<580>	4115	201	658	S<530>	3265	201	708	S<480>	2465	201
609	S<579>	4099	354	659	S<529>	3249	354	709	S<479>	2449	354
610	S<578>	4083	201	660	S<528>	3233	201	710	S<478>	2433	201
611	S<577>	4067	354	661	S<527>	3217	354	711	S<477>	2417	354
612	S<576>	4051	201	662	S<526>	3201	201	712	S<476>	2401	201
613	S<575>	4035	354	663	S<525>	3185	354	713	S<475>	2385	354
614	S<574>	4019	201	664	S<524>	3169	201	714	S<474>	2369	201
615	S<573>	4003	354	665	S<523>	3153	354	715	S<473>	2353	354
616	S<572>	3987	201	666	S<522>	3137	201	716	S<472>	2337	201
617	S<571>	3971	354	667	S<521>	3121	354	717	S<471>	2321	354
618	S<570>	3955	201	668	S<520>	3105	201	718	S<470>	2305	201
619	S<569>	3939	354	669	S<519>	3089	354	719	S<469>	2289	354
620	S<568>	3923	201	670	S<518>	3073	201	720	S<468>	2273	201
621	S<567>	3907	354	671	S<517>	3057	354	721	S<467>	2257	354
622	S<566>	3891	201	672	S<516>	3041	201	722	S<466>	2241	201
623	S<565>	3875	354	673	S<515>	3025	354	723	S<465>	2225	354
624	S<564>	3859	201	674	S<514>	3009	201	724	S<464>	2209	201
625	S<563>	3843	354	675	S<513>	2993	354	725	S<463>	2193	354
626	S<562>	3827	201	676	S<512>	2977	201	726	S<462>	2177	201
627	S<561>	3811	354	677	S<511>	2961	354	727	S<461>	2161	354
628	S<560>	3795	201	678	S<510>	2945	201	728	S<460>	2145	201
629	S<559>	3779	354	679	S<509>	2929	354	729	S<459>	2129	354
630	S<558>	3763	201	680	S<508>	2913	201	730	S<458>	2113	201
631	S<557>	3747	354	681	S<507>	2897	354	731	S<457>	2097	354
632	S<556>	3731	201	682	S<506>	2881	201	732	S<456>	2081	201
633	S<555>	3715	354	683	S<505>	2865	354	733	S<455>	2065	354
634	S<554>	3699	201	684	S<504>	2849	201	734	S<454>	2049	201
635	S<553>	3683	354	685	S<503>	2833	354	735	S<453>	2033	354
636	S<552>	3667	201	686	S<502>	2817	201	736	S<452>	2017	201
637	S<551>	3651	354	687	S<501>	2801	354	737	S<451>	2001	354
638	S<550>	3635	201	688	S<500>	2785	201	738	S<450>	1985	201
639	S<549>	3619	354	689	S<499>	2769	354	739	S<449>	1969	354
640	S<548>	3603	201	690	S<498>	2753	201	740	S<448>	1953	201
641	S<547>	3587	354	691	S<497>	2737	354	741	S<447>	1937	354
642	S<546>	3571	201	692	S<496>	2721	201	742	S<446>	1921	201
643	S<545>	3555	354	693	S<495>	2705	354	743	S<445>	1905	354
644	S<544>	3539	201	694	S<494>	2689	201	744	S<444>	1889	201
645	S<543>	3523	354	695	S<493>	2673	354	745	S<443>	1873	354
646	S<542>	3507	201	696	S<492>	2657	201	746	S<442>	1857	201
647	S<541>	3491	354	697	S<491>	2641	354	747	S<441>	1841	354
648	S<540>	3425	201	698	S<490>	2625	201	748	S<440>	1825	201
649	S<539>	3409	354	699	S<489>	2609	354	749	S<439>	1809	354
650	S<538>	3393	201	700	S<488>	2593	201	750	S<438>	1793	201

Table 63. Pad Center Coordinates

No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y
751	S<437>	1777	354	801	S<387>	977	354	851	S<337>	-950	354
752	S<436>	1761	201	802	S<386>	961	201	852	S<336>	-966	201
753	S<435>	1745	354	803	S<385>	945	354	853	S<335>	-982	354
754	S<434>	1729	201	804	S<384>	929	201	854	S<334>	-998	201
755	S<433>	1713	354	805	S<383>	913	354	855	S<333>	-1014	354
756	S<432>	1697	201	806	S<382>	897	201	856	S<332>	-1030	201
757	S<431>	1681	354	807	S<381>	881	354	857	S<331>	-1046	354
758	S<430>	1665	201	808	S<380>	865	201	858	S<330>	-1062	201
759	S<429>	1649	354	809	S<379>	849	354	859	S<329>	-1078	354
760	S<428>	1633	201	810	S<378>	833	201	860	S<328>	-1094	201
761	S<427>	1617	354	811	S<377>	817	354	861	S<327>	-1110	354
762	S<426>	1601	201	812	S<376>	801	201	862	S<326>	-1126	201
763	S<425>	1585	354	813	S<375>	785	354	863	S<325>	-1142	354
764	S<424>	1569	201	814	S<374>	769	201	864	S<324>	-1158	201
765	S<423>	1553	354	815	S<373>	753	354	865	S<323>	-1174	354
766	S<422>	1537	201	816	S<372>	737	201	866	S<322>	-1190	201
767	S<421>	1521	354	817	S<371>	721	354	867	S<321>	-1206	354
768	S<420>	1505	201	818	S<370>	705	201	868	S<320>	-1222	201
769	S<419>	1489	354	819	S<369>	689	354	869	S<319>	-1238	354
770	S<418>	1473	201	820	S<368>	673	201	870	S<318>	-1254	201
771	S<417>	1457	354	821	S<367>	657	354	871	S<317>	-1270	354
772	S<416>	1441	201	822	S<366>	641	201	872	S<316>	-1286	201
773	S<415>	1425	354	823	S<365>	625	354	873	S<315>	-1302	354
774	S<414>	1409	201	824	S<364>	609	201	874	S<314>	-1318	201
775	S<413>	1393	354	825	S<363>	593	354	875	S<313>	-1334	354
776	S<412>	1377	201	826	S<362>	577	201	876	S<312>	-1350	201
777	S<411>	1361	354	827	S<361>	561	354	877	S<311>	-1366	354
778	S<410>	1345	201	828	S<360>	-582	201	878	S<310>	-1382	201
779	S<409>	1329	354	829	S<359>	-598	354	879	S<309>	-1398	354
780	S<408>	1313	201	830	S<358>	-614	201	880	S<308>	-1414	201
781	S<407>	1297	354	831	S<357>	-630	354	881	S<307>	-1430	354
782	S<406>	1281	201	832	S<356>	-646	201	882	S<306>	-1446	201
783	S<405>	1265	354	833	S<355>	-662	354	883	S<305>	-1462	354
784	S<404>	1249	201	834	S<354>	-678	201	884	S<304>	-1478	201
785	S<403>	1233	354	835	S<353>	-694	354	885	S<303>	-1494	354
786	S<402>	1217	201	836	S<352>	-710	201	886	S<302>	-1510	201
787	S<401>	1201	354	837	S<351>	-726	354	887	S<301>	-1526	354
788	S<400>	1185	201	838	S<350>	-742	201	888	S<300>	-1542	201
789	S<399>	1169	354	839	S<349>	-758	354	889	S<299>	-1558	354
790	S<398>	1153	201	840	S<348>	-774	201	890	S<298>	-1574	201
791	S<397>	1137	354	841	S<347>	-790	354	891	S<297>	-1590	354
792	S<396>	1121	201	842	S<346>	-806	201	892	S<296>	-1606	201
793	S<395>	1105	354	843	S<345>	-822	354	893	S<295>	-1622	354
794	S<394>	1089	201	844	S<344>	-838	201	894	S<294>	-1638	201
795	S<393>	1073	354	845	S<343>	-854	354	895	S<293>	-1654	354
796	S<392>	1057	201	846	S<342>	-870	201	896	S<292>	-1670	201
797	S<391>	1041	354	847	S<341>	-886	354	897	S<291>	-1686	354
798	S<390>	1025	201	848	S<340>	-902	201	898	S<290>	-1702	201
799	S<389>	1009	354	849	S<339>	-918	354	899	S<289>	-1718	354
800	S<388>	993	201	850	S<338>	-934	201	900	S<288>	-1734	201

Table 64. Pad Center Coordinates

No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y
901	S<287>	-1750	354	951	S<237>	-2550	354	1001	S<187>	-3350	354
902	S<286>	-1766	201	952	S<236>	-2566	201	1002	S<186>	-3366	201
903	S<285>	-1782	354	953	S<235>	-2582	354	1003	S<185>	-3382	354
904	S<284>	-1798	201	954	S<234>	-2598	201	1004	S<184>	-3398	201
905	S<283>	-1814	354	955	S<233>	-2614	354	1005	S<183>	-3414	354
906	S<282>	-1830	201	956	S<232>	-2630	201	1006	S<182>	-3430	201
907	S<281>	-1846	354	957	S<231>	-2646	354	1007	S<181>	-3446	354
908	S<280>	-1862	201	958	S<230>	-2662	201	1008	S<180>	-3512	201
909	S<279>	-1878	354	959	S<229>	-2678	354	1009	S<179>	-3528	354
910	S<278>	-1894	201	960	S<228>	-2694	201	1010	S<178>	-3544	201
911	S<277>	-1910	354	961	S<227>	-2710	354	1011	S<177>	-3560	354
912	S<276>	-1926	201	962	S<226>	-2726	201	1012	S<176>	-3576	201
913	S<275>	-1942	354	963	S<225>	-2742	354	1013	S<175>	-3592	354
914	S<274>	-1958	201	964	S<224>	-2758	201	1014	S<174>	-3608	201
915	S<273>	-1974	354	965	S<223>	-2774	354	1015	S<173>	-3624	354
916	S<272>	-1990	201	966	S<222>	-2790	201	1016	S<172>	-3640	201
917	S<271>	-2006	354	967	S<221>	-2806	354	1017	S<171>	-3656	354
918	S<270>	-2022	201	968	S<220>	-2822	201	1018	S<170>	-3672	201
919	S<269>	-2038	354	969	S<219>	-2838	354	1019	S<169>	-3688	354
920	S<268>	-2054	201	970	S<218>	-2854	201	1020	S<168>	-3704	201
921	S<267>	-2070	354	971	S<217>	-2870	354	1021	S<167>	-3720	354
922	S<266>	-2086	201	972	S<216>	-2886	201	1022	S<166>	-3736	201
923	S<265>	-2102	354	973	S<215>	-2902	354	1023	S<165>	-3752	354
924	S<264>	-2118	201	974	S<214>	-2918	201	1024	S<164>	-3768	201
925	S<263>	-2134	354	975	S<213>	-2934	354	1025	S<163>	-3784	354
926	S<262>	-2150	201	976	S<212>	-2950	201	1026	S<162>	-3800	201
927	S<261>	-2166	354	977	S<211>	-2966	354	1027	S<161>	-3816	354
928	S<260>	-2182	201	978	S<210>	-2982	201	1028	S<160>	-3832	201
929	S<259>	-2198	354	979	S<209>	-2998	354	1029	S<159>	-3848	354
930	S<258>	-2214	201	980	S<208>	-3014	201	1030	S<158>	-3864	201
931	S<257>	-2230	354	981	S<207>	-3030	354	1031	S<157>	-3880	354
932	S<256>	-2246	201	982	S<206>	-3046	201	1032	S<156>	-3896	201
933	S<255>	-2262	354	983	S<205>	-3062	354	1033	S<155>	-3912	354
934	S<254>	-2278	201	984	S<204>	-3078	201	1034	S<154>	-3928	201
935	S<253>	-2294	354	985	S<203>	-3094	354	1035	S<153>	-3944	354
936	S<252>	-2310	201	986	S<202>	-3110	201	1036	S<152>	-3960	201
937	S<251>	-2326	354	987	S<201>	-3126	354	1037	S<151>	-3976	354
938	S<250>	-2342	201	988	S<200>	-3142	201	1038	S<150>	-3992	201
939	S<249>	-2358	354	989	S<199>	-3158	354	1039	S<149>	-4008	354
940	S<248>	-2374	201	990	S<198>	-3174	201	1040	S<148>	-4024	201
941	S<247>	-2390	354	991	S<197>	-3190	354	1041	S<147>	-4040	354
942	S<246>	-2406	201	992	S<196>	-3206	201	1042	S<146>	-4056	201
943	S<245>	-2422	354	993	S<195>	-3222	354	1043	S<145>	-4072	354
944	S<244>	-2438	201	994	S<194>	-3238	201	1044	S<144>	-4088	201
945	S<243>	-2454	354	995	S<193>	-3254	354	1045	S<143>	-4104	354
946	S<242>	-2470	201	996	S<192>	-3270	201	1046	S<142>	-4120	201
947	S<241>	-2486	354	997	S<191>	-3286	354	1047	S<141>	-4136	354
948	S<240>	-2502	201	998	S<190>	-3302	201	1048	S<140>	-4152	201
949	S<239>	-2518	354	999	S<189>	-3318	354	1049	S<139>	-4168	354
950	S<238>	-2534	201	1000	S<188>	-3334	201	1050	S<138>	-4184	201

Table 65. Pad Center Coordinates

No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y
1051	S<137>	-4200	354	1101	S<87>	-5000	354	1151	S<37>	-5800	354
1052	S<136>	-4216	201	1102	S<86>	-5016	201	1152	S<36>	-5816	201
1053	S<135>	-4232	354	1103	S<85>	-5032	354	1153	S<35>	-5832	354
1054	S<134>	-4248	201	1104	S<84>	-5048	201	1154	S<34>	-5848	201
1055	S<133>	-4264	354	1105	S<83>	-5064	354	1155	S<33>	-5864	354
1056	S<132>	-4280	201	1106	S<82>	-5080	201	1156	S<32>	-5880	201
1057	S<131>	-4296	354	1107	S<81>	-5096	354	1157	S<31>	-5896	354
1058	S<130>	-4312	201	1108	S<80>	-5112	201	1158	S<30>	-5912	201
1059	S<129>	-4328	354	1109	S<79>	-5128	354	1159	S<29>	-5928	354
1060	S<128>	-4344	201	1110	S<78>	-5144	201	1160	S<28>	-5944	201
1061	S<127>	-4360	354	1111	S<77>	-5160	354	1161	S<27>	-5960	354
1062	S<126>	-4376	201	1112	S<76>	-5176	201	1162	S<26>	-5976	201
1063	S<125>	-4392	354	1113	S<75>	-5192	354	1163	S<25>	-5992	354
1064	S<124>	-4408	201	1114	S<74>	-5208	201	1164	S<24>	-6008	201
1065	S<123>	-4424	354	1115	S<73>	-5224	354	1165	S<23>	-6024	354
1066	S<122>	-4440	201	1116	S<72>	-5240	201	1166	S<22>	-6040	201
1067	S<121>	-4456	354	1117	S<71>	-5256	354	1167	S<21>	-6056	354
1068	S<120>	-4472	201	1118	S<70>	-5272	201	1168	S<20>	-6072	201
1069	S<119>	-4488	354	1119	S<69>	-5288	354	1169	S<19>	-6088	354
1070	S<118>	-4504	201	1120	S<68>	-5304	201	1170	S<18>	-6104	201
1071	S<117>	-4520	354	1121	S<67>	-5320	354	1171	S<17>	-6120	354
1072	S<116>	-4536	201	1122	S<66>	-5336	201	1172	S<16>	-6136	201
1073	S<115>	-4552	354	1123	S<65>	-5352	354	1173	S<15>	-6152	354
1074	S<114>	-4568	201	1124	S<64>	-5368	201	1174	S<14>	-6168	201
1075	S<113>	-4584	354	1125	S<63>	-5384	354	1175	S<13>	-6184	354
1076	S<112>	-4600	201	1126	S<62>	-5400	201	1176	S<12>	-6200	201
1077	S<111>	-4616	354	1127	S<61>	-5416	354	1177	S<11>	-6216	354
1078	S<110>	-4632	201	1128	S<60>	-5432	201	1178	S<10>	-6232	201
1079	S<109>	-4648	354	1129	S<59>	-5448	354	1179	S<9>	-6248	354
1080	S<108>	-4664	201	1130	S<58>	-5464	201	1180	S<8>	-6264	201
1081	S<107>	-4680	354	1131	S<57>	-5480	354	1181	S<7>	-6280	354
1082	S<106>	-4696	201	1132	S<56>	-5496	201	1182	S<6>	-6296	201
1083	S<105>	-4712	354	1133	S<55>	-5512	354	1183	S<5>	-6312	354
1084	S<104>	-4728	201	1134	S<54>	-5528	201	1184	S<4>	-6328	201
1085	S<103>	-4744	354	1135	S<53>	-5544	354	1185	S<3>	-6344	354
1086	S<102>	-4760	201	1136	S<52>	-5560	201	1186	S<2>	-6360	201
1087	S<101>	-4776	354	1137	S<51>	-5576	354	1187	S<1>	-6376	354
1088	S<100>	-4792	201	1138	S<50>	-5592	201	1188	DUMMY<29>	-6392	201
1089	S<99>	-4808	354	1139	S<49>	-5608	354	1189	DUMMY<30>	-6408	354
1090	S<98>	-4824	201	1140	S<48>	-5624	201	1190	DUMMY<31>	-6424	201
1091	S<97>	-4840	354	1141	S<47>	-5640	354	1191	DUMMY<32>	-6440	354
1092	S<96>	-4856	201	1142	S<46>	-5656	201	1192	DUMMY<33>	-6456	201
1093	S<95>	-4872	354	1143	S<45>	-5672	354	1193	DUMMY<34>	-6472	354
1094	S<94>	-4888	201	1144	S<44>	-5688	201	1194	DUMMY<35>	-6488	201
1095	S<93>	-4904	354	1145	S<43>	-5704	354	1195	DUMMY<36>	-6504	354
1096	S<92>	-4920	201	1146	S<42>	-5720	201	1196	G<319>	-6520	201
1097	S<91>	-4936	354	1147	S<41>	-5736	354	1197	G<317>	-6536	354
1098	S<90>	-4952	201	1148	S<40>	-5752	201	1198	G<315>	-6552	201
1099	S<89>	-4968	354	1149	S<39>	-5768	354	1199	G<313>	-6568	354
1100	S<88>	-4984	201	1150	S<38>	-5784	201	1200	G<311>	-6584	201

Table 66. Pad Center Coordinates

No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y	No.	PAD Name	Center-X	Center-Y
1201	G<309>	-6600	354	1251	G<209>	-7400	354	1301	G<109>	-8200	354
1202	G<307>	-6616	201	1252	G<207>	-7416	201	1302	G<107>	-8216	201
1203	G<305>	-6632	354	1253	G<205>	-7432	354	1303	G<105>	-8232	354
1204	G<303>	-6648	201	1254	G<203>	-7448	201	1304	G<103>	-8248	201
1205	G<301>	-6664	354	1255	G<201>	-7464	354	1305	G<101>	-8264	354
1206	G<299>	-6680	201	1256	G<199>	-7480	201	1306	G<99>	-8280	201
1207	G<297>	-6696	354	1257	G<197>	-7496	354	1307	G<97>	-8296	354
1208	G<295>	-6712	201	1258	G<195>	-7512	201	1308	G<95>	-8312	201
1209	G<293>	-6728	354	1259	G<193>	-7528	354	1309	G<93>	-8328	354
1210	G<291>	-6744	201	1260	G<191>	-7544	201	1310	G<91>	-8344	201
1211	G<289>	-6760	354	1261	G<189>	-7560	354	1311	G<89>	-8360	354
1212	G<287>	-6776	201	1262	G<187>	-7576	201	1312	G<87>	-8376	201
1213	G<285>	-6792	354	1263	G<185>	-7592	354	1313	G<85>	-8392	354
1214	G<283>	-6808	201	1264	G<183>	-7608	201	1314	G<83>	-8408	201
1215	G<281>	-6824	354	1265	G<181>	-7624	354	1315	G<81>	-8424	354
1216	G<279>	-6840	201	1266	G<179>	-7640	201	1316	G<79>	-8440	201
1217	G<277>	-6856	354	1267	G<177>	-7656	354	1317	G<77>	-8456	354
1218	G<275>	-6872	201	1268	G<175>	-7672	201	1318	G<75>	-8472	201
1219	G<273>	-6888	354	1269	G<173>	-7688	354	1319	G<73>	-8488	354
1220	G<271>	-6904	201	1270	G<171>	-7704	201	1320	G<71>	-8504	201
1221	G<269>	-6920	354	1271	G<169>	-7720	354	1321	G<69>	-8520	354
1222	G<267>	-6936	201	1272	G<167>	-7736	201	1322	G<67>	-8536	201
1223	G<265>	-6952	354	1273	G<165>	-7752	354	1323	G<65>	-8552	354
1224	G<263>	-6968	201	1274	G<163>	-7768	201	1324	G<63>	-8568	201
1225	G<261>	-6984	354	1275	G<161>	-7784	354	1325	G<61>	-8584	354
1226	G<259>	-7000	201	1276	G<159>	-7800	201	1326	G<59>	-8600	201
1227	G<257>	-7016	354	1277	G<157>	-7816	354	1327	G<57>	-8616	354
1228	G<255>	-7032	201	1278	G<155>	-7832	201	1328	G<55>	-8632	201
1229	G<253>	-7048	354	1279	G<153>	-7848	354	1329	G<53>	-8648	354
1230	G<251>	-7064	201	1280	G<151>	-7864	201	1330	G<51>	-8664	201
1231	G<249>	-7080	354	1281	G<149>	-7880	354	1331	G<49>	-8680	354
1232	G<247>	-7096	201	1282	G<147>	-7896	201	1332	G<47>	-8696	201
1233	G<245>	-7112	354	1283	G<145>	-7912	354	1333	G<45>	-8712	354
1234	G<243>	-7128	201	1284	G<143>	-7928	201	1334	G<43>	-8728	201
1235	G<241>	-7144	354	1285	G<141>	-7944	354	1335	G<41>	-8744	354
1236	G<239>	-7160	201	1286	G<139>	-7960	201	1336	G<39>	-8760	201
1237	G<237>	-7176	354	1287	G<137>	-7976	354	1337	G<37>	-8776	354
1238	G<235>	-7192	201	1288	G<135>	-7992	201	1338	G<35>	-8792	201
1239	G<233>	-7208	354	1289	G<133>	-8008	354	1339	G<33>	-8808	354
1240	G<231>	-7224	201	1290	G<131>	-8024	201	1340	G<31>	-8824	201
1241	G<229>	-7240	354	1291	G<129>	-8040	354	1341	G<29>	-8840	354
1242	G<227>	-7256	201	1292	G<127>	-8056	201	1342	G<27>	-8856	201
1243	G<225>	-7272	354	1293	G<125>	-8072	354	1343	G<25>	-8872	354
1244	G<223>	-7288	201	1294	G<123>	-8088	201	1344	G<23>	-8888	201
1245	G<221>	-7304	354	1295	G<121>	-8104	354	1345	G<21>	-8904	354
1246	G<219>	-7320	201	1296	G<119>	-8120	201	1346	G<19>	-8920	201
1247	G<217>	-7336	354	1297	G<117>	-8136	354	1347	G<17>	-8936	354
1248	G<215>	-7352	201	1298	G<115>	-8152	201	1348	G<15>	-8952	201
1249	G<213>	-7368	354	1299	G<113>	-8168	354	1349	G<13>	-8968	354
1250	G<211>	-7384	201	1300	G<111>	-8184	201	1350	G<11>	-8984	201

Table 67. Pad Center Coordinates

No.	PAD Name	Center-X	Center-Y
1351	G<9>	-9000	354
1352	G<7>	-9016	201
1353	G<5>	-9032	354
1354	G<3>	-9048	201
1355	G<1>	-9064	354
1356	DUMMY<37>	-9080	201
1357	DUMMY<38>	-9096	354
1358	DUMMY<39>	-9112	201
1359	DUMMY<40>	-9128	354

19.2. APPLICATION CIRCUIT

The following figure indicates a schematic diagram of application circuit for S6D0154.

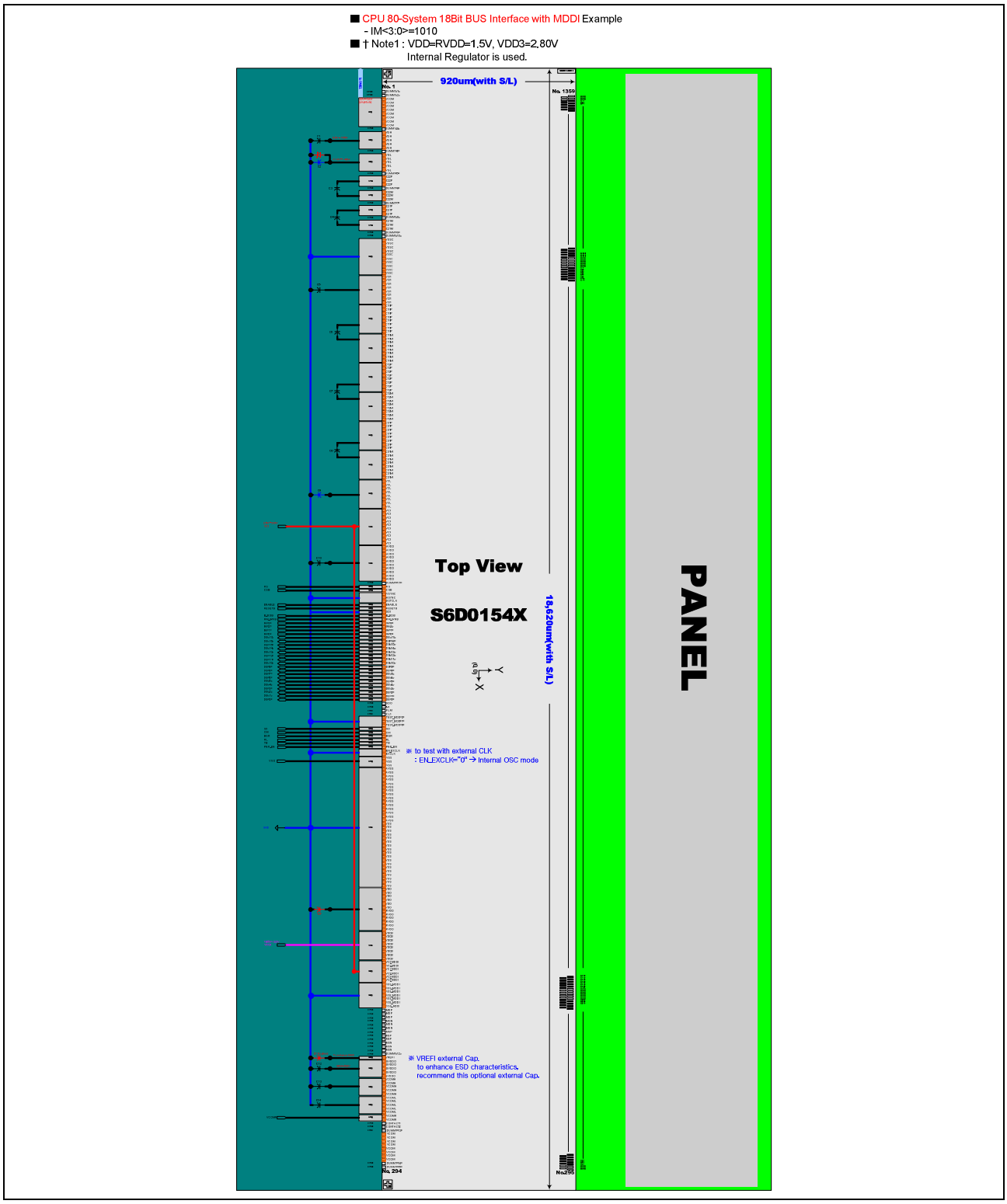


Figure 134. Application Circuit Example

Note. CSB and RW_WRB pads must be connected to VDD3 or VSS level when MDDI is used. But, it is recommended that connect to VDD3.

19.3. EXTERNAL COMPONENT

Table 68. External Component

Name	Device	Value	Connection	Note	
C1	Capacitor	1uF	VGH – GND	Maximum Ratings Voltage	18V
C2	Capacitor	1uF	VGL – GND		18V
C3	Capacitor	1uF	C22P – C22M		18V
C4	Capacitor	1uF	C21P – C21M		18V
C5	Capacitor	1uF	VCI1 – GND		3V
C6	Capacitor	1uF	C11P – C11M		6V
C7	Capacitor	1uF	C12P – C12M		6V
C8	Capacitor	1uF	C31P – C31M		6V
C9	Capacitor	1uF	VCL – GND		6V
C10	Capacitor	1uF	AVDD – GND		6V
C11	Capacitor	1uF	RVDD – GND		3V
C12	Capacitor	1uF	VREFI – GND		3V
C13	Capacitor	1uF	GVDDO – GND		6V
C14	Capacitor	1uF	VCOMH – GND		6V
C15	Capacitor	1uF	VCOML – GND		6V
D1	Diode	-	(+)VGL – GND(-)	VF ≤ 0.3V (@ IF = 20mA, Ta = 25°C) VR ≥ max.20V	