4.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
OBL = obligatory; connect as described in circuit diagram
DVSS: if not used, connect to DVSS
AHVSS: connect to AHVSS

4.2.1. MAP 440yA Pin List

Pin No. PMQFP 80-11	Pin No. PMQFP 80-1	Pin Name	Type	Connection (If not used)	Short Description
1	1	NC		LV	Not Connected
2	2	I2C_CL	IN/OUT	OBL	I^2C Clock
3	3	I2C_DA	IN/OUT	OBL	I^2C Data
4	4	I2S_CL	IN/OUT	LV	Sync. I^2S Clock
5	5	I2S_WS	IN/OUT	LV	Sync. I^2S Word Strobe
6	6	I2S_DA_OUT	OUT	LV	Sync. I^2S Data Output
7	7	I2S_DA_IN1	IN	LV	Sync. I^2S Data Input 1
8	8	I2S_DEL_IN	IN	LV	Sync. I^2S Input from Delay Line
9	9	I2S_DEL_OUT	OUT	LV	Sync. I^2S Output to External Delay Line
10	10	I2S_DEL_CL	OUT	LV	I^2S Clock Output for External Delay
11	11	I2S_DEL_WS	OUT	LV	I^2S Word Strobe Output for External Delay
12	12	DVSUP	IN	OBL	Digital Power Supply
13	13	DVSUP	IN	OBL	Digital Power Supply
14	14	DVSS		OBL	Digital Ground
15	15	DVSS		OBL	Digital Ground
16	–	DVSS		OBL	Digital Ground
17	16	I2S_DA_IN2	IN	LV	Sync. I^2S Data Input 2
18	22	NC		LV	Not Connected
19	17	I2S_CL3	IN/OUT	LV	Async. I^2S Clock Input / Sync. I^2S Clock Output
20	18	I2S_WS3	IN/OUT	LV	Async. I^2S Word Strobe Input / Sync. I^2S Word Strobe Output
21	19	RESETQ	IN	OBL	Power-On Reset (active low)
22	20	I2S_DA_IN3	IN	LV	Sync./Async. I^2S Data Input 3
23	21	I2S_DA_IN4	IN	LV	Sync. I^2S Data Input 4
24	23	DACA_R	OUT	LV	Aux Output, Right

Pin No. PMQFP 80-11	Pin No. PMQFP 80-1	Pin Name	Type	Connection (If not used)	Short Description
25	24	DACA_L	OUT	LV	Aux Output, Left
26	25	VREF2		OBL	Reference Ground 2
27	26	DACM_R	OUT	LV	Main Output, Right
28	27	DACM_L	OUT	LV	Main Output, Left
29	28	DACM_C	OUT	LV	Main Output, Center
30	29	DACM_SUB	OUT	LV	Main Output, Subwoofer
31	30	DACM_SR	OUT	LV	Surround Output, Right
32	31	DACM_SL	OUT	LV	Surround Output, Left
33	33	LINE_OUT2R	OUT	LV	Line 2 Output, Right
34	34	LINE_OUT2L	OUT	LV	Line 2 Output, Left
35	35	VREF1		OBL	Reference Ground 1
36	36	LINE_OUT1R	OUT	LV	Line 1 Output, Right
37	37	LINE_OUT2L	OUT	LV	Line 1 Output, Left
38	38	CAPL_A		OBL	Volume Capacitor Aux
39	39	AHVSUP	IN	OBL	Analog Power Supply +8 V
40	40	CAPL_M		OBL	Volume Capacitor Main
41	41	LINE_OUT3R	OUT	LV	Line 3 Output, Right
42	42	LINE_OUT3L	OUT	LV	Line 3 Output, Left
43	43	AHVSS		OBL	Analog Ground
44	44	AHVSS		OBL	Analog Ground
45	45	AGNDC		OBL	Analog Reference Voltage
46	46	NC		LV	Not Connected
47	48	LINE_IN4L	IN	LV	Line 4 Input, Left
48	49	LINE_IN4R	IN	LV	Line 4 Input, Right
49	–	ASG		AHVSS	Analog Shield Ground
50	50	LINE_IN3L	IN	LV	Line 3 Input, Left
51	51	LINE_IN3R	IN	LV	Line 3 Input, Right
52	–	ASG		AHVSS	Analog Shield Ground
53	52	LINE_IN2L	IN	LV	Line 2 Input, Left
54	53	LINE_IN2R	IN	LV	Line 2 Input, Right
55	–	ASG		AHVSS	Analog Shield Ground

Pin No. PMQFP 80-11	Pin No. PMQFP 80-1	Pin Name	Type	Connection (If not used)	Short Description
56	54	LINE_IN1L	IN	LV	Line 1 Input, Left
57	55	LINE_IN1R	IN	LV	Line 1 Input, Right
58	56	VREFTOP		OBL	Reference Voltage
59	57	LINE_IN5L	IN	LV	Line 5 Input, Left
60	58	LINE_IN5R	IN	LV	Line 5 Input, Right
61	59	AVSS		OBL	Analog Ground for IF Part
62	60	AVSS		OBL	Analog Ground for IF Part
63	47	NC		LV	Not Connected
64	32	NC		LV	Not Connected
65	61	AVSUP	IN	OBL	Analog Power Supply +5 V
66	62	AVSUP	IN	OBL	Analog Power Supply +5 V
67	63	NC		LV	Not Connected
68	64	NC		LV	Not Connected
69	65	NC		LV	Not Connected
70	66	TESTEN		AVSS	Test Pin (must be connected to ground)
71	67	XTAL_IN	IN	OBL/LV	Crystal Oscillator Input
72	68	XTAL_OUT	OUT	OBL	Crystal Oscillator Output
73	69	TP	IN	LV	Test Input
74	70	AUD_CL_OUT	OUT	LV	Audio Clock Output (18.432 MHz)
75	71-75	NC		LV	Not Connected
76	76	SPDIF_OUT	OUT	LV	S/PDIF Output
77	77	DCTRI/O_1	IN/OUT	LV	Digital Control Port 1
78	78	DCTRI/O_0	IN/OUT	LV	Digital Control Port 0
79	79	ADR_SEL	IN	OBL	I^2C Address Select
80	80	STANDBYQ	IN	OBL	Standby (active low)

4.2.2. MAP 440yA Pin Descriptions

NC – Pin not connected.

I2C_CL – I^2C Clock Input/Output (Fig. 4–14)
At this pin I^2C bus clock signal must be supplied. The signal can be pulled down by the MAP in case of wait conditions.

I2C_DA – I^2C Data Input/Output (Fig. 4–14)
At this pin the I^2C bus data is written to or read from the MAP.

I2S_CL – I^2S Clock Input/Output (Fig. 4–15)
Clock line for the synchronous I^2S bus. In master mode, this line is driven by the MAP; in slave mode, an external I^2S-Bus clock has to be supplied.

I2S_WS – I^2S Word Strobe Input/Output
(Fig. 4–15)
Word strobe line for the synchronous I^2S bus. In master mode, this line is driven by the MAP; in slave mode, an external I^2S word strobe has to be supplied.

I2S_DA_OUT – I^2S Data Output 1 (Fig. 4–19)
Output of digital serial sound data of the MAP on the synchronous I^2S bus.

I2S_DA_IN1 – I^2S Data Input 1 (Fig. 4–12)
First input of digital serial sound data to the MAP via the synchronous I^2S-Bus.

I2S_DA_IN2 – I^2S Data Input 2 (Fig. 4–12)
Second input of digital serial sound data to the MAP via the synchronous I^2S bus.

I2S_DA_IN3 – I^2S Data Input 3 (Fig. 4–12)
Input of digital serial sound data to the MAP via the asynchronous I^2S bus.

I2S_DA_IN4 – I^2S Data Input 4 (Fig. 4–12)
Input of digital serial sound data to the MAP via the asynchronous I^2S bus.

I2S_CL3 – I^2S Clock Input (Fig. 4–12)
Clock line for the asynchronous I^2S bus. In slave mode, an external I^2S bus clock has to be supplied.

I2S_WS3 – I2S Word Strobe Input (Fig. 4–12)
Word strobe line for the asynchronous I^2S bus. In slave mode, an external I^2S bus word strobe has to be supplied.

I2S_DEL_IN – 8-channel I^2S input interface from external audio delay (MAD) (Fig. 4–15)

I2S_DEL_OUT – 8-channel I^2S output interface to external audio delay (MAD) (Fig. 4–15)

I2S_DEL_CL – Clock output for I^2S interface to external delay line (MAD) (Fig. 4–19).

I2S_DEL_WS – Word strobe output for I^2S interface to external delay line (MAD) (Fig. 4–19).

DVSUP* – Digital Supply Voltage
Power supply for the digital circuitry of the MAP. Must be connected to a +5 V power supply.

DVSS* – Digital Ground
Ground connection for the digital circuitry of the MAP.

AHVSUP* – Analog Power Supply High Voltage
Power is supplied via this pin for the analog circuitry of the MAP (except IF input). This pin must be connected to the +8 V supply (+5 V-operation is possible with restrictions in performance).

AHVSS* – Analog Power Supply High Voltage Ground
Ground connection for the analog circuitry of the MAP (except IF input).

AVSUP* – Analog Power Supply Voltage
Power is supplied via this pin for the analog IF input circuitry of the MAP. This pin must be connected to the +5 V supply.

AVSS* – Analog Power Supply Voltage
Ground connection for the analog IF input circuitry of the MAP.

AGNDC – Internal Analog Reference Voltage
This pin serves as the internal ground connection for the analog circuitry (except IF input). It must be connected to the VREF pins with a 3.3 µF and a 100 nF capacitor in parallel. This pins shows a DC level of typically 3.73 V (with AHVSUP = 8 V).

VREF1 – Reference Ground 1
Reference analog ground. This pin must be connected separately to the ground (AHVSS). VREF1 serves as a clean ground and should be used as the reference for analog connections to the Line outputs.

VREF2 – Reference Ground 2
Reference analog ground. This pin must be connected separately to the ground (AHVSS). VREF2 serves as a clean ground and should be used as the reference for analog connections to the Main and Aux outputs.

VREFTOP – Reference Voltage
Via this pin, an internal reference voltage is decoupled. It must be connected to AVSS pins with a 10 µF and a 100 nF capacitor in parallel. Traces must be kept short.

TESTEN – Test Enable Pin (Fig. 4–10)
This pin enables factory test modes. For normal operation, it must be connected to ground.

TP – This pin enables factory test modes. For normal operation, it must be left vacant.

CAPLA – Volume Capacitor Aux (Fig. 4–20)
A 10-µF capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for Aux volume changes in order to suppress audible plops. The value of the capacitor can be lowered to 1-µF if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

CAPLM – Volume Capacitor Main (Fig. 4–20)
A 10-µF capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for Main volume changes in order to suppress audible plops. The value of the capacitor can be lowered to 1 µF if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

RESETQ – Reset Input (Fig. 4–9)
In the steady state, high level is required. If pulled down, the MAP 44xyA is reset.

STANDBYQ – Stand-by
In normal operation, this pin must be High. If the MAP is switched off by first pulling STANDBYQ low and then (after >1 µs delay) switching off the 5 V, but keeping the 8 V power supply (**'Stand-by' mode**), the Line switches maintain their position and function.

ADR_SEL – I^2C Bus Address Select (Fig. 4–13)
By means of this pin, one of three device addresses for the MAP can be selected. The pin can be connected to ground (I^2C device addresses $80/81_{hex}$), to +5 V supply ($84/85_{hex}$), or left open ($88/89_{hex}$).

D_CTR_I/O_1/0 – Digital Control Input/Output Pins (Fig. 4–15)
These pins serve as general purpose input/output pins. Pin D_CTR_I/O_1 can be used as an interrupt request pin to the controller.

XTAL_IN, XTAL_OUT – Crystal Input and Output Pins (Fig. 4–16)
These pins are connected to an 18.432 MHz crystal oscillator which is digitally tuned by integrated capacitances. An external clock can be fed into XTAL_OUT (leave XTAL_IN vacant in this case). The audio clock output signal AUD_CL_OUT is derived from the oscillator. External capacitors at each crystal pin to ground (AVSS) are required. It should be verified by layout, that no supply current for the digital circuitry is flowing through the ground connection point.

AUD_CL_OUT – Audio Clock Output (Fig. 4–16)
This is the 18.432 MHz main clock output.

LINE_IN1L/R – Line1 Inputs (Fig. 4–11)
The analog input signal for Line 1 is fed to this pin. Analog input connection must be AC-coupled.

LINE_IN2L/R – Line 2 Inputs (Fig. 4–11)
The analog input signal for Line 2 is fed to this pin. Analog input connection must be AC-coupled.

LINE_IN3L/R – Line3 Inputs (Fig. 4–11)
The analog input signal for Line 3 is fed to this pin. Analog input connection must be AC-coupled.

LINE_IN4L/R – Line 4 Inputs (Fig. 4–11)
The analog input signal for Line 4 is fed to this pin. Analog input connection must be AC-coupled.

LINE_IN5L/R – Line 5 Input (Fig. 4–11)
The analog input signal for Line 4 is fed to this pin. Analog input connection must be AC-coupled.

ASG* – Analog Shield Ground
Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between Line inputs.

LINE_OUT1R/L – Line 1 Outputs (Fig. 4–18)
Output of the Line 1 signal. Connections to these pins must use a 100-Ω series resistor and are intended to be AC-coupled.

LINE_OUT2R/L – Line 2 Outputs (Fig. 4–18)
Output of the Line 2 signal. Connections to these pins must use a 100 Ω series resistor and are intended to be AC-coupled.

LINE_OUT3R/L – Line 3 Outputs (Fig. 4–18)
Output of the Line 3 signal. Connections to these pins must use a 100 Ω series resistor and are intended to be AC-coupled.

DACM_R/L – Main Outputs (Fig. 4–17)
Output of the Main L/R signals. A 330 pF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected Main volume.

DACM_C – Center Output (Fig. 4–17, only available in MAP 44x2K)
Output of the Center signal. A 330 pF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected Main volume.

DACM_SUB – Subwoofer Output (Fig. 4–17)
Output of the Subwoofer signal. A 330 pF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected Main volume.

DACM_SR/SL – Surround Outputs (Fig. 4–17, only available in MAP 44x2K)
Output of the Surround signal. A 330 pF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected Main volume.

DACA_R/L – Aux Outputs (Fig. 4–17)
Output of the Aux signal. A 330 nF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected Aux volume.

SPDIF_OUT – S/PDIF Output.

4.2.3. MAP 460yA Pin List

NC = not connected; leave vacant
LV = if not used, leave vacant
OBL = obligatory; connect as described in circuit diagram
DVSS: if not used, connect to DVSS
AHVSS: connect to AHVSS
PWM_VSS = connect to PWM_VSS if not used

Pin No.			Pin Name	Type	Connection (If not used)	Short Description
PMQFP 100-1	PMQFP 80-11	PMQFP 80-1				
1	–	–	NC		LV	Not Connected
2	–	–	NC		LV	Not Connected
3	23	23	DACA_R	OUT	LV	Aux Output, Right
4	24	24	DACA_L	OUT	LV	Aux Output, Left
5	25	25	VREF2		AHVSS	Reference Ground 2
6	26	26	PWM_BM	OUT	LV	PWM– Output, Subwoofer
7	27	27	PWM_BP	OUT	LV	PWM+ Output, Subwoofer
8	–	–	PWM_CM	OUT	LV	PWM– Output, Center
9	–	–	PWM_CP	OUT	LV	PWM+ Output, Center
10	–	–	PWM_SRM	OUT	LV	PWM– Output, Surround Right
11	–	–	PWM_SRP	OUT	LV	PWM+ Output, Surround Right
12	28	28	PWM_VDD	IN	OBL	PWM VDD
13	29	29	PWM_VSS		OBL	PWM VSS
14	30	30	PWM_RM	OUT	LV	PWM– Output, Right
15	31	31	PWM_RP	OUT	LV	PWM+ Output, Right
16	–	–	PWM_SLM	OUT	OBL	PWM– Output, Surround Left
17	–	–	PWM_SLP	OUT	OBL	PWM+ Output, Surround Left
18	32	32	PWM_LM	OUT	LV	PWM– Output, Left
19	33	33	PWM_LP	OUT	LV	PWM+ Output, Left
20	–	–	NC		NC	Not Connected
21	34	34	LINE_OUT2R	OUT	LV	Line 2 output, Right
22	35	35	LINE_OUT2L	OUT	LV	Line 2 output, Left
23	36	36	VREF1		OBL	Reference Ground 1
24	37	37	LINE_OUT1R	OUT	LV	Line 1 Output, Right
25	38	38	LINE_OUT1_L	OUT	LV	Line 1 Output, Left
26	39	39	CAPL_A		OBL	Volume Capacitor Aux

Pin No.			Pin Name	Type	Connection (If not used)	Short Description
PMQFP 100-1	PMQFP 80-11	PMQFP 80-1				
27	40	40	AHVSUP		OBL	Analog Power Supply +8 V
28	–	–	CAPL_M		OBL	Volume Capacitor Speaker
29	–	–	NC		LV	Not Connected
30	41	41	LINE_OUT3R	OUT	LV	Line 3 Output, Right
31	42	42	LINE_OUT3L	OUT	LV	Line 3 Output, left
32	43/ 44	43/ 44	AHVSS		OBL	Analog Ground
33	46	46/ 47	NC		LV	Not Connected
34	45	45	AGNDC		OBL	Analog Reference Voltage
35	47	48	LINE_IN4L	IN	LV	Line 4 Input, Left
36	48	49	LINE_IN4R	IN	LV	Line 4 Input, Right
37	49	–	ASG		AHVSS	Analog Shield Ground
38	50	50	LINE_IN3L	IN	LV	Line 3 Input, Left
39	51	51	LINE_IN3R	IN	LV	Line 3 Input, Right
40	52	–	ASG		AHVSS	Analog Shield Ground
41	53	52	LINE_IN2L	IN	LV	Line 2 Input, Left
42	54	53	LINE_IN2R	IN	LV	Line 2 Input, Right
43	55	–	ASG		AHVSS	Analog Shield Ground
44	56	54	LINE_IN1L	IN	LV	Line 1 Input, Left
45	57	55	LINE_IN1R	IN	LV	Line 1 Input, Right
46	58	56	VREFTOP		OBL	Reference Voltage
47	59	57	LINE_IN5L	IN	LV	Line Input 5, Left
48	60	58	LINE_IN5R	IN	LV	Line Input 5, Right
49	63	–	NC		LV	Not Connected
50	–	–	NC		LV	Not Connected
51	61	59	AVSS		OBL	Analog Ground, IF-part
52	62	60	AVSS		OBL	Analog Ground, IF-part
53	64	61	AVSUP		OBL	Analog Power Supply +5 V
54	65	62	AVSUP		OBL	Analog Power Supply +5 V
55	66	63	NC		LV	Not Connected
56	67	64	NC		LV	Not Connected

Pin No. PMQFP 100-1	Pin No. PMQFP 80-11	Pin No. PMQFP 80-1	Pin Name	Type	Connection (If not used)	Short Description
57	68	65	NC		LV	Not Connected
58	69	66	TESTEN		AVSS	Test Pin (must be connected to ground)
59	–	–	NC		LV	Not Connected
60	70	67	XTAL_IN		OBL	Crystal Oscillator
61	71	68	XTAL_OUT		OBL / LV	Crystal Oscillator
62	–	–	NC		LV	Not Connected
63	72	69	TP		LV	Test Pin
64	–	–	NC		LV	Not Connected
65	73	70	AUD_CL_OUT	OUT	LV	Audio Clock Output (18.432 MHz)
66	–	71-73	NC		LV	Not Connected
67	–	–	NC		LV	Not Connected
68	74	74	VALID_B	OUT	LV	PA Mute Signal, Subwoofer
69	–	–	VALID_C	OUT	LV	PA Mute Signal, Center
70	–	–	VALID_SR	OUT	LV	PA Mute Signal, Surround Right
71	–	–	VALID_SL	OUT	LV	PA Mute Signal, Surround Left
72	75	75	VALID_LR	OUT	LV	PA Mute Signal, Left+Right
73	76	76	SPDIF_OUT	OUT	LV	S/PDIF Output
74	77	77	DCTRI/O_1	IN/OUT	LV	Digital Control Port 1
75	78	78	DCTRI/O_0	IN/OUT	LV	Digital Control Port 0
76	79	79	ADR_SEL	IN	OBL	I^2C Bus Address Select
77	80	80	STANDBYQ	IN	OBL	Standby (active low)
78	1	1	SHUTDOWNQ	IN	OBL	PA Error Feedback Signal
79	2	2	I2C_CL	IN/OUT	OBL	I^2C Clock
80	3	3	I2C_DA	IN/OUT	OBL	I^2C Data
81	4	4	I2S_CL	IN/OUT	LV	Sync. I^2S Clock
82	5	5	I2S_WS	IN/OUT	LV	Sync. I^2S Word Strobe
83	6	6	I2S_DA_OUT	OUT	LV	Sync. I^2S Data Output
84	7	7	I2S_DA_IN1	IN	LV	Sync. I^2S Data Input 1
85	8	8	I2S_DEL_IN	IN	LV	Sync. I^2S Input from External Delay Line
86	9	9	I2S_DEL_OUT	OUT	LV	Sync. I^2S Output to External Delay Line
87	10	10	I2S_DEL_CL	OUT	LV	I^2S Clock Output for External Delay

Pin No.			Pin Name	Type	Connection (If not used)	Short Description
PMQFP 100-1	PMQFP 80-11	PMQFP 80-1				
88	11	11	I2S_DEL_WS	OUT	LV	Sync. I^2S Word Strobe to External Delay Line
89	12	12	DVSUP		OBL	Digital Power Supply
90	13	13	DVSUP		OBL	Digital Power Supply
91	14	14	DVSS		OBL	Digital Ground
92	15	15	DVSS		OBL	Digital Ground
93	16	–	DVSS		OBL	Digital Ground
94	–	–	NC		LV	Not Connected
95	17	16	I2S_DA_IN2	IN	LV	Sync. I^2S Data Input 2
96	18	17	I2S_CL3	IN/OUT	LV	Async. I^2S Clock Input / Sync. I^2S Clock Output
97	19	18	I2S_WS3	IN/OUT	LV	Async. I^2S Word Strobe Input / Sync. I^2S Word Strobe Output
98	20	19	RESETQ	IN	OBL	Power-On Reset (active low)
99	21	20	I2S_DA_IN3	IN	LV	Sync. I^2S Data Input 3
100	22	21	I2S_DA_IN4	IN	LV	Sync. I^2S Data Input 4

4.2.4. MAP 460yA Pin Descriptions

NC – Pin not connected.

I2C_CL – I²C Clock Input/Output (Fig. 4–14)
At this pin I²C bus clock signal must be supplied. The signal can be pulled down by the MAP in case of wait conditions.

I2C_DA – I²C Data Input/Output (Fig. 4–14)
At this pin the I²C bus data is written to or read from the MAP.

I2S_CL – I²S Clock Input/Output (Fig. 4–15)
Clock line for the synchronous I²S bus. In master mode, this line is driven by the MAP; in slave mode, an external I²S-Bus clock has to be supplied.

I2S_WS – I²S Word Strobe Input/Output
(Fig. 4–15)
Word strobe line for the synchronous I²S bus. In master mode, this line is driven by the MAP; in slave mode, an external I²S word strobe has to be supplied.

I2S_DA_OUT – I²S Data Output 1 (Fig. 4–19)
Output of digital serial sound data of the MAP on the synchronous I²S bus.

I2S_DA_IN1 – I²S Data Input 1 (Fig. 4–12)
First input of digital serial sound data to the MAP via the synchronous I²S-Bus.

I2S_DA_IN2 – I²S Data Input 2 (Fig. 4–12)
Second input of digital serial sound data to the MAP via the synchronous I²S bus.

I2S_DA_IN3 – I²S Data Input 3 (Fig. 4–12)
Input of digital serial sound data to the MAP via the asynchronous I²S bus.

I2S_DA_IN4 – I²S Data Input 4 (Fig. 4–12)
Input of digital serial sound data to the MAP via the asynchronous I²S bus.

I2S_CL3 – I²S Clock Input (Fig. 4–12)
Clock line for the asynchronous I²S bus. In slave mode, an external I²S bus clock has to be supplied.

I2S_WS3 – I2S Word Strobe Input (Fig. 4–12)
Word strobe line for the asynchronous I²S bus. In slave mode, an external I²S bus word strobe has to be supplied.

I2S_DEL_IN – 8-channel I²S input interface from external audio delay (MAD) (Fig. 4–15)

I2S_DEL_OUT – 8-channel I²S output interface to external audio delay (MAD) (Fig. 4–15)

I2S_DEL_CL – Clock output for I²S interface to external delay line (MAD) (Fig. 4–19).

I2S_DEL_WS – Word strobe output for I²S interface to external delay line (MAD) (Fig. 4–19).

DVSUP* – Digital Supply Voltage
Power supply for the digital circuitry of the MAP. Must be connected to a +5 V power supply.

DVSS* – Digital Ground
Ground connection for the digital circuitry of the MAP.

AHVSUP* – Analog Power Supply High Voltage
Power is supplied via this pin for the analog circuitry of the MAP (except IF input). This pin must be connected to the +8 V supply (+5 V-operation is possible with restrictions in performance).

AHVSS* – Analog Power Supply High Voltage Ground
Ground connection for the analog circuitry of the MAP (except IF input).

AVSUP* – Analog Power Supply Voltage
Power is supplied via this pin for the analog IF input circuitry of the MAP. This pin must be connected to the +5 V supply.

AVSS* – Analog Power Supply Voltage
Ground connection for the analog IF input circuitry of the MAP.

AGNDC – Internal Analog Reference Voltage
This pin serves as the internal ground connection for the analog circuitry (except IF input). It must be connected to the VREF pins with a 3.3 µF and a 100 nF capacitor in parallel. This pins shows a DC level of typically 3.73 V (with AHVSUP = 8 V).

VREF1 – Reference Ground 1
Reference analog ground. This pin must be connected separately to the ground (AHVSS). VREF1 serves as a clean ground and should be used as the reference for analog connections to the Line outputs.

VREF2 – Reference Ground 2
Reference analog ground. This pin must be connected separately to the ground (AHVSS). VREF2 serves as a clean ground and should be used as the reference for analog connections to the Main and Aux outputs.

VREFTOP – Reference Voltage
Via this pin, an internal reference voltage is decoupled. It must be connected to AVSS pins with a 10 µF and a 100 nF capacitor in parallel. Traces must be kept short.

PWM_VDD – PWM Supply
Supply for PWM circuitry of the MAP. Must be connected to a 3.3 V supply.

PWM_VSS – PWM Ground
Ground connection for PWM circuitry of the MAP. Connect to common Ground with external PA.

TESTEN – Test Enable Pin (Fig. 4–10)
This pin enables factory test modes. For normal operation, it must be connected to ground.

TP – This pin enables factory test modes. For normal operation, it must be left vacant.

CAPLA – Volume Capacitor Aux (Fig. 4–20)
A 10 µF capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for Aux volume changes in order to suppress audible plops. The value of the capacitor can be lowered to 1 µF if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

RESETQ – Reset Input (Fig. 4–9)
In the steady state, high level is required. If pulled down, the MAP 46xyA is reset.

STANDBYQ – Stand-by
In normal operation, this pin must be High. If the MAP is switched off by first pulling STANDBYQ low and then (after >1 µs delay) switching off the 5 V, but keeping the 8-V power supply (**'Stand-by' mode**), the Line switches maintain their position and function.

ADR_SEL – I^2C Bus Address Select (Fig. 4–13)
By means of this pin, one of three device addresses for the MAP can be selected. The pin can be connected to ground (I^2C device addresses $80/81_{hex}$), to +5 V supply ($84/85_{hex}$), or left open ($88/89_{hex}$).

D_CTR_I/O_1/0 – Digital Control Input/Output Pins (Fig. 4–15)
These pins serve as general purpose input/output pins. Pin D_CTR_I/O_1 can be used as an interrupt request pin to the controller.

XTAL_IN, XTAL_OUT – Crystal Input and Output Pins (Fig. 4–16)
These pins are connected to an 18.432 MHz crystal oscillator which is digitally tuned by integrated capacitances. An external clock can be fed into XTAL_IN (leave XTAL_OUT vacant in this case). The audio clock output signal AUD_CL_OUT is derived from the oscillator. External capacitors at each crystal pin to ground (AVSS) are required. It should be verified by layout, that no supply current for the digital circuitry is flowing through the ground connection point.

AUD_CL_OUT – Audio Clock Output (Fig. 4–16)
This is the 18.432 MHz main clock output.

LINE_IN1L/R – Line 1 Inputs (Fig. 4–11)
The analog input signal for Line 1 is fed to this pin. Analog input connection must be AC-coupled.

LINE_IN2L/R – Line 2 Inputs (Fig. 4–11)
The analog input signal for Line 2 is fed to this pin. Analog input connection must be AC-coupled.

LINE_IN3L/R – Line 3 Inputs (Fig. 4–11)
The analog input signal for Line 3 is fed to this pin. Analog input connection must be AC-coupled.

LINE_IN4L/R – Line 4 Inputs (Fig. 4–11)
The analog input signal for Line 4 is fed to this pin. Analog input connection must be AC-coupled.

LINE_IN5L/R – Line 5Inputs (Fig. 4–11)
The analog input signal for Line 5is fed to this pin. Analog input connection must be AC-coupled.

ASG* – Analog Shield Ground
Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between Line inputs.

LINE_OUT_R/L – Line 1 Outputs (Fig. 4–18)
Output of the Line 1 signal. Connections to these pins must use a 100-Ω series resistor and are intended to be AC-coupled.

LINE_OUT_R/L – Line 2 Outputs (Fig. 4–18)
Output of the Line 2 signal. Connections to these pins must use a 100 Ω series resistor and are intended to be AC-coupled.

LINE_OUT_R/L – Line 3 Outputs (Fig. 4–18)
Output of the Line 3 signal. Connections to these pins must use a 100 Ω series resistor and are intended to be AC-coupled.

PWM_BM/P* – PWM outputs for subwoofer (Fig. 4–22)
Differential signal to directly drive a switching PA circuit (H-BRIDGE).

PWM_CM/P* – PWM outputs for center channel (Fig. 4–22, only available in MAP 4602K)
Differential signal to directly drive a switching PA circuit (H-BRIDGE).

PWM_SRM/P* – PWM outputs for surround right channel (Fig. 4–22, only available in MAP 4602K)
Differential signal to directly drive a switching PA circuit (H-BRIDGE).

PWM_VDD – PWM Supply
Supply for PWM circuitry of the MAP. Must be connected to a 3.3 V supply.

PWM_VSS – PWM Ground
Ground connection for PWM circuitry of the MAP. Connect to common Ground with external PA.

PWM_RM/P* – PWM outputs for right channel (Fig. 4–22)
Differential signal to directly drive a switching PA circuit (H-BRIDGE).

PWM_SLM/P* – PWM outputs for surround left channel (Fig. 4–22, only available in MAP 4602K)
Differential signal to directly drive a switching PA circuit (H-BRIDGE).

PWM_LM/P* – PWM outputs for left channel (Fig. 4–22)
Differential signal to directly drive a switching PA circuit (H-BRIDGE).

VALID_B – PA Mute Signal, Subwoofer (Fig. 4–23)
This pin is the PA mute control pin for the subwoofer. It is to be connected to a MUTE or RESET input of a switching PA circuit (H-BRIDGE).

VALID_C – PA Mute Signal, Center (Fig. 4–23)
This pin is the PA mute control pin for the center channel. It is to be connected to a MUTE or RESET input of a switching PA circuit (H-BRIDGE).

VALID_SR – PA Mute Signal, Surround Right (Fig. 4–23)
This pin is the PA mute control pin for the surround right channel. It is to be connected to a MUTE or RESET input of a switching PA circuit (H-BRIDGE).

VALID_SL – PA Mute Signal, Surround Left (Fig. 4–23)
This pin is the PA mute control pin for the surround left channel. It is to be connected to a MUTE or RESET input of a switching PA circuit (H-BRIDGE).

VALID_LR – PA Mute Signal, Left+Right (Fig. 4–23)
This pin is the PA mute control pin for the left and right channel. It is to be connected to a MUTE or RESET input of a switching PA circuit (H-BRIDGE).

SHUTDOWNQ – PA Error Feedback Input
Detects a single error signal from external switching PA's, e.g., in case of overtemperature. If low for at least 3 consecutive clock cycles, all VALID_x pins are forced to low. To connect multiple PA's all error signals must be combined with an OR circuit.

DACA_R/L – Aux Outputs (Fig. 4–17)
Output of the Aux signal. A 1 nF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected Aux volume.

SPDIF_OUT – S/PDIF Output.

*** Application Note:**
All ground pins should be connected to one low-resistive ground plane.

All supply pins should be connected separately with short and low-resistive lines to the power supply.

Decoupling capacitors from DVSUP to DVSS, AVSUP to AVSS, PWM_VDD to PWM_VSS and AHVSUP to AHVSS are recommended to be placed as close as possible to these pins. The decoupling of DVSUP and DVSS is the most important. The use of multiple capacitors in parallel is recommended. By carefully selecting different values, the frequency range of the decoupling can be extended and decoupling resonances can be avoided. Micronas reference applications use 220 pF, 470 pF, 1.5 nF, and 10 µF with the lowest value placed nearest to the pins.

The ASG pins should be connected as close as possible to the MAP ground. They are intended as ground connection for the shield of the Line signals and must not be connected to ground at the Line-connector.

Note: All PWM output pins do not have a short circuit protection. For optimal audio performance the PCB signal tracks from these outputs to the inputs of the according power stage should be kept to a minimum, not to exceed an equivalent of 70 mm of a 100 Ω transmission line. This reduces capacitive loading which is necessary to maintain the fast rise and fall times of the pulse modulated signals.

4.3. Pin Configurations

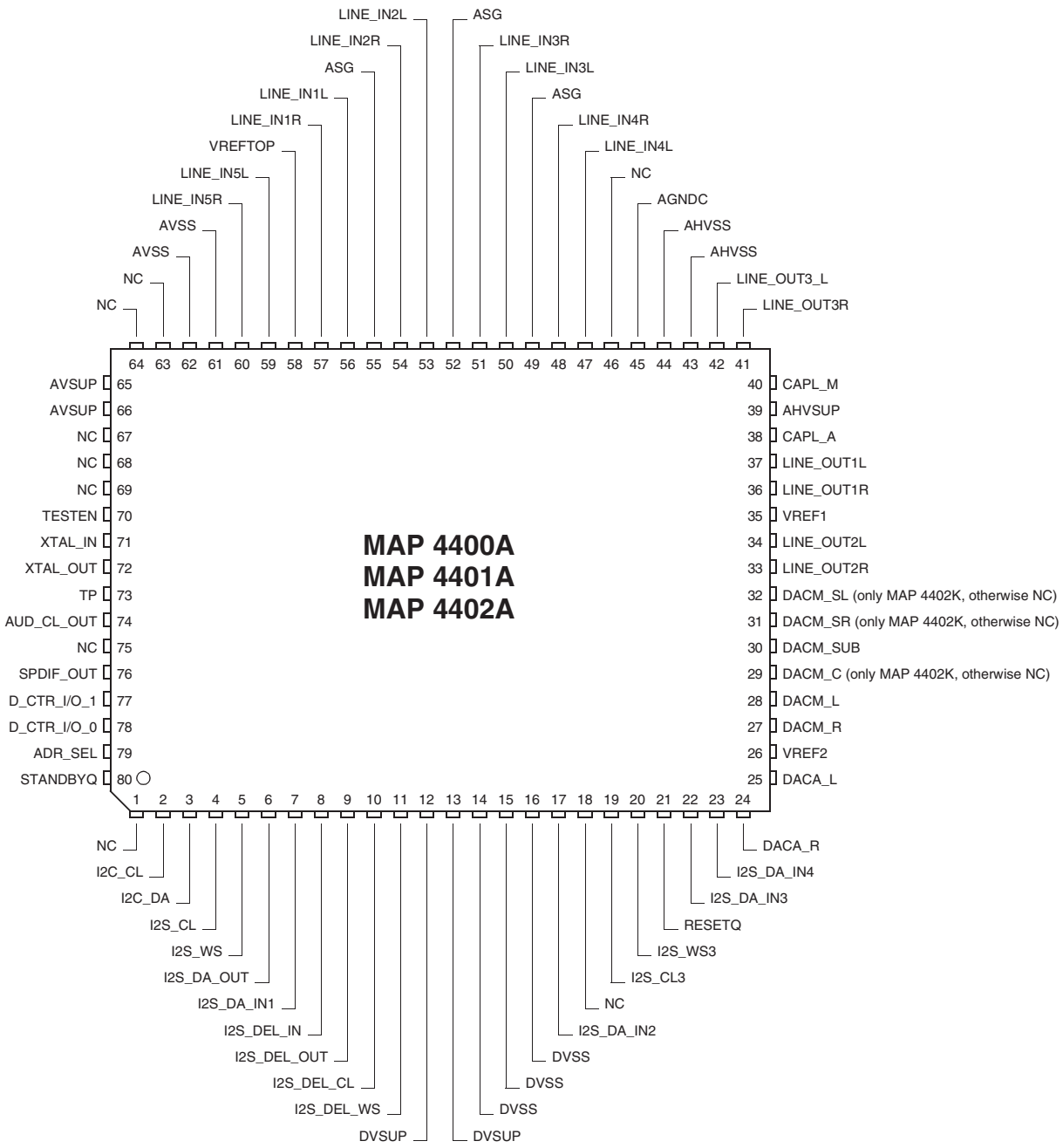

Fig. 4–4: MAP 440yA in PMQFP80-11 package

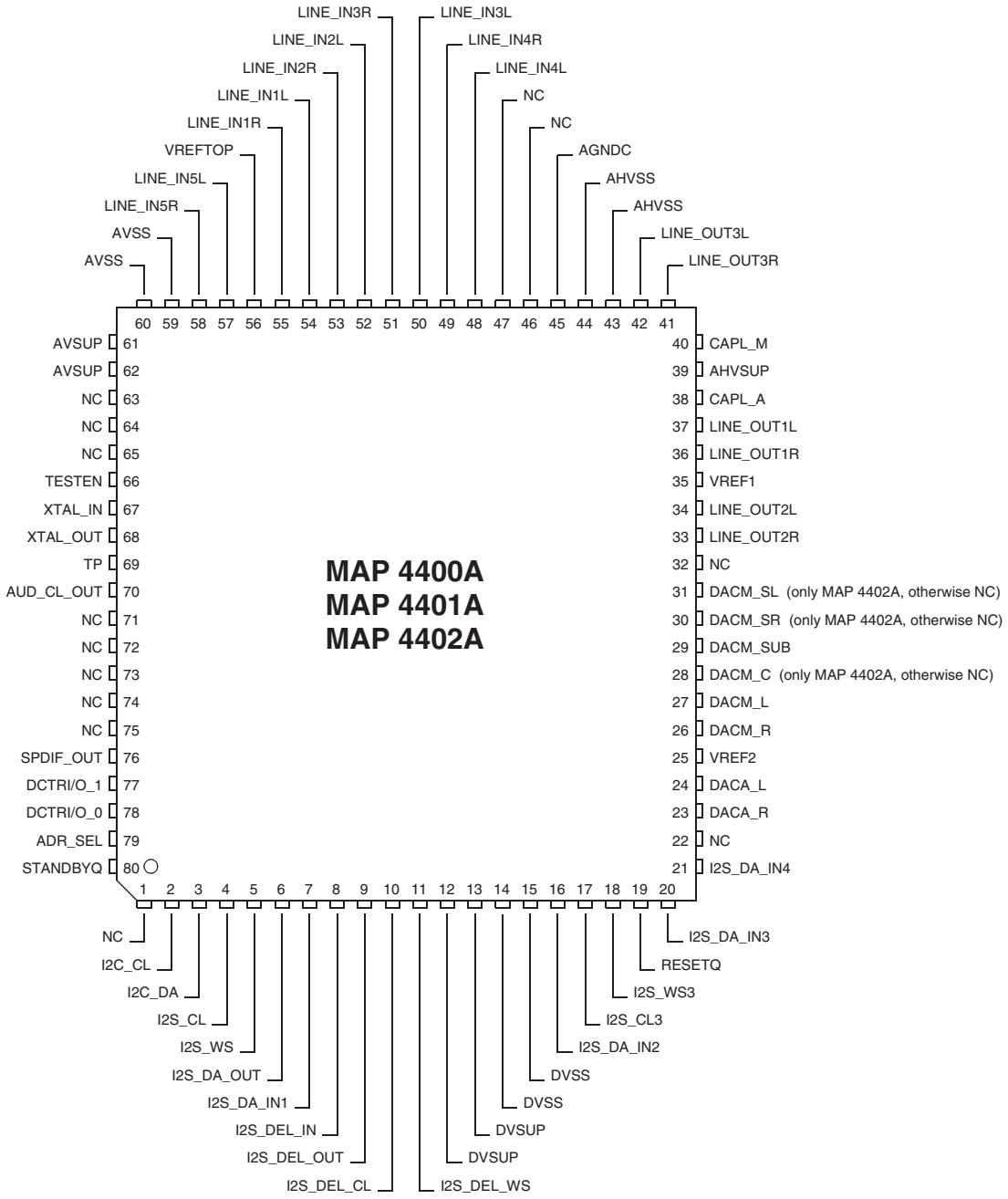

Fig. 4–5: MAP 440yA in PMQFP80-1 package

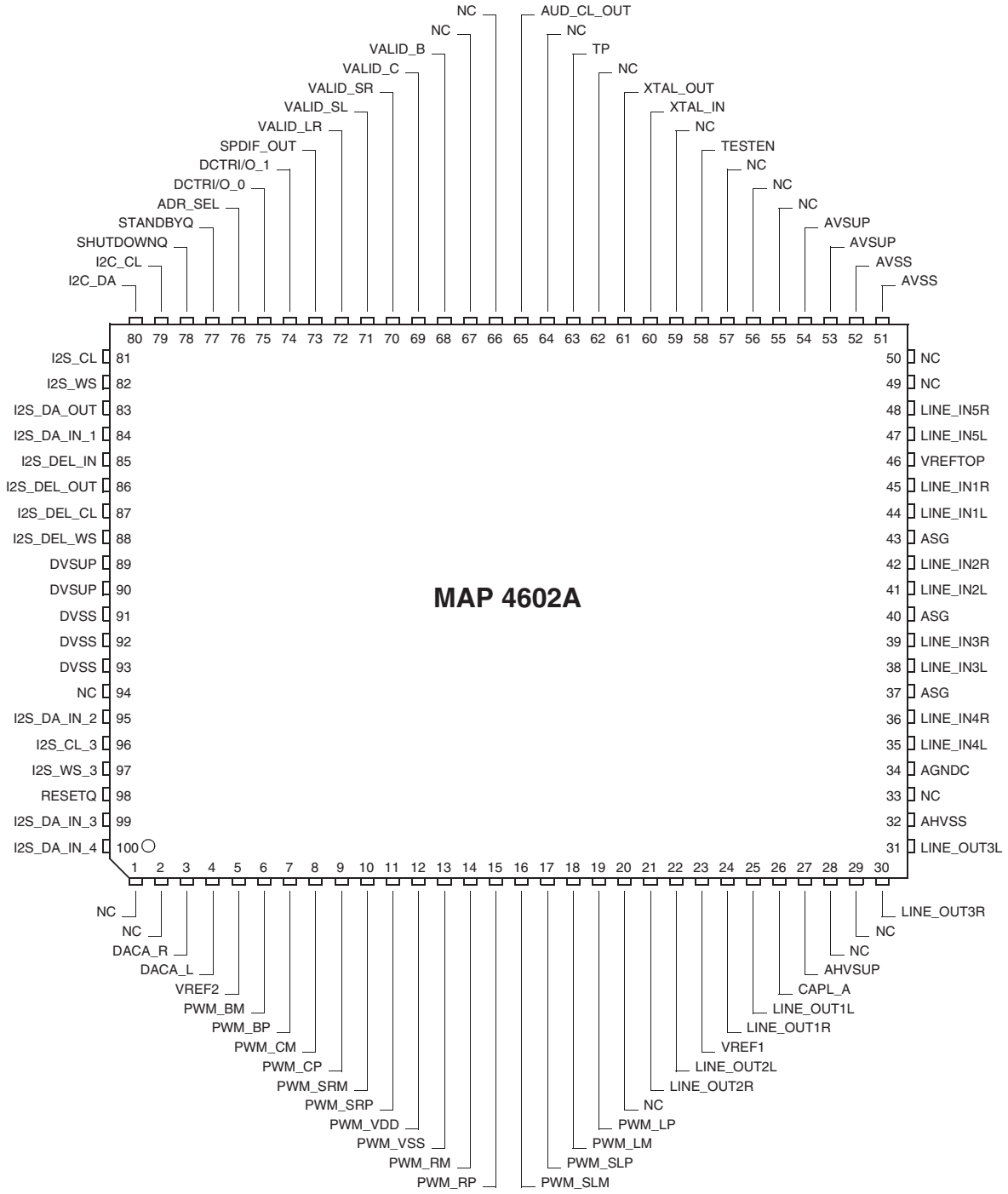

Fig. 4–6: MAP 4602A in PMQFP100-1 package

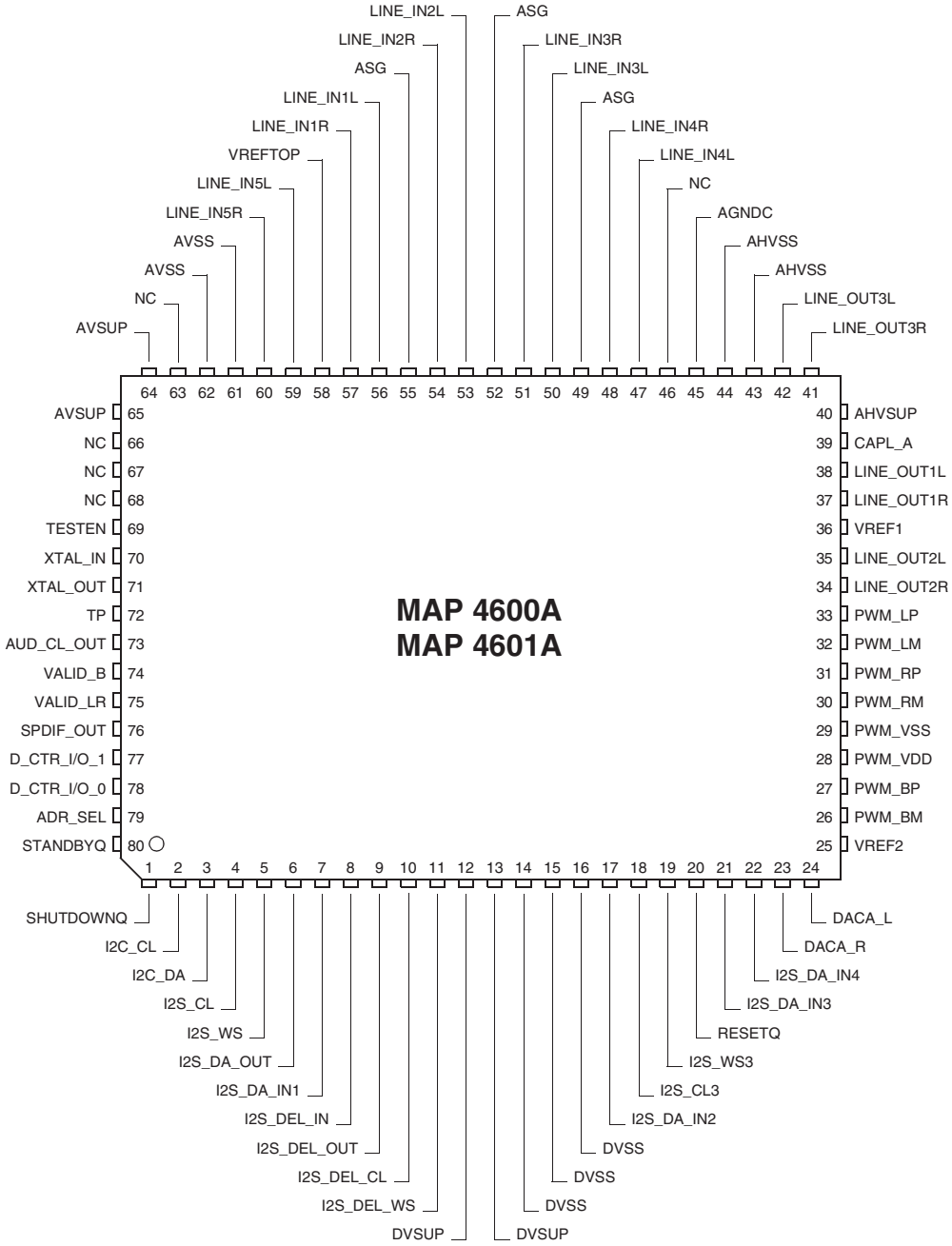

Fig. 4–7: MAP 460yA in PMQFP80-11 package

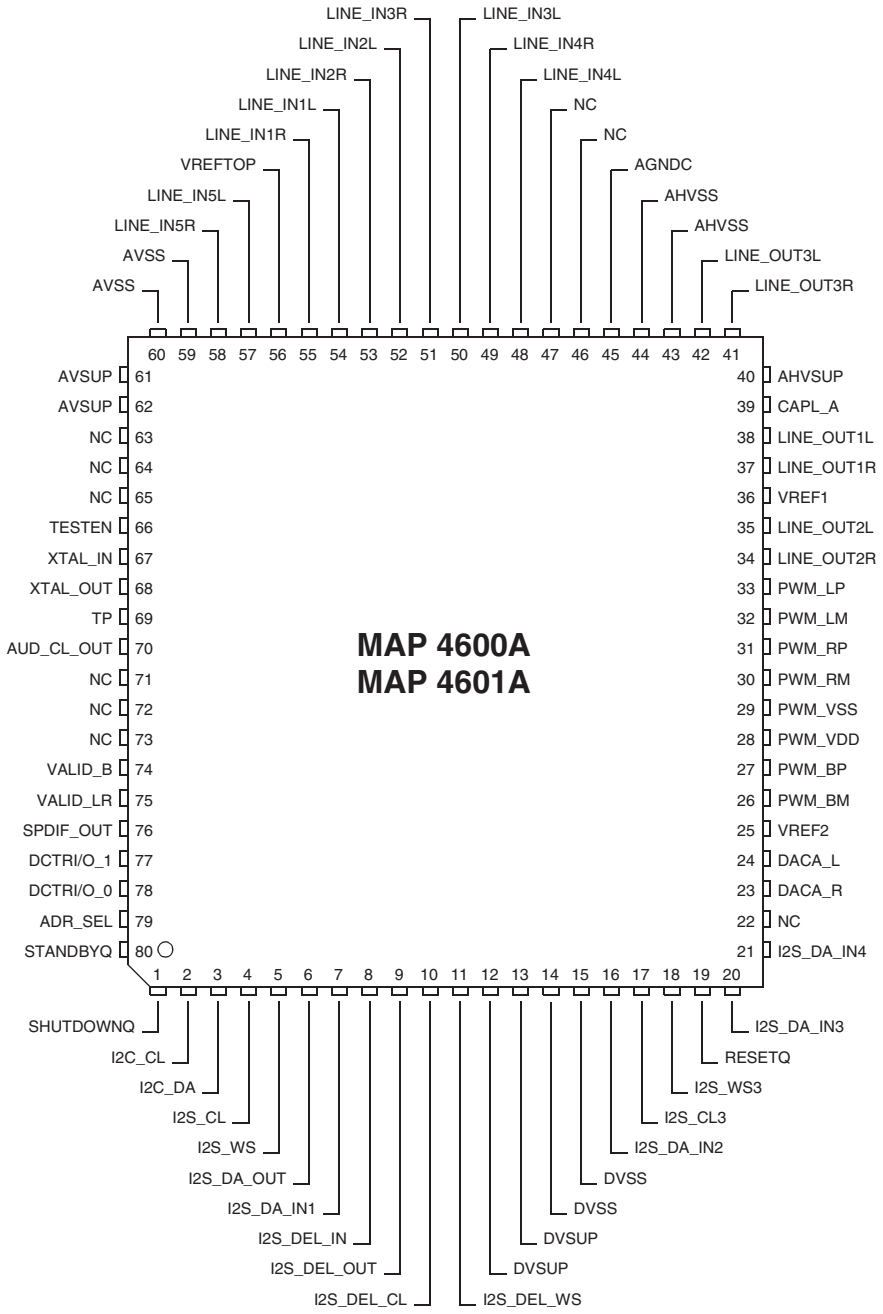

Fig. 4–8: MAP 460yA in PMQFP80-1 package