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S1D13506 Color LCD/CRT/TV Controller

Hardware Functional Specification

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Table of Contents

1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13506 Color LCD/CRT/TV Controller. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This specification will be updated as appropriate. Please check the Epson Research and Development Website at http://www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

1.2 Overview Description

The S1D13506 is a color LCD/CRT/TV graphics controller interfacing to a wide range of CPUs and display devices. The S1D13506 architecture is designed to meet the low cost, low power requirements of the embedded markets, such as Mobile Communications, Hand-Held PC's, and Office Automation.

The S1D13506 supports multiple CPUs, all LCD panel types, CRT, TV, and additionally provides a number of differentiating features. Products requiring digital camera input can take advantage of the directly supported WINNOV VideumCam™ digital interface. The EPSON Independent Simultaneous Display (EISD) capability allows the user to configure two different images on two different displays, while the SviwelView™, Hardware Cursor, Ink Layer, and BitBLT engine offer substantial performance benefits. These features, combined with the S1D13506's Operating System independence, make it an ideal display solution for a wide variety of applications.

2 Features

2.1 Memory Interface

- 16-bit DRAM interface:
  - EDO-DRAM up to 40MHz data rate (80M Bytes/s).
  - FPM-DRAM up to 25MHz data rate (50M Bytes/s).
- Memory size options:
  - 512K bytes using one 256K×16 device.
  - 2M bytes using one 1M×16 device.
- A configuration register can be programmed to enhance performance by tailoring the memory control output timing to the DRAM device.
- The complete 2M byte display buffer address space is directly and contiguously available through the 21-bit address bus.

2.2 CPU Interface

- Supports the following interfaces:
  - Epson E0C33 (16-bit interface to 32-bit microprocessor).
  - Hitachi SH-4 bus interface.
  - Hitachi SH-3 bus interface.
  - MIPS/ISA.
  - Motorola MC68000 (16-bit interface to 16/32-bit microprocessor/microcontroller).
  - Motorola MC68030 (16-bit interface to 16/32-bit microprocessor/microcontroller).
  - Motorola PowerPC MPC82x (16-bit interface to 32-bit microprocessor).
  - MPU bus interface with programmable READY.
  - NEC MIPS VR41xx.
  - PC Card (PCMCIA).
  - Philips MIPS PR31500/31700.
  - Toshiba MIPS TX39xx.
  - StrongARM (PC Card).
- One-stage write buffer for minimum wait-state CPU writes.
- Registers are memory-mapped – the M/R# pin selects between display buffer and register address space.

2.3 Display Support

- 4/8-bit monochrome or 4/8/16-bit color LCD interface for single-panel, single-drive displays.
- 8-bit monochrome or 8/16-bit color LCD interface for dual-panel, dual-drive displays.
- Direct support for 9/12-bit TFT/D-TFD, 18-bit TFT/D-TFD is supported up to 64K colors.
- Direct support for CRT up to 64K colors using Embedded RAMDAC.
- Direct support for NTSC/PAL TV output using Embedded RAMDAC.

2.4 Display Modes

- 4/8/15/16 bit-per-pixel (bpp) color depths.
- Up to 64 shades of gray on monochrome passive LCD panels using Frame Rate Modulation (FRM) and Dithering.
- Up to 32K/64K colors in 15/16 bpp modes on color passive LCD panels using dithering.
- Up to 64K colors on TFT/D-TFD, CRT and TV.
- 4/8 bit-per-pixel color depths are mapped using three 256x4 Look-Up Tables (LUT) allowing 16/256 out of a possible 4096 colors.
- Separate LUTs for LCD and CRT/TV.
- 15/16 bit-per-pixel color depths are mapped directly, bypassing the LUT.
- Example Resolutions:
  320 x 240 at a color depth of 16 bpp.
  640 x 240 at a color depth of 16 bpp.
  640 x 480 at a color depth of 16 bpp.
  800 x 600 at a color depth of 16 bpp.

2.5 Display Features

- SwivelView™: 90°, 180°, 270° hardware rotation of display image.
- EPSON Independent Simultaneous Display (EISD): displays independent images on different displays (CRT or TV and passive or TFT/D-TFD panel).
- Virtual Display Support: displays images larger than the panel size through the use of panning and scrolling.
- Hardware Cursor/Ink Layer: separate 64x64x2 hardware cursor or 2-bit ink layer for both LCD and CRT/TV.
- Double Buffering/Multi-pages: for smooth animation and instantaneous screen update.

2.6 Clock Source

- Memory clock can be derived from CLKI or BUSCLK pin. It can be internally divided by 2.
- Pixel clock can be derived from CLKI, CLKI2, or BUSCLK pin. It can be internally divided by 2, 3 or 4.
- Bus clock can be BUSCLK or (BUSCLK)/2, i.e. a 2x clock may be used.

2.7 Acceleration

- 2D Engine including the following 2 ROP BitBLTs:
  Write BLT.
  Move BLT.
  Solid Fill.
  Pattern Fill.
  Transparent Write BLT.
  Transparent Move BLT.
  Read BLT.
  Color Expansion.
  Move BLT with Color Expansion.

2.8 MediaPlug Interface

- Built-in WINNOV MediaPlug interface.
- Videum®Cam support at resolution of 320x240x256 color at 30fps.

2.9 Miscellaneous

- The memory data bus, MD[15:0], is used to configure the chip at power-on.
- Three General Purpose Input/Output pins, GPIO[3:1], are available if upper Memory Address pins are not required for asymmetric DRAM support.
- Power save mode is initiated by software.
- Operating voltage from 2.7 volts to 5.5 volts.
- 128-pin QFP15 surface mount package.

3 Typical System Implementation Diagrams

For the pin mapping of each system implementation, see Table 5-7:, “CPU Interface Pin Mapping,” on page 32.

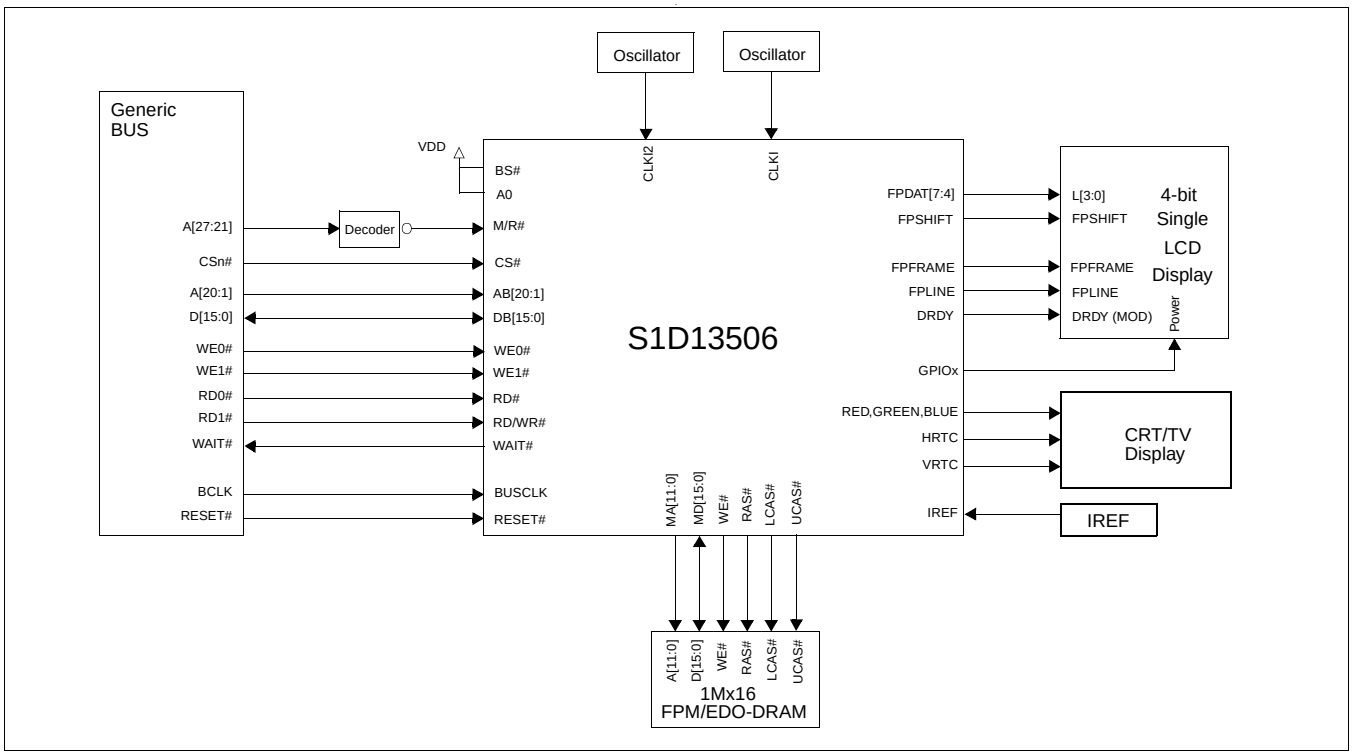

Figure 3-1: Typical System Diagram (Generic Bus)

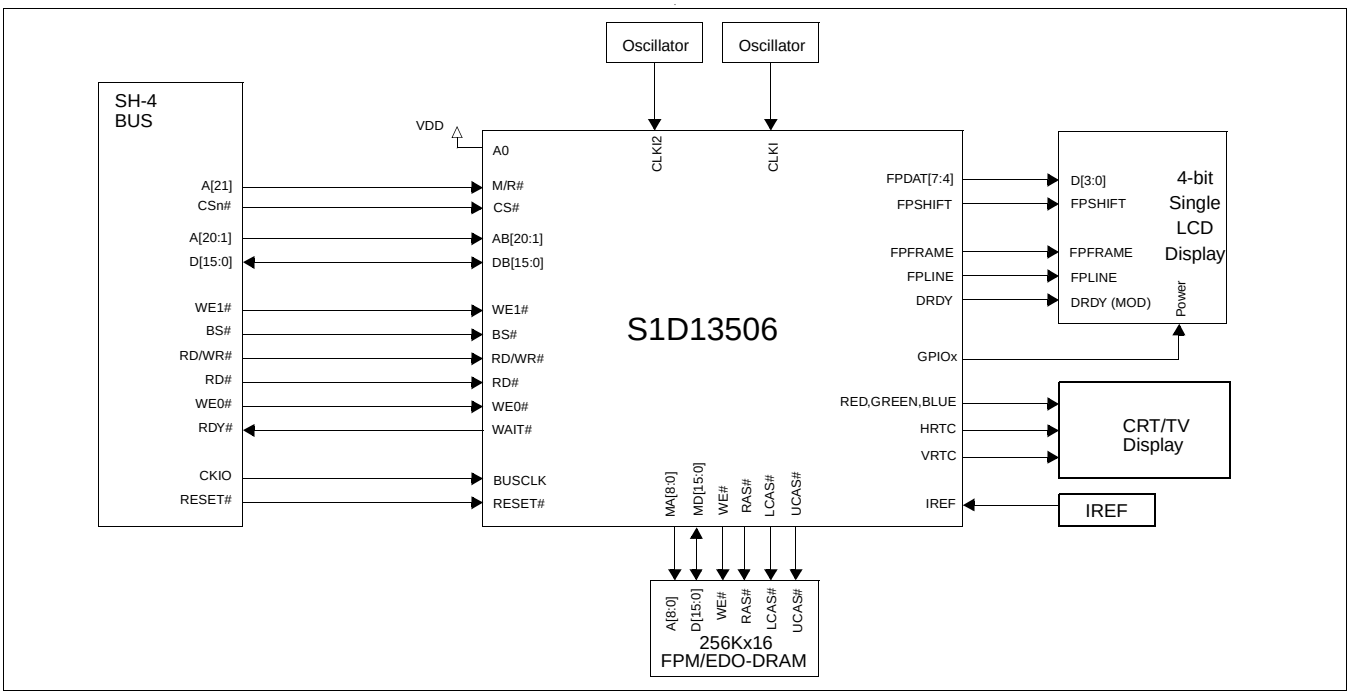

Figure 3-2: Typical System Diagram (Hitachi SH-4 Bus)

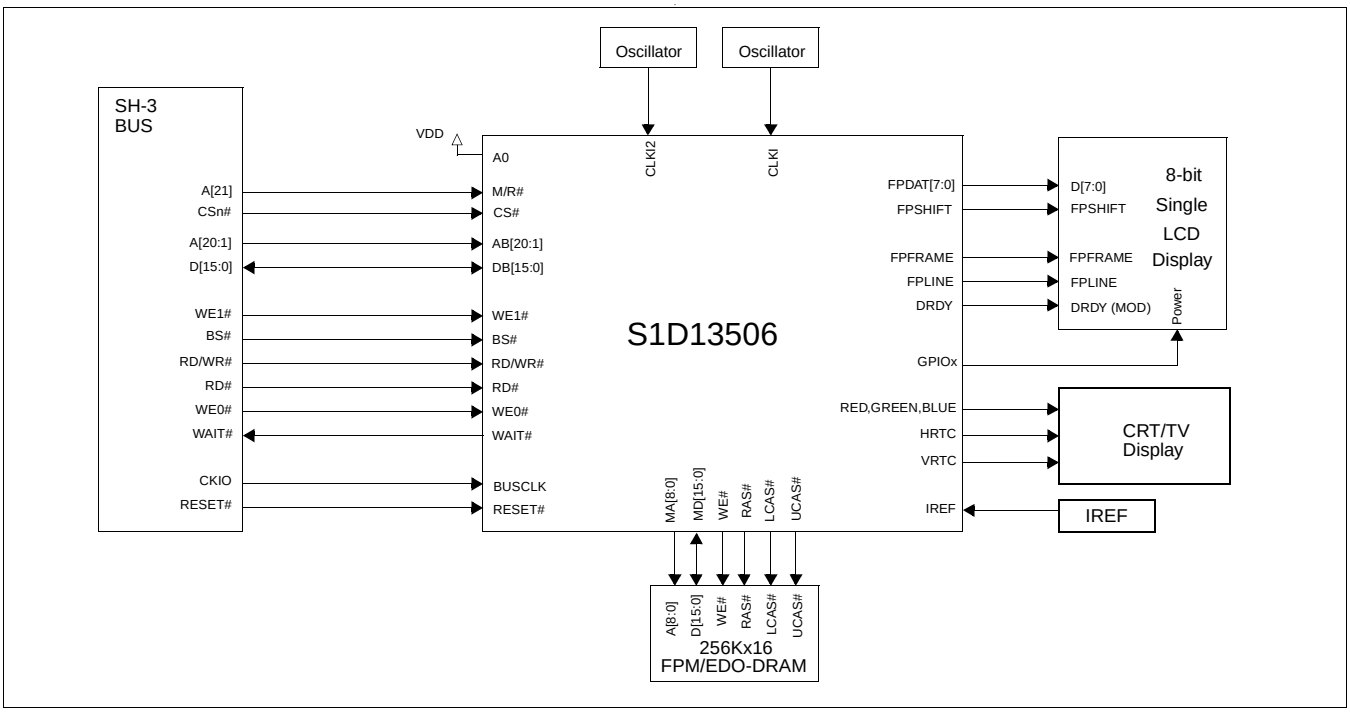

Figure 3-3: Typical System Diagram (Hitachi SH-3 Bus)

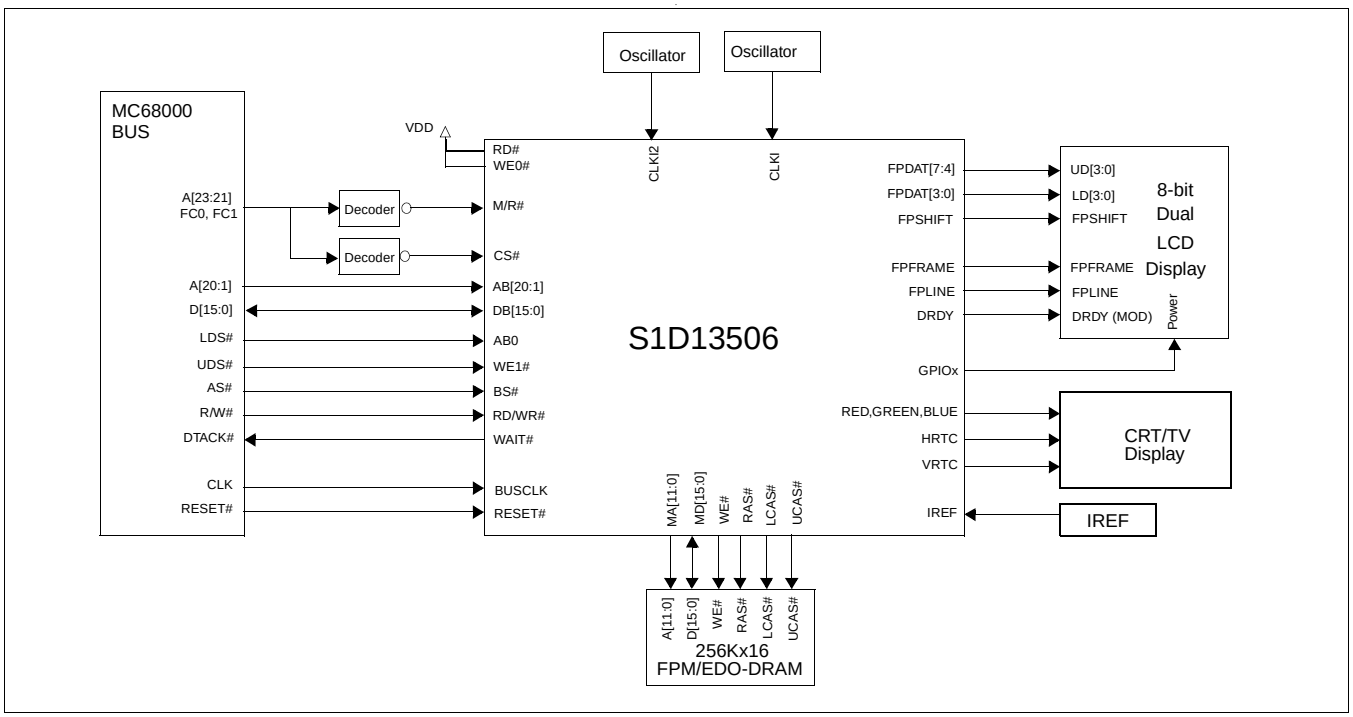

Figure 3-4: Typical System Diagram (MC68K Bus 1, Motorola 16-Bit 68000)

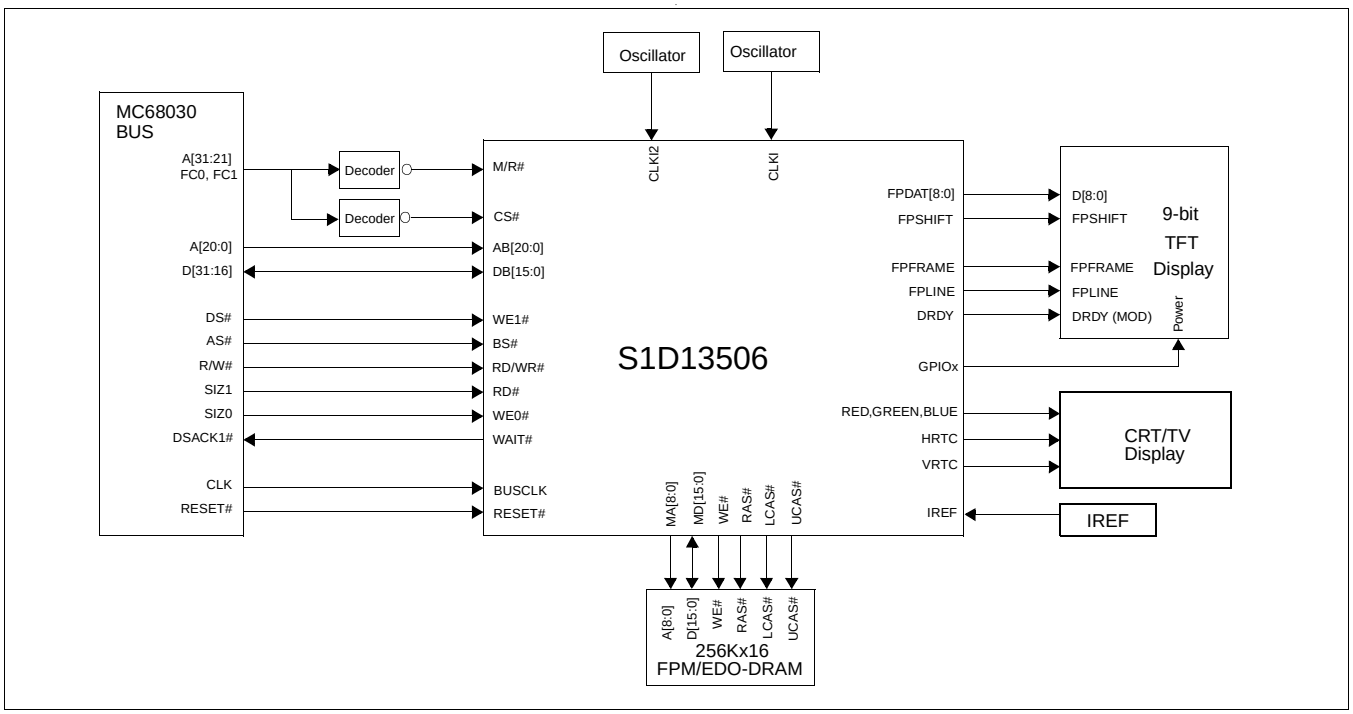

Figure 3-5: Typical System Diagram (MC68K Bus 2, Motorola 32-Bit 68030)

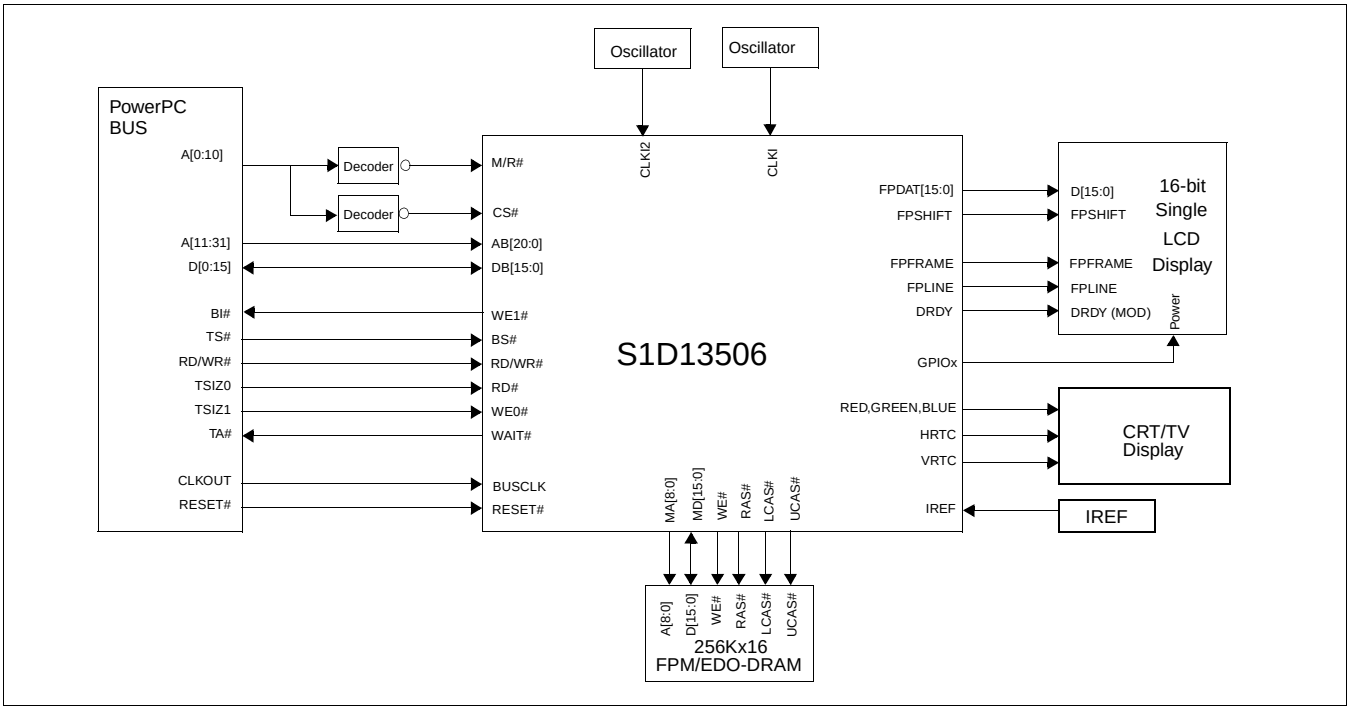

Figure 3-6: Typical System Diagram (Motorola PowerPC Bus)

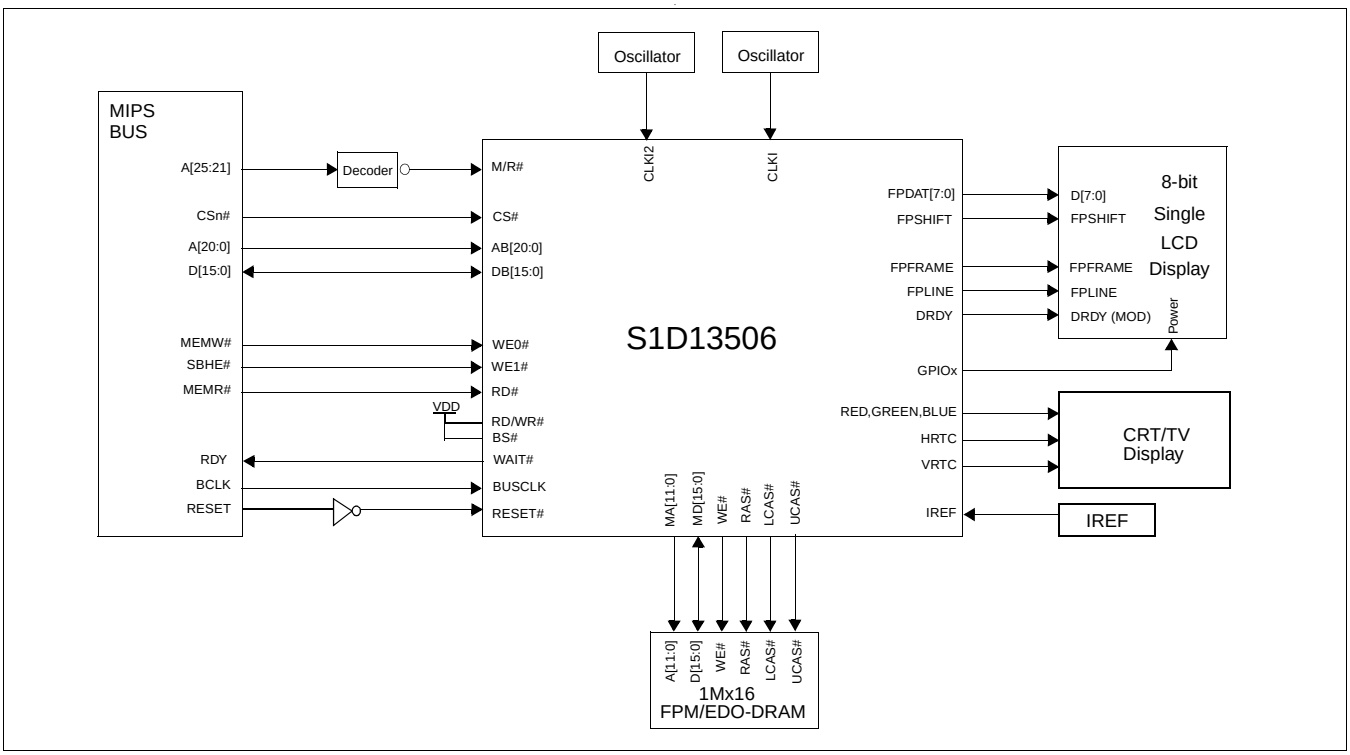

Figure 3-7: Typical System Diagram (NECVR41xx MIPS Bus)

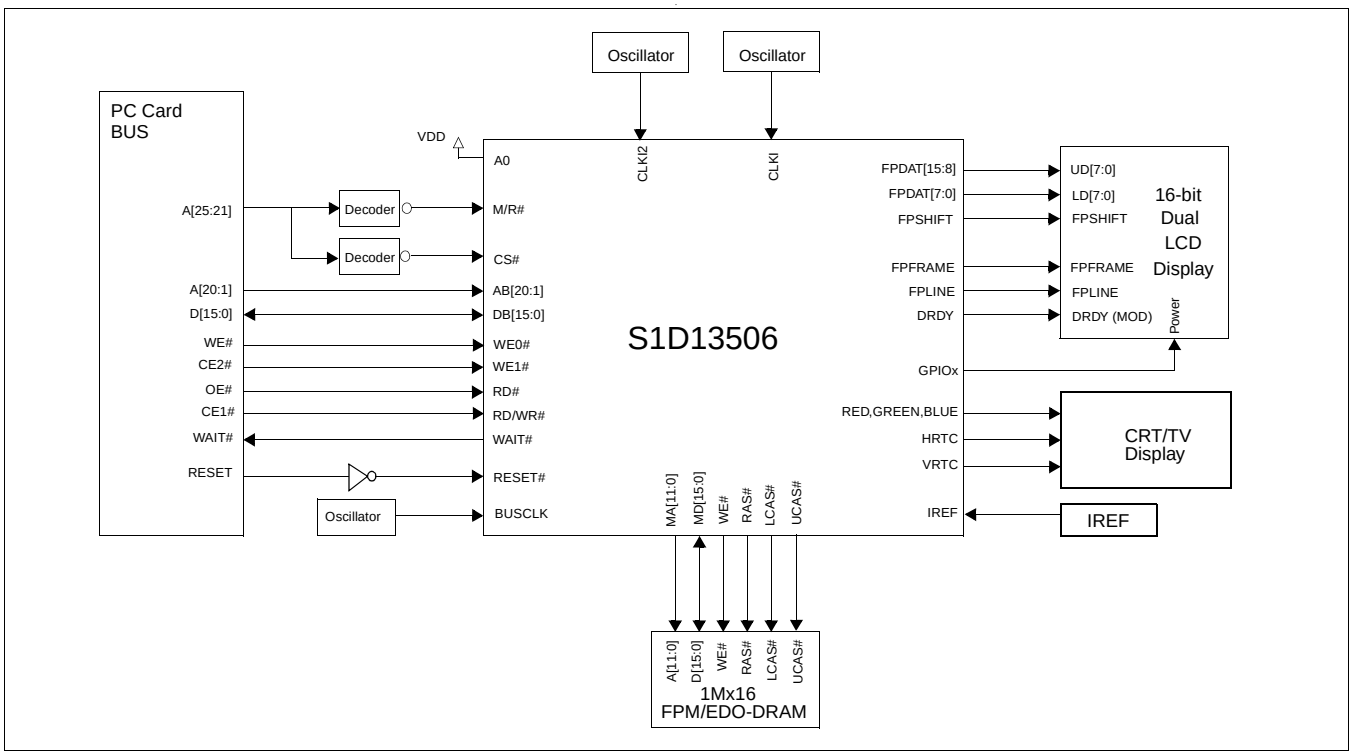

Figure 3-8: Typical System Diagram (PC Card Bus)

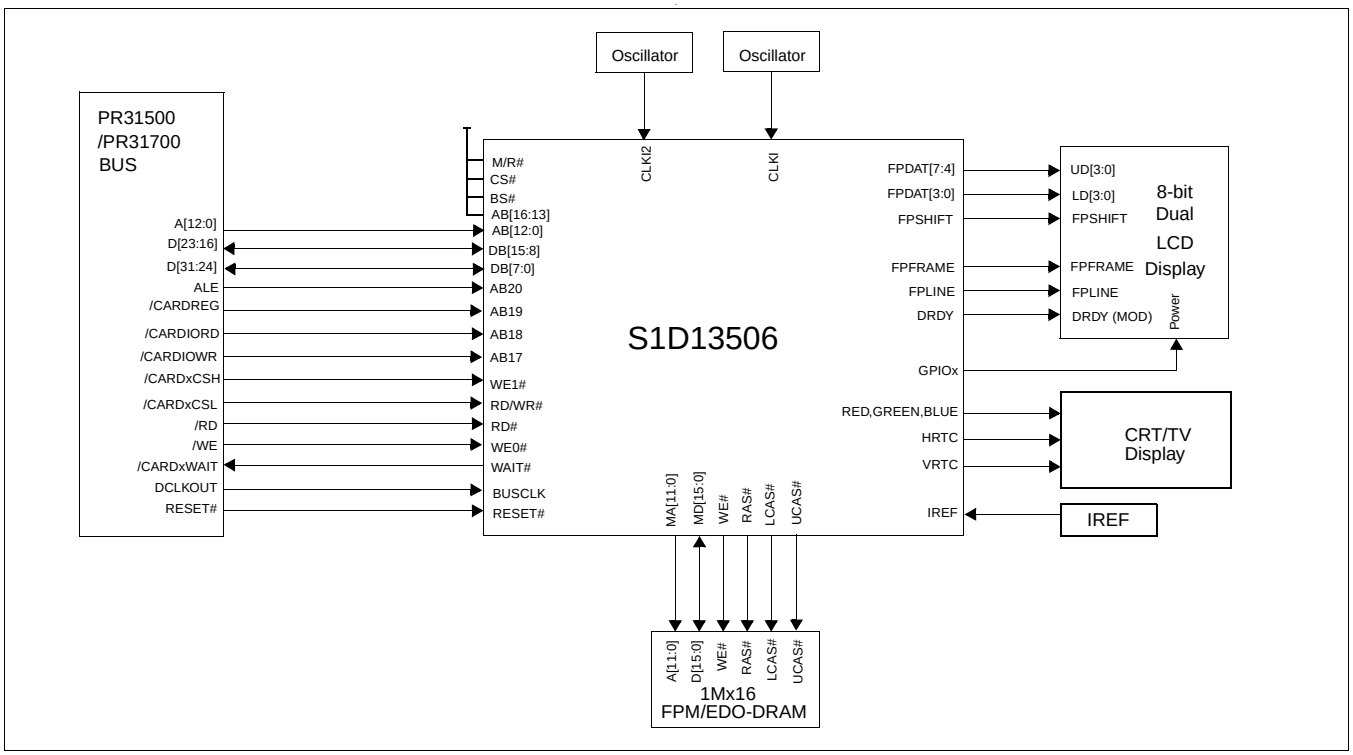

Figure 3-9: Typical System Diagram (Philips MIPS PR31500/PR31700 Bus)

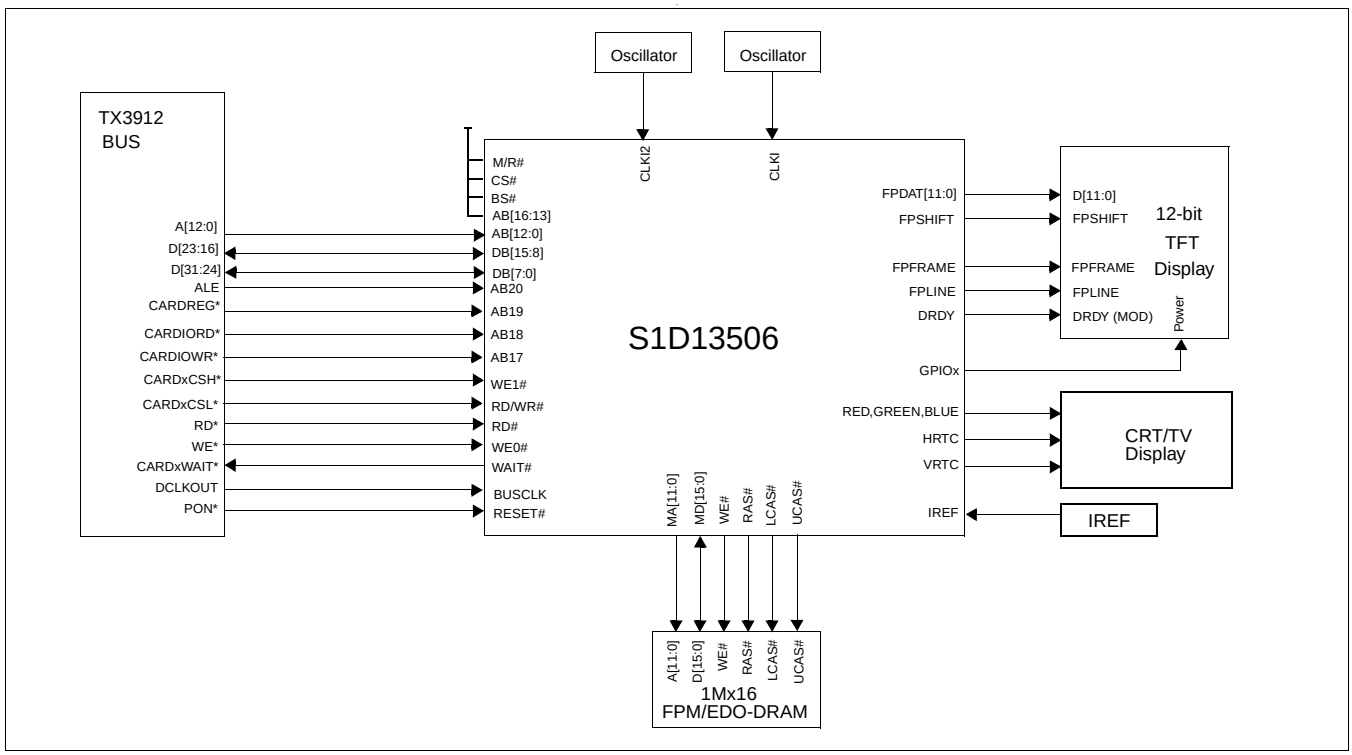

Figure 3-10: Typical System Diagram (Toshiba MIPS TX3912 Bus)

4 Internal Description

4.1 Block Diagram Showing Pipelines

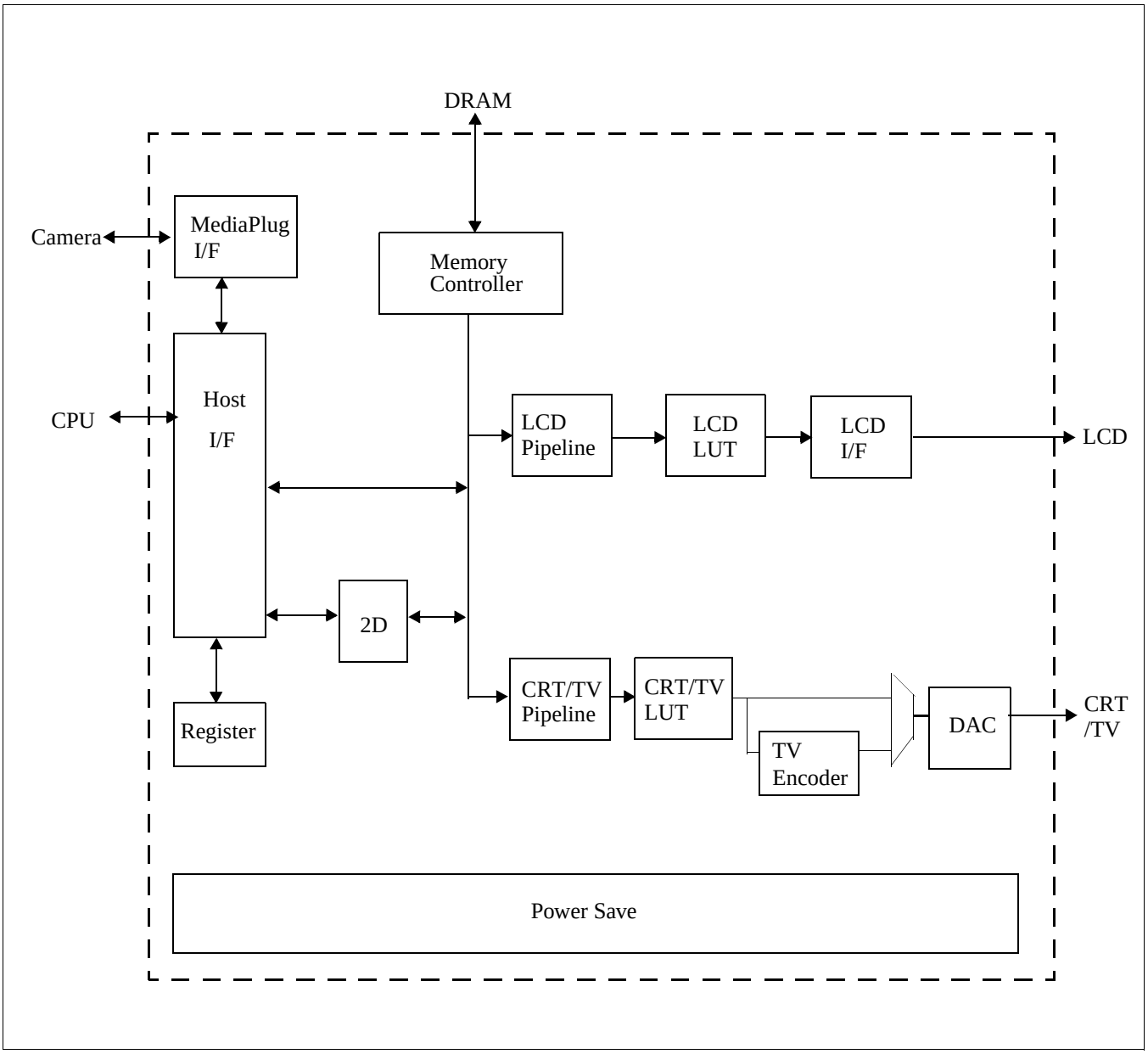

Figure 4-1: S1D13506 Block Diagram

5 Pins

5.1 Pinout Diagram

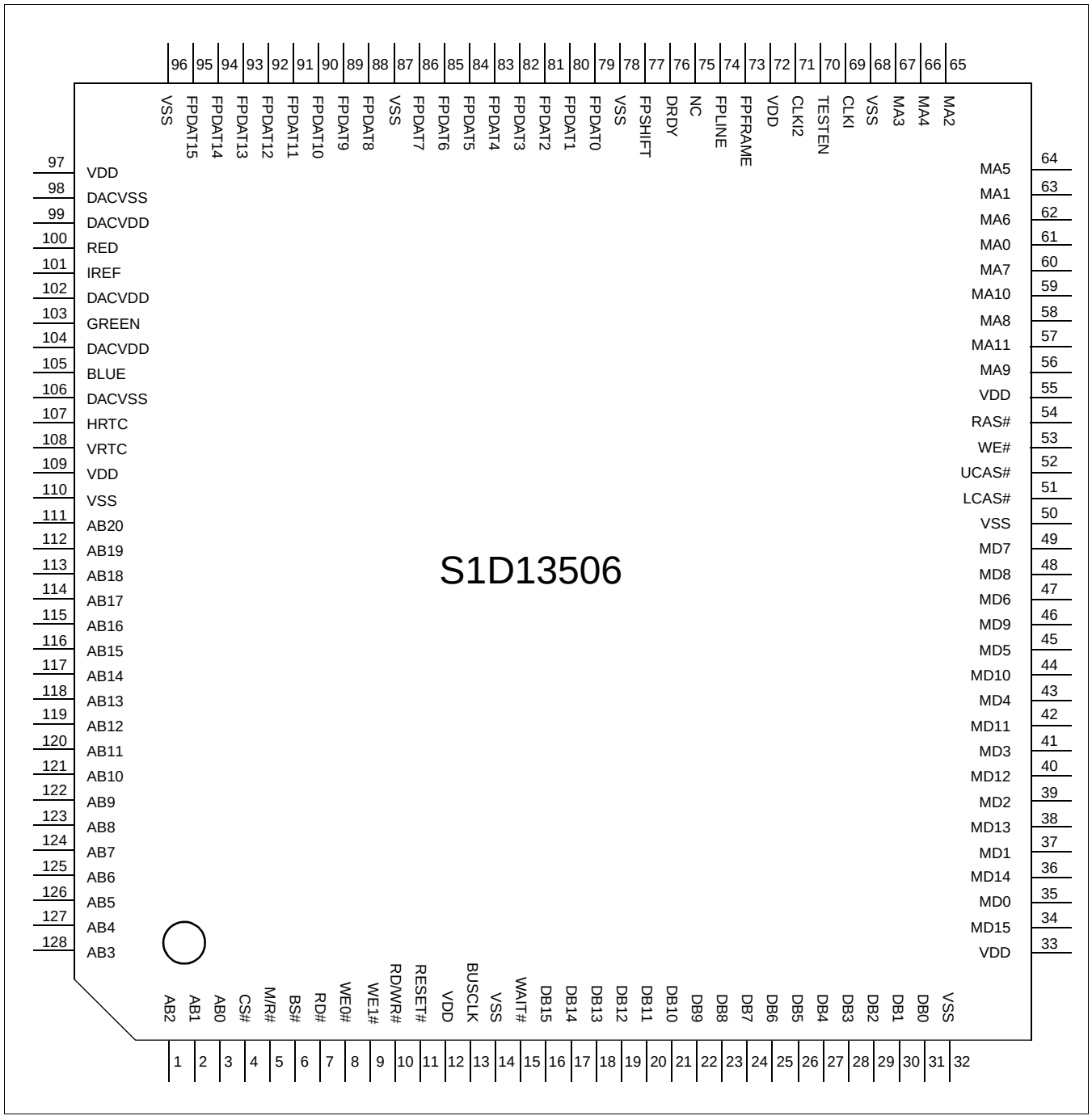

Figure 5-1: Pinout Diagram

128-pin QFP15 surface mount package

5.2 Pin Description

Key:

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
A	=	Analog
P	=	Power pin
C	=	CMOS level input
CD	=	CMOS level input with pull down resistor (typical values of 50Ω/90KΩ at 5V/3.3V respectively)
CS	=	CMOS level Schmitt input
COx	=	CMOS output driver, x denotes driver type (1=4/-4mA, 2=8/-8mA, 3=12/-12mA @ 5V)
TSx	=	Tri-state CMOS output driver, x denotes driver type (1=4/-4mA, 2=8/-8mA, 3=12/-12mA @ 5V), x denotes driver type (1=4/-4mA, 2=8/-8mA, 3=12/-12mA @ 5V)
TSu	=	TSx with pull up resistor (typical values of 100KΩ/180KΩ at 5V/3.3V respectively)
TSxD	=	TSx with pull down resistor, x denotes driver type (1=4/-4mA, 2=8/-8mA, 3=12/-12mA @ 5V) (typical values of 100KΩ/180KΩ at 5V/3.3V)
CNx	=	CMOS low-noise output driver, x denotes driver type (1=4/-4mA, 2=8/-8mA, 3=12/-12mA @ 5V)
CNxU	=	CNx with pull up resistor, x denotes driver type (1=4/-4mA, 2=8/-8mA, 3=12/-12mA @ 5V)
CNxD	=	CNx with pull down resistor, x denotes driver type (1=4/-4mA, 2=8/-8mA, 3=12/-12mA @ 5V)

5.2.1 Host Bus Interface

Table 5-1: Host Bus Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
AB0	I	3	CS	Hi-Z	• For SH-3/SH-4 Bus, this pin must be connected to V_{SS} or V_{DD}. • For MC68K Bus 1, this pin inputs the lower data strobe (LDS#). • For MC68K Bus 2, this pin inputs system address bit 0 (A0). • For Generic Bus, this pin must be connected to V_{SS} or V_{DD}. • For MIPS/ISA Bus, this pin inputs system address bit 0 (SA0). • For Philips PR31500/31700 Bus, this pin inputs system address bit 0 (A0). • For Toshiba TX3912 Bus, this pin inputs system address bit 0 (A0). • For PowerPC Bus, this pin inputs system address bit 31 (A31). • For PC Card (PCMCIA) Bus, this pin must be connected to V_{SS} or V_{DD}. SeeTable 5-7:, “CPU Interface Pin Mapping,” on page 32 for summary. See the respective AC Timing diagram for detailed functionality.
AB[12:1]	I	119-128, 1, 2	C	Hi-Z	• For PowerPC Bus, these pins input the system address bits 19 through 30 (A[19:30]). • For all other busses, these pins input the system address bits 12 through 1 (A[12:1]). See Table 5-7:, “CPU Interface Pin Mapping,” on page 32 for summary. See the respective AC Timing diagram for detailed functionality.

Table 5-1: Host Bus Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
AB[16:13]	I	115-118	C	Hi-Z	• For Philips PR31500/31700 Bus, these pins are connected to V_{DD}. • For Toshiba TX3912 Bus, these pins are connected to V_{DD}. • For PowerPC Bus, these pins input the system address bits 15 through 18 (A[15:18]). • For all other busses, these pins input the system address bits 16 through 13 (A[16:13]). See Table 5-7:, “CPU Interface Pin Mapping,” on page 32 for summary. See the respective AC Timing diagram for detailed functionality.
AB17	I	114	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin inputs the IO write command (/CARDIOWR). • For Toshiba TX3912 Bus, this pin inputs the IO write command (CARDIOWR*). • For PowerPC Bus, this pin inputs the system address bit 14 (A14). • For all other busses, this pin inputs the system address bit 17 (A17). See Table 5-7:, “CPU Interface Pin Mapping,” on page 32 for summary. See the respective AC Timing diagram for detailed functionality.
AB18	I	113	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin inputs the IO read command (/CARDIORD). • For Toshiba TX3912 Bus, this pin inputs the IO read command (CARDIORD*). • For PowerPC Bus, this pin inputs the system address bit 13 (A13). • For all other busses, this pin inputs the system address bit 18 (A18). See Table 5-7:, “CPU Interface Pin Mapping,” on page 32 for summary. See the respective AC Timing diagram for detailed functionality.
AB19	I	112	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin inputs the card control register access (/CARDREG). • For Toshiba TX3912 Bus, this pin inputs the card control register access (CARDREG*). • For PowerPC Bus, this pin inputs the system address bit 12 (A12). • For all other busses, this pin inputs the system address bit 19 (A19). See Table 5-7:, “CPU Interface Pin Mapping,” on page 32 for summary. See the respective AC Timing diagram for detailed functionality.
AB20	I	111	C	Hi-Z	• For the MIPS/ISA Bus, this pin inputs system address bit 20. Note that for the ISA Bus, the unlatched LA20 must first be latched before input to AB20. • For Philips PR31500/31700 Bus, this pin inputs the address latch enable (ALE). • For Toshiba TX3912 Bus, this pin inputs the address latch enable (ALE). • For PowerPC Bus, this pin inputs the system address bit 11 (A11). • For all other busses, this pin inputs the system address bit 20 (A20). See Table 5-7:, “CPU Interface Pin Mapping,” on page 32 for summary. See the respective AC Timing diagram for detailed functionality.

Table 5-1: Host Bus Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
DB[15:0]	IO	16-31	C/TS2	Hi-Z	These pins are the system data bus. For 8-bit bus modes, unused data pins should be tied to V_{DD}. • For SH-3/SH-4 Bus, these pins are connected to D[15:0]. • For MC68K Bus 1, these pins are connected to D[15:0]. • For MC68K Bus 2, these pins are connected to D[31:16] for 32-bit devices (e.g. MC68030) or D[15:0] for 16-bit devices (e.g. MC68340). • For Generic Bus, these pins are connected to D[15:0]. • For MIPS/ISA Bus, these pins are connected to SD[15:0]. • For Philips PR31500/31700 Bus, pins DB[15:8] are connected to D[23:16] and pins DB[7:0] are connected to D[31:24]. • For Toshiba TX3912 Bus, pins DB[15:8] are connected to D[23:16] and pins DB[7:0] are connected to D[31:24]. • For PowerPC Bus, these pins are connected to D[0:15]. • For PC Card (PCMCIA) Bus, these pins are connected to D[15:0]. See Table 5-7:, “CPU Interface Pin Mapping,” on page 32 for summary. See the respective AC Timing diagram for detailed functionality.
WE1#	IO	9	CS/TS 2	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the write enable signal for the upper data byte (WE1#). • For MC68K Bus 1, this pin inputs the upper data strobe (UDS#). • For MC68K Bus 2, this pin inputs the data strobe (DS#). • For Generic Bus, this pin inputs the write enable signal for the upper data byte (WE1#). • For MIPS/ISA Bus, this pin inputs the system byte high enable signal (SBHE#). • For Philips PR31500/31700 Bus, this pin inputs the odd byte access enable signal (/CARDxCSH). • For Toshiba TX3912 Bus, this pin inputs the odd byte access enable signal (CARDxCSH*). • For PowerPC Bus, this pin outputs the burst inhibit signal (BI#). • For PC Card (PCMCIA) Bus, this pin inputs the card enable 2 signal (CE2#). See Table 5-7:, “CPU Interface Pin Mapping,” on page 32 for summary. See the respective AC Timing diagram for detailed functionality.
M/R#	I	5	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin is connected to V_{DD}. • For Toshiba TX3912 Bus, this pin is connected to V_{DD}. • For all other busses, this input pin is used to select between the display buffer and register address spaces of the S1D13506. M/R# is set high to access the display buffer and low to access the registers. See *Register Mapping*. See Table 5-7:, “CPU Interface Pin Mapping,” on page 32.
CS#	I	4	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin is connected to V_{DD}. • For Toshiba TX3912 Bus, this pin is connected to V_{DD}. • For all other busses, this is the Chip Select input. See Table 5-7:, “CPU Interface Pin Mapping,” on page 32. See the respective AC Timing diagram for detailed functionality.

Table 5-1: Host Bus Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
BUSCLK	I	13	C	Hi-Z	This pin inputs the system bus clock. It is possible to apply a 2x clock and divide it by 2 internally - see MD12 in *Summary of Configuration Options*. • For SH-3/SH-4 Bus, this pin is connected to CKIO. • For MC68K Bus 1, this pin is connected to CLK. • For MC68K Bus 2, this pin is connected to CLK. • For Generic Bus, this pin is connected to BCLK. • For MIPS/ISA Bus, this pin is connected to CLK. • For Philips PR31500/31700 Bus, this pin is connected to DCLKOUT. • For Toshiba TX3912 Bus, this pin is connected to DCLKOUT. • For PowerPC Bus, this pin is connected to CLKOUT. • For PC Card (PCMCIA) Bus, this pin is connected to an external input clock source. See Table 5-7:, “CPU Interface Pin Mapping,” on page 32 for summary. See the respective AC Timing diagram for detailed functionality.
BS#	I	6	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the bus start signal (BS#). • For MC68K Bus 1, this pin inputs the address strobe (AS#). • For MC68K Bus 2, this pin inputs the address strobe (AS#). • For Generic Bus, this pin is connected to V_{DD}. • For MIPS/ISA Bus, this pin is connected to V_{DD}. • For Philips PR31500/31700 Bus, this pin is connected to V_{DD}. • For Toshiba TX3912 Bus, this pin is connected to V_{DD}. • For PowerPC Bus, this pin inputs the Transfer Start signal (TS#). • For PC Card (PCMCIA) Bus, this pin is connected to V_{DD}. See Table 5-7:, “CPU Interface Pin Mapping,” on page 32 for summary. See the respective AC Timing diagram for detailed functionality.
RD/WR#	I	10	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the read write signal (RD/WR#). The S1D13506 needs this signal for early decode of the bus cycle. • For MC68K Bus 1, this pin inputs the read write signal (R/W#). • For MC68K Bus 2, this pin inputs the read write signal (R/W#). • For Generic Bus, this pin inputs the read command for the upper data byte (RD1#). • For MIPS/ISA Bus, this pin is connected to V_{DD}. • For Philips PR31500/31700 Bus, this pin inputs the even byte access enable signal (/CARDxCSL). • For Toshiba TX3912 Bus, this pin inputs the even byte access enable signal (CARDxCSL*). • For PowerPC Bus, this pin inputs the read write signal (RD/WR#). • For PC Card (PCMCIA) Bus, this pin inputs the card enable 1 signal (CE1#). See Table 5-7:, “CPU Interface Pin Mapping,” on page 32 for summary. See the respective AC Timing diagram for detailed functionality.

Table 5-1: Host Bus Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
RD#	I	7	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the read signal (RD#). • For MC68K Bus 1, this pin is connected to V_{DD}. • For MC68K Bus 2, this pin inputs the bus size bit 1 (SIZ1). • For Generic Bus, this pin inputs the read command for the lower data byte (RD0#). • For MIPS/ISA Bus, this pin inputs the memory read signal (MEMR#). • For Philips PR31500/31700 Bus, this pin inputs the memory read command (/RD). • For Toshiba TX3912 Bus, this pin inputs the memory read command (RD*). • For PowerPC Bus, this pin inputs the transfer size 0 signal (TSIZ0). • For PC Card (PCMCIA) Bus, this pin inputs the output enable signal (OE#). See Table 5-7:, “CPU Interface Pin Mapping,” on page 32 for summary. See the respective AC Timing diagram for detailed functionality.
WE0#	I	8	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the write enable signal for the lower data byte (WE0#). • For MC68K Bus 1, this pin must be connected to V_{DD} • For MC68K Bus 2, this pin inputs the bus size bit 0 (SIZ0). • For Generic Bus, this pin inputs the write enable signal for the lower data byte (WE0#). • For MIPS/ISA Bus, this pin inputs the memory write signal (MEMW#). • For Philips PR31500/31700 Bus, this pin inputs the memory write command (/WE). • For Toshiba TX3912 Bus, this pin inputs the memory write command (WE*). • For PowerPC Bus, this pin inputs the Transfer Size 1 signal (TSIZ1). • For PC Card (PCMCIA) Bus, this pin inputs the write enable signal (WE#). See Table 5-7:, “CPU Interface Pin Mapping,” on page 32 for summary. See the respective AC Timing diagram for detailed functionality.

Table 5-1: Host Bus Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
WAIT#	O	15	TS2	Hi-Z[a] or 1[b] or 0[c]	The active polarity of the WAIT# output is configurable; the state of MD5 on the rising edge of RESET# defines the active polarity of WAIT# - see *"Summary of Configuration Options"*. • For SH-3 Bus, this pin outputs the wait request signal (WAIT#); MD5 must be pulled low during reset by the internal pull-down resistor. • For SH-4 Bus, this pin outputs the ready signal (RDY#); MD5 must be pulled high during reset by an external pull-up resistor. • For MC68K Bus 1, this pin outputs the data transfer acknowledge signal (DTACK#); MD5 must be pulled high during reset by an external pull-up resistor. • For MC68K Bus 2, this pin outputs the data transfer and size acknowledge bit 1 (DSACK1#); MD5 must be pulled high during reset by an external pull-up resistor. • For Generic Bus, this pin outputs the wait signal (WAIT#); MD5 must be pulled low during reset by the internal pull-down resistor. • For MIPS/ISA Bus, this pin outputs the IO channel ready signal (IOCHRDY); MD5 must be pulled low during reset by the internal pull-down resistor. • For Philips PR31500/31700 Bus, this pin outputs the wait state signal (/CARDxWAIT). MD5 must be pulled low during reset by the internal pull-down resistor. • For Toshiba TX3912 Bus, this pin outputs the wait state signal (CARDxWAIT*). MD5 must be pulled low during reset by the internal pull-down resistor. • For PowerPC Bus, this pin outputs the transfer acknowledge signal (TA#); MD5 must be pulled high during reset by an external pull-up resistor. • For PC Card (PCMCIA) Bus, this pin outputs the wait signal (WAIT#); MD5 must be pulled low during reset by the internal pull-down resistor. See Table 5-7:, "CPU Interface Pin Mapping," on page 32 for summary. See the respective AC Timing diagram for detailed functionality.
RESET#	I	11	CS	0	Active low input that clears all internal registers and forces all outputs to their inactive states. Note that active high RESET signals must be inverted before input to this pin.

[a]When the MD configuration at RESET# is set such that WAIT# can be tristated.
[b]When the MD configuration at RESET# is set such that WAIT# is always driven and active low.
[c]When the MD configuration at RESET# is set such that WAIT# is always driven and active high.

5.2.2 Memory Interface

Table 5-2: Memory Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
LCAS#	O	51	CO1	1	• For dual-CAS# DRAM, this is the column address strobe for the lower byte (LCAS#). • For single-CAS DRAM, this is the column address strobe (CAS#). See Table 5-8:, “Memory Interface Pin Mapping,” on page 33 for summary. See Memory Interface Timing on page 62 for detailed functionality.
UCAS#	O	52	CO1	1	This is a multi-purpose pin: • For dual-CAS# DRAM, this is the column address strobe for the upper byte (UCAS#). • For single-CAS# DRAM, this is the write enable signal for the upper byte (UWE#). See Table 5-8:, “Memory Interface Pin Mapping,” on page 33 for summary. See Memory Interface Timing on page 62 for detailed functionality.
WE#	O	53	CO1	1	• For dual-CAS# DRAM, this is the write enable signal (WE#). • For single-CAS# DRAM, this is the write enable signal for the lower byte (LWE#). See Table 5-8:, “Memory Interface Pin Mapping,” on page 33 for summary. See Memory Interface Timing on page 62 for detailed functionality.
RAS#	O	54	CO1	1	Row address strobe - see Memory Interface Timing on page 62 for detailed functionality.
MD[15:0]	IO	34, 36, 38, 40, 42, 44, 46, 48, 49, 47, 45, 43, 41, 39, 37, 35	C/TS1D	Hi-Z (pull 0)	Bi-directional memory data bus. During reset, these pins are inputs and their states at the rising edge of RESET# are used to configure the chip - see Summary of Configuration Options on page 31. Internal pull-down resistors (typical values of 100KΩ/180KΩ at 5V/3.3V respectively) pull the reset states to 0. External pull-up resistors can be used to pull the reset states to 1. See Memory Interface Timing on page 62 for detailed functionality.

Table 5-2: Memory Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
MA[8:0]	O	58, 60, 62, 64, 66, 67, 65, 63, 61	CO1	0	Multiplexed memory address - see Memory Interface Timing on page 62 for detailed functionality.
MA9	IO	56	C/TS1	0[a] or Hi-Z[b]	This is a multi-purpose pin: • For 2M byte DRAM, this is memory address bit 9 (MA9). • For asymmetrical 512K byte DRAM, this is memory address bit 9 (MA9). • For symmetrical 512K byte DRAM, this pin can be used as general purpose IO pin 3 (GPIO3). Note that unless configured otherwise, this pin defaults to an input and must be driven to a valid logic level. See Table 5-8:, “Memory Interface Pin Mapping,” on page 33 for summary. See Memory Interface Timing on page 62 for detailed functionality.
MA10	IO	59	C/TS1	0[c] or Hi-Z[d]	This is a multi-purpose pin: • For asymmetrical 2M byte DRAM this is memory address bit 10 (MA10). • For symmetrical 2M byte DRAM and all 512K byte DRAM this pin can be used as general purpose IO pin 1 (GPIO1). Note that unless configured otherwise, this pin defaults to an input and must be driven to a valid logic level. See Table 5-8:, “Memory Interface Pin Mapping,” on page 33 for summary. See Memory Interface Timing on page 62 for detailed functionality.
MA11	IO	57	C/TS1	0[e] or Hi-Z[f] or 1[g]	This is a multi-purpose pin: • For asymmetrical 2M byte DRAM this is memory address bit 11 (MA11). • For symmetrical 2M byte DRAM and all 512K byte DRAM this pin can be used as general purpose IO pin 2 (GPIO2). Note that unless configured otherwise, this pin defaults to an input and must be driven to a valid logic level. See Table 5-8:, “Memory Interface Pin Mapping,” on page 33 for summary. See Memory Interface Timing on page 62 for detailed functionality. This pin can also be configured as the MediaPlug power pin VMPEPWR - see Table 5-10:, “MA11, MA10, MA9, and DRDY Pin Mapping,” on page 35 for details.

[a]When the MD configuration at RESET# is set such that MA9 is used as MA9.
[b]When the MD configuration at RESET# is set such that MA9 is used as GPIO3.
[c]When the MD configuration at RESET# is set such that MA10 is used as MA10.
[d]When the MD configuration at RESET# is set such that MA10 is used as GPIO1.
[e]When the MD configuration at RESET# is set such that MA11 is used as MA11.
[f]When the MD configuration at RESET# is set such that MA11 is used as GPIO2.
[g]When the MD configuration at RESET# is set such that MA11 is used as VMPEPWR.

5.2.3 LCD Interface

Table 5-3: LCD Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
FPDAT[8:0]	O	88, 86-79	CN3	0	Panel data bus. Not all pins are used for some panels - see Table 5-9:, “LCD Interface Pin Mapping,” on page 34 for details. Unused pins are driven low. FPDAT[15:8] can be configured for MediaPlug interface - see Table 5-11:, “MediaPlug Interface Pin Mapping,” on page 35 for details.
FPDAT9	O	89	CN3D	0[a] or Hi-Z[b]	Panel data bus. Not all pins are used for some panels - see Table 5-9:, “LCD Interface Pin Mapping,” on page 34 for details. Unused pins are driven low. FPDAT[15:8] can be configured for MediaPlug interface - see Table 5-11:, “MediaPlug Interface Pin Mapping,” on page 35 for details.
FPDAT[13:10]	IO	93-90	C/TS3U	0[c] or Hi-Z[d]	Panel data bus. Not all pins are used for some panels - see Table 5-9:, “LCD Interface Pin Mapping,” on page 34 for details. Unused pins are driven low. FPDAT[15:8] can be configured for MediaPlug interface - see Table 5-11:, “MediaPlug Interface Pin Mapping,” on page 35 for details.
FPDAT[15:14]	O	95,94	CN3	0	Panel data bus. Not all pins are used for some panels - see Table 5-9:, “LCD Interface Pin Mapping,” on page 34 for details. Unused pins are driven low. FPDAT[15:8] can be configured for MediaPlug interface - see Table 5-11:, “MediaPlug Interface Pin Mapping,” on page 35 for details.
FPFRAME	O	73	CN3	0	Frame pulse
FPLINE	O	74	CN3	0	Line pulse
FPSHIFT	O	77	CO3	0	Shift clock
DRDY	O	76	CO3	0[e] or 1[f]	This is a multi-purpose pin: • For TFT/D-TFD panels this is the display enable output (DRDY). • For passive LCD with Format 1 interface this is the 2nd Shift Clock (FPSHIFT2). • For all other LCD panels this is the LCD backplane bias signal (MOD). See Table 5-9:, “LCD Interface Pin Mapping,” on page 34 and REG[030h] for details. This pin can also be configured as the MediaPlug power pin VMPEPWR - see Table 5-10:, “MA11, MA10, MA9, and DRDY Pin Mapping,” on page 35 for details.

[a]When the MD configuration at RESET# is set such that FPDAT9 is used as FPDAT9.
[b]When the MD configuration at RESET# is set such that FPDAT9 is used as VMPRCTL.
[c]When the MD configuration at RESET# is set such that FPDAT[13:10] is used as FPDAT[13:10].
[d]When the MD configuration at RESET# is set such that FPDAT[13:10] is used as VMPD[3:0].
[e]When the MD configuration at RESET# is set such that DRDY is used as DRDY (MOD).
[f]When the MD configuration at RESET# is set such that DRDY is used as VMPEPWR.

5.2.4 CRT Interface

Table 5-4: CRT Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
HRTC	O	107	CN3	0	Horizontal retrace signal for CRT
VRTC	O	108	CN3	0	Vertical retrace signal for CRT
RED	O	100	A	no output current	Analog output for CRT color Red / S-Video Luminance
GREEN	O	103	A	no output current	Analog output for CRT color Green / Composite Video Out
BLUE	O	105	A	no output current	Analog output for CRT color Blue / S-Video Chrominance
IREF	I	101	A	--	Current reference for DAC. This pin must be connected to V_{SS} if the DAC is not needed.

5.2.5 Miscellaneous

Table 5-5: Miscellaneous Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
CLKI	I	69	C	--	Selectable input clock. Can be used for the internal pixel clock (PCLK), memory clock (MCLK), and MediaPlug Clock.
CLKI2	I	71	C	--	Selectable input clock. Can be used for the internal pixel clock (PCLK) and MediaPlug Clock.
TESTEN	I	70	CD	--	Test Enable. This pin should be connected to V_{SS} for normal operation.
VDD	P	12, 33, 55, 72, 97, 109	P	--	V_{DD}
DACVDD	P	99, 102, 104	P	--	DAC V_{DD}
VSS	P	14, 32, 50, 68, 78, 87, 96, 110	P	--	V_{SS}
DACVSS	P	98, 106	P	--	DAC V_{SS}
NC	-	75		--	Not connected

5.3 Summary of Configuration Options

Table 5-6: Summary of Power-On/Reset Options

Pin Name	value of this pin at rising edge of RESET# is used to configure:(1/0)	
	1	**0**
MD0	Not used, value of this pin at rising edge of RESET# can be read at REG[00Ch] bit 0	
MD11,MD[3:1]	Select Host Bus Interface as follows: **MD11 MD3 MD2 MD1 Host Bus** 0 0 0 0 SH-4/SH-3 Bus interface 0 0 0 1 MC68K Bus 1 0 0 1 0 MC68K Bus 2 0 0 1 1 Generic 0 1 0 0 Reserved 0 1 0 1 MIPS/ISA 0 1 1 0 PowerPC 0 1 1 1 PC Card (PCMCIA) 1 1 1 1 Philips PR31500/PR31700 / Toshiba TX3912	
MD4	Little Endian	Big Endian
MD5	WAIT# is active high (1 = insert wait state)	WAIT# is active low (0 = insert wait state)
MD[7:6]	Memory Address/GPIO configuration: (See Table 5-10:, “MA11, MA10, MA9, and DRDY Pin Mapping,” on page 35) 00 = symmetrical 256K×16 DRAM. MA[8:0] = DRAM address. MA[11:9] can be used as GPIO2,1,3 pins. 01 = symmetrical 1M×16 DRAM. MA[9:0] = DRAM address. MA[11:10] can be used as GPIO2,1 pins. 10 = asymmetrical 256K×16 DRAM. MA[9:0] = DRAM address. MA[11:10] can be used as GPIO2,1 pins. 11 = asymmetrical 1M×16 DRAM. MA[11:0] = DRAM address.	
MD8	Not used, value of this pin at rising edge of RESET# can be read at REG[00Dh] bit 0	
MD9	Not used, value of this pin at rising edge of RESET# can be read at REG[00Dh] bit 1	
MD10	Not Used, value of this pin at rising edge of RESET# can be read at REG[00Dh] bit 2	
MD12	BUSCLK input divided by 2	BUSCLK input not divided
MD13	Configure FPDAT[15:8] for MediaPlug I/F. External latches required to support 16-bit passive panels.	Support 16-bit passive panels directly
MD14	DRDY or MA11 is configured as MediaPlug power down pin (VMPEPWR). (See Table 5-10:, “MA11, MA10, MA9, and DRDY Pin Mapping,” on page 35)	DRDY is configured as a normal LCD I/F output pin. MA11 is configured as either a memory address or GPIO2. (See Table 5-10:, “MA11, MA10, MA9, and DRDY Pin Mapping,” on page 35)
MD15	WAIT# is always driven	WAIT# is tristated when the chip is not accessed by the host

5.4 Multiple Function Pin Mapping

Table 5-7: CPU Interface Pin Mapping

S1D13506 Pin Names	Generic	Hitachi SH-4/SH-3	MIPS/ISA	Motorola MC68K Bus 1	Motorola MC68K Bus 2	Motorola PowerPC	PC Card	Philips PR31500 /PR31700	Toshiba TX3912
AB20	A20	A20	LatchA20	A20	A20	A11	A20	ALE	ALE
AB19	A19	A19	SA19	A19	A19	A12	A19	/CARDREG	CARDREG*
AB18	A18	A18	SA18	A18	A18	A13	A18	/CARDIORD	CARDIORD*
AB17	A17	A17	SA17	A17	A17	A14	A17	/CARDIOWR	CARDIOWR*
AB[16:13]	A[16:13]	A[16:13]	SA[16:13]	A[16:13]	A[16:13]	A[15:18]	A[16:13]	Connected to V_{DD}	Connected to V_{DD}
AB[12:1]	A[12:1]	A[12:1]	SA[12:1]	A[12:1]	A[12:1]	A[19:30]	A[12:1]	A[12:1]	A[12:1]
AB0	Connected to V_{DD}[1]	Connected to V_{DD}[1]	SA0	LDS#	A0	A31	Connected to V_{DD}[1]	A0	A0
DB[15:8]	D[15:0]	D[15:8]	SD[15:0]	D[15:8]	D[31:24]	D[0:7]	D[15:0]	D[23:16]	D[23:16]
DB[7:0]	D[7:0]	D[7:0]	SD[7:0]	D[7:0]	D[23:16]	D[8:15]	D[7:0]	D[31:24]	D[31:24]
WE1#	WE1#	WE1#	SBHE#	UDS#	DS#	$\overline{BI}$	CE2#	/CARDxCSH	CARDxCSH*
M/R#	External Decode							Connected to V_{DD}	Connected to V_{DD}
CS#	External Decode							Connected to V_{DD}	Connected to V_{DD}
BUSCLK	BCLK	CKIO	CLK	CLK	CLK	CLKOUT	External Oscillator[2]	DCLKOUT	DCLKOUT
BS#	Connected to V_{DD}	BS#	Connected to V_{DD}	AS#	AS#	$\overline{TS}$	Connected to V_{DD}	Connected to V_{DD}	Connected to V_{DD}
RD/WR#	RD1#	RD/WR#	Connected to V_{DD}	R/W#	R/W#	$\overline{RD/WR}$	CE1#	/CARDxCSL	CARDxCSL*
RD#	RD0#	RD#	MEMR#	Connected to V_{DD}	SIZ1	TSIZ0	OE#	/RD	RD*
WE0#	WE0#	WE0#	MEMW#	Connected to V_{DD}	SIZ0	TSIZ1	WE#	/WE	WE*
WAIT#	WAIT#	RDY# /WAIT#	IOCHRDY	DTACK#	DSACK1#	$\overline{TA}$	WAIT#	/CARDxWAIT	CARDxWAIT*
RESET#	RESET#	RESET#	inverted RESET	RESET#	RESET#	RESET#	inverted RESET	RESET#	PON*

Note
All GPIO pins default to input on reset and unless programmed otherwise, must be connected to either V_{SS} or IO V_{DD} if not used.

Note
[1] AB0 is not used internally for these busses and must be connected to either V_{SS} or V_{DD}.

[2] For further information on interfacing the S1D13506 to the PC Card bus, see *Interfacing to the PC Card Bus*, document number X25B-G-005-xx.

Table 5-8: Memory Interface Pin Mapping

S1D13506 Pin Names	FPM/EDO-DRAM							
	Sym 256Kx16		Asym 256Kx16		Sym 1Mx16		Asym 1Mx16	
	2-CAS#	2-WE#	2-CAS#	2-WE#	2-CAS#	2-WE#	2-CAS#	2-WE#
MD[15:0]	D[15:0]							
MA[8:0]	A[8:0]							
MA9[1]	GPIO3[2]		A9				A9	
MA10[1]	GPIO1[2]						A10	
MA11[1]	GPIO2[2]						A11	
UCAS#	UCAS#	UWE#	UCAS#	UWE#	UCAS#	UWE#	UCAS#	UWE#
LCAS#	LCAS#	CAS#	LCAS#	CAS#	LCAS#	CAS#	LCAS#	CAS#
WE#	WE#	LWE#	WE#	LWE#	WE#	LWE#	WE#	LWE#
RAS#	RAS#							

Note

[1] For MA9, MA10, and MA11 functionality see Table 5-10:, “MA11, MA10, MA9, and DRDY Pin Mapping,” on page 35.

[2] All GPIO pins default to input on reset and unless programmed otherwise, should be connected to either V_{SS} or IO V_{DD} if not used.

Table 5-9: LCD Interface Pin Mapping

S1D13506 Pin Names	Monochrome Passive Panel			Color Passive Panel						Color TFT/D-TFD Panel		
	Single		Dual	Single	Single Format 1	Single Format 2	Single	Dual				
	4-bit	8-bit	8-bit	4-bit	8-bit	8-bit	16-Bit	8-bit	16-bit	9-bit	12-bit	18-bit
FPFRAME	FPFRAME											
FPLINE	FPLINE											
FPSHIFT	FPSHIFT											
DRDY	MOD				FPSHIFT2	MOD				DRDY		
FPDAT0	driven 0	D0	LD0	driven 0	D0	D0	D0	LD0	LD0	R2	R3	R5
FPDAT1	driven 0	D1	LD1	driven 0	D1	D1	D1	LD1	LD1	R1	R2	R4
FPDAT2	driven 0	D2	LD2	driven 0	D2	D2	D2	LD2	LD2	R0	R1	R3
FPDAT3	driven 0	D3	LD3	driven 0	D3	D3	D3	LD3	LD3	G2	G3	G5
FPDAT4	D0	D4	UD0	D0	D4	D4	D8	UD0	UD0	G1	G2	G4
FPDAT5	D1	D5	UD1	D1	D5	D5	D9	UD1	UD1	G0	G1	G3
FPDAT6	D2	D6	UD2	D2	D6	D6	D10	UD2	UD2	B2	B3	B5
FPDAT7	D3	D7	UD3	D3	D7	D7	D11	UD3	UD3	B1	B2	B4
FPDAT8	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D4	driven 0	LD4	B0	B1	B3
FPDAT9	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D5	driven 0	LD5	driven 0	R0	R2
FPDAT10	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D6	driven 0	LD6	driven 0	driven 0	R1
FPDAT11	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D7	driven 0	LD7	driven 0	G0	G2
FPDAT12	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D12	driven 0	UD4	driven 0	driven 0	G1
FPDAT13	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D13	driven 0	UD5	driven 0	driven 0	G0
FPDAT14	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D14	driven 0	UD6	driven 0	B0	B2
FPDAT15	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D15	driven 0	UD7	driven 0	driven 0	B1

Note

DRDY and FPDAT[15:8] may be used by the MediaPlug interface when the MediaPlug is enabled. For MediaPlug Interface pin mapping, see Table 5-11:.

Note

For FPDATxx to LCD interface hardware connections, refer to Section 7.5, “Display Interface” on page 73.

Table 5-10: MA11, MA10, MA9, and DRDY Pin Mapping

MD14, MD7, MD6	MA11	MA10	MA9	DRDY
000	GPIO2	GPIO1	GPIO3	DRDY
001	GPIO2	GPIO1	MA9	DRDY
010	GPIO2	GPIO1	MA9	DRDY
011	MA11	MA10	MA9	DRDY
100	VMPEPWR	GPIO1	GPIO3	DRDY
101	VMPEPWR	GPIO1	MA9	DRDY
110	VMPEPWR	GPIO1	MA9	DRDY
111	MA11	MA10	MA9	VMPEPWR

Table 5-11: MediaPlug Interface Pin Mapping

S1D13506 Pin Names	IO Type	MediaPlug I/F (MD13=1 at RESET)
FPDAT8	O	VMPLCTL
FPDAT9	I	VMPRCTL
FPDAT10	IO	VMPD0
FPDAT11	IO	VMPD1
FPDAT12	IO	VMPD2
FPDAT13	IO	VMPD3
FPDAT14	O	VMPCLK
FPDAT15	O	VMPCLKN
DRDY or MA11[1]	O	VMPEPWR

Note

[1] Either DRDY or MA11 may be used for VMPEPWR (see Table 5-10: “MA11, MA10, MA9, and DRDY Pin Mapping”). If DRDY is required by the LCD interface and MA11 is required by the DRAM interface then VMPEPWR is not available.

5.5 CRT/TV Interface

The following figure shows external circuitry for the CRT/TV interface.

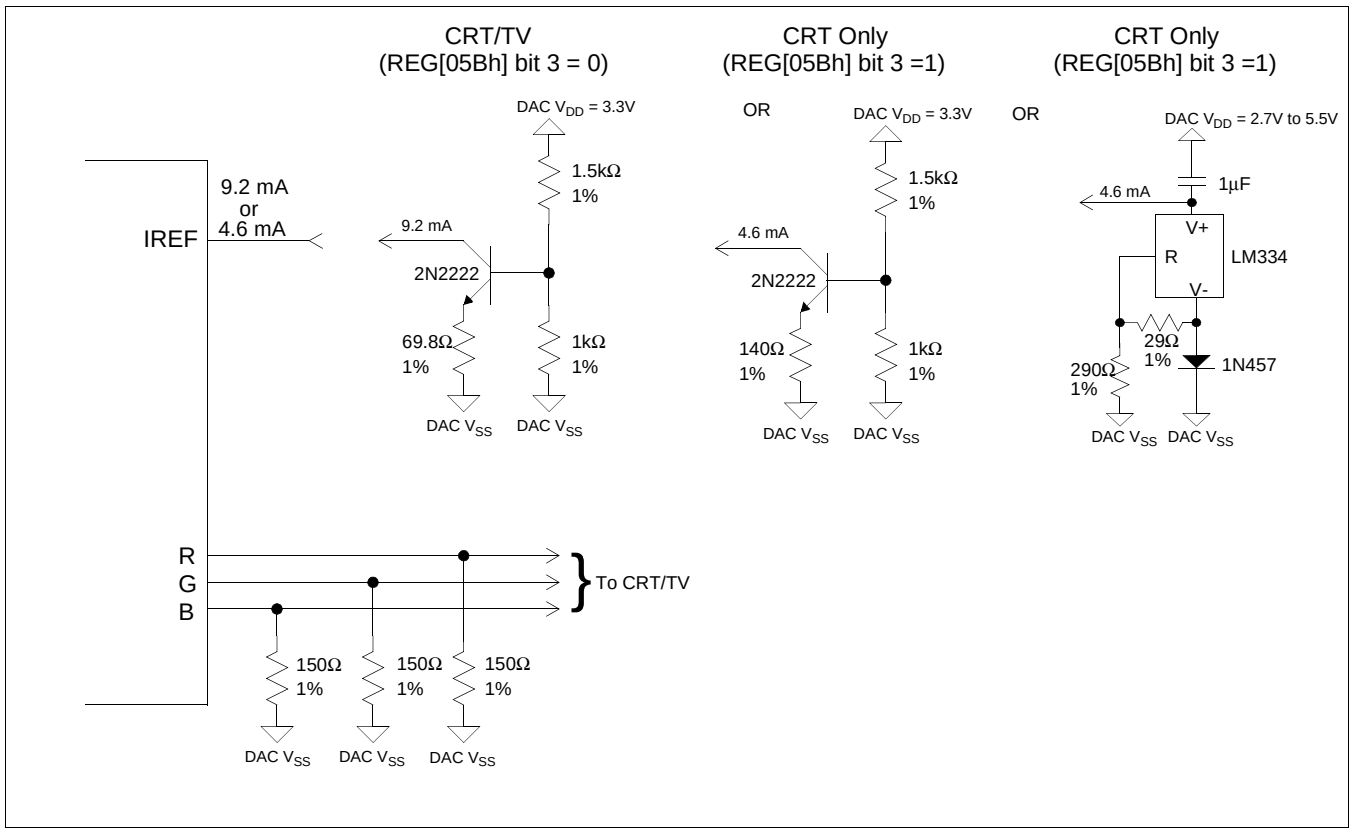

Figure 5-2: External Circuitry for CRT/TV Interface

Note

Example implementation only, individual characteristics of components may affect actual IREF current.

6 D.C. Characteristics

Table 6-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}	Supply Voltage	V_{SS} - 0.3 to 6.0	V
DAC V_{DD}	Supply Voltage	V_{SS} - 0.3 to 6.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-65 to 150	° C
T_{SOL}	Solder Temperature/Time	260 for 10 sec. max at lead	° C

Table 6-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Supply Voltage	V_{SS} = 0 V	2.7	3.0/3.3/5.0	5.5	V
V_{IN}	Input Voltage		V_{SS}		V_{DD}	V
T_{OPR}	Operating Temperature		-40	25	85	° C

Table 6-3: Electrical Characteristics for VDD = 5.0V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions			400	uA
I_{IZ}	Input Leakage Current		-1		1	µA
I_{OZ}	Output Leakage Current		-1		1	µA
V_{OH}	High Level Output Voltage	VDD = min I_{OL} = -4mA (Type1), -8mA (Type2) -12mA (Type3)	V_{DD} - 0.4			V
V_{OL}	Low Level Output Voltage	VDD = min I_{OL} = 4mA (Type1), 8mA (Type2) 12mA (Type3)			0.4	V
V_{IH}	High Level Input Voltage	CMOS level, V_{DD} = max	3.5			V
V_{IL}	Low Level Input Voltage	CMOS level, V_{DD} = min			1.0	V
V_{T+}	High Level Input Voltage	CMOS Schmitt, V_{DD} = 5.0V			4.0	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt, V_{DD} = 5.0V	0.8			V
V_{H1}	Hysteresis Voltage	CMOS Schmitt, V_{DD} = 5.0V	0.3			V
R_{PD}	Pull Down Resistance	$V_I = V_{DD}$	50	100	200	kΩ
C_I	Input Pin Capacitance				12	pF
C_O	Output Pin Capacitance				12	pF
C_{IO}	Bi-Directional Pin Capacitance				12	pF

Table 6-4: Electrical Characteristics for VDD = 3.3V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions			290	uA
I_{IZ}	Input Leakage Current		-1		1	µA
I_{OZ}	Output Leakage Current		-1		1	µA
V_{OH}	High Level Output Voltage	VDD = min I_{OL} = -2mA (Type1), -4mA (Type2) -6mA (Type3)	V_{DD} - 0.3			V
V_{OL}	Low Level Output Voltage	VDD = min I_{OL} = 2mA (Type1), 4mA (Type2) 6mA (Type3)			0.3	V
V_{IH}	High Level Input Voltage	CMOS level, V_{DD} = max	2.2			V
V_{IL}	Low Level Input Voltage	CMOS level, V_{DD} = min			0.8	V
V_{T+}	High Level Input Voltage	CMOS Schmitt, V_{DD} = 3.3V			2.4	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt, V_{DD} = 3.3V	0.6			V
V_{H1}	Hysteresis Voltage	CMOS Schmitt, V_{DD} = 3.3V	0.1			V
R_{PD}	Pull Down Resistance	$V_I = V_{DD}$	90	180	360	kΩ
C_I	Input Pin Capacitance				12	pF
C_O	Output Pin Capacitance				12	pF
C_{IO}	Bi-Directional Pin Capacitance				12	pF

Table 6-5: Electrical Characteristics for VDD = 3.0V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions			260	uA
I_{IZ}	Input Leakage Current		-1		1	µA
I_{OZ}	Output Leakage Current		-1		1	µA
V_{OH}	High Level Output Voltage	VDD = min I_{OL} = -1.8mA (Type1), -3.5mA (Type2) -5mA (Type3)	V_{DD} - 0.3			V
V_{OL}	Low Level Output Voltage	VDD = min I_{OL} = 1.8mA (Type1), 3.5mA (Type2) 5mA (Type3)			0.3	V
V_{IH}	High Level Input Voltage	CMOS level, V_{DD} = max	2.0			V
V_{IL}	Low Level Input Voltage	CMOS level, V_{DD} = min			0.8	V
V_{T+}	High Level Input Voltage	CMOS Schmitt, V_{DD} = 3.0V			2.3	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt, V_{DD} = 3.0V	0.5			V
V_{H1}	Hysteresis Voltage	CMOS Schmitt, V_{DD} = 3.0V	0.1			V
R_{PD}	Pull Down Resistance	$V_I = V_{DD}$	100	200	400	kΩ
C_I	Input Pin Capacitance				12	pF
C_O	Output Pin Capacitance				12	pF
C_{IO}	Bi-Directional Pin Capacitance				12	pF

7 A.C. Characteristics

Conditions: V_{DD} = 3.0V ± 10% and V_{DD} = 5.0V ± 10%
T_A = -40° C to 85° C
T_{rise} and T_{fall} for all inputs must be ≤ 5 ns (10% ~ 90%)
C_L = 50pF (CPU Interface), unless noted
C_L = 100pF (LCD Panel Interface)
C_L = 10pF (Display Memory Interface)
C_L = 10pF (CRT Interface)

7.1 CPU Interface Timing

7.1.1 Generic Timing

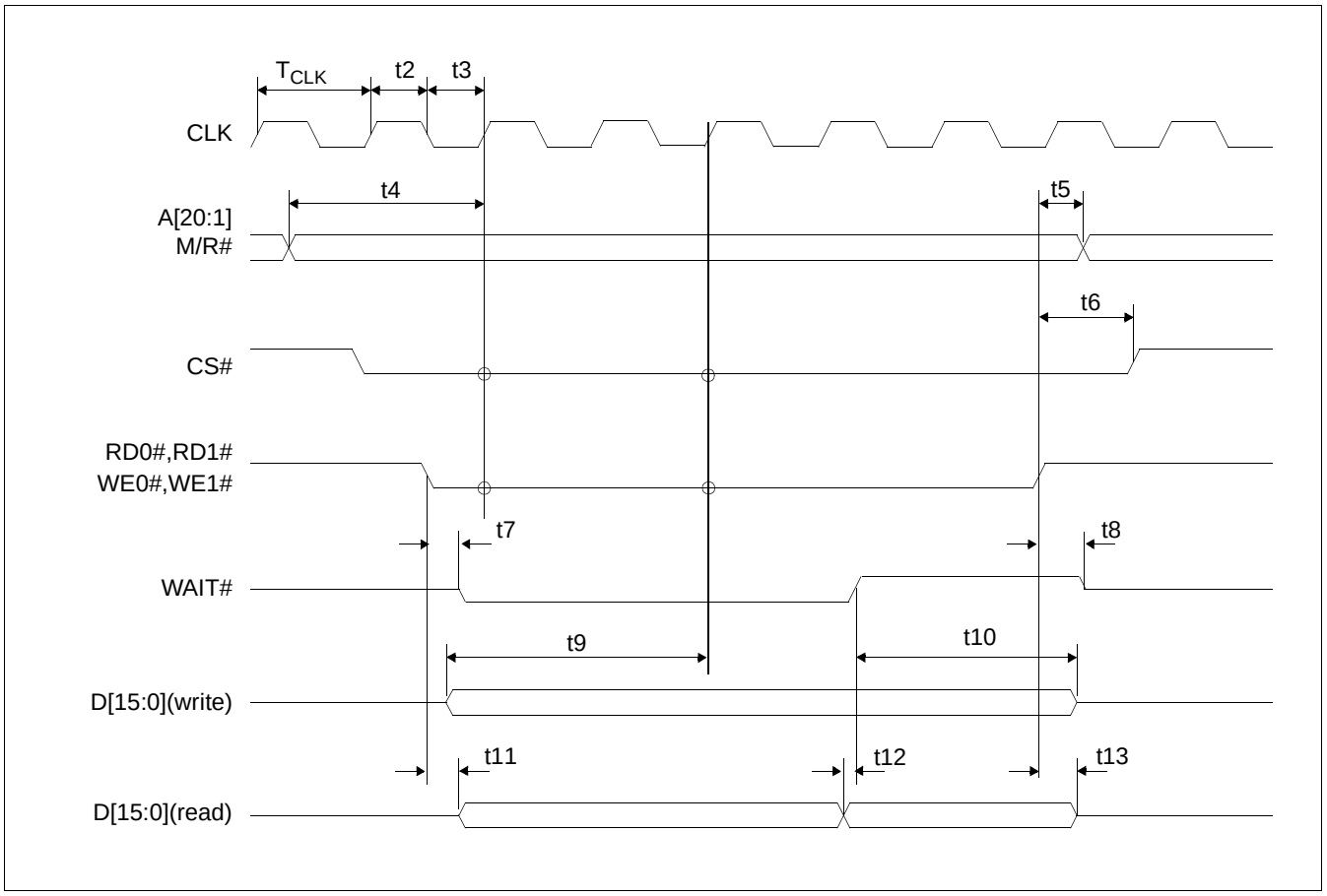

Figure 7-1: Generic Timing

Note
The above timing diagram is not applicable if MD12 = 1 (BUSCLK divided by 2).

Table 7-1: Generic Timing

		3.0V		5.0V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{CLK}	Clock frequency		50		50	MHz
T_{CLK}	Clock period	$1/f_{CLK}$		$1/f_{CLK}$		ns
t2	Clock pulse width high	6		6		ns
t3	Clock pulse width low	6		6		ns
t4	A[20:1], M/R# setup to first CLK where CS# = 0 and either RD0#, RD1#= 0 or WE0#, WE1#= 0	4		3		ns
t5	A[20:1], M/R# hold from rising edge of either RD0#, RD1# or WE0#, WE1#	0		0		ns
t6	CS# hold from rising edge of either RD0#, RD1# or WE0#, WE1#	0		0		ns
t7	Falling edge of either RD0#, RD1# or WE0#, WE1# to WAIT# driven low	4	21	3	13	ns
t8	Rising edge of either RD0#, RD1# or WE0#, WE1# to WAIT# tri-state	3	14	2	7	ns
t9	D[15:0] setup to third CLK where CS# = 0 and WE0#, WE1# = 0 (write cycle)	0		0		ns
t10	D[15:0] hold (write cycle)	0		0		ns
t11	Falling edge RD0#, RD1# to D[15:0] driven (read cycle)	3		3		ns
t12	D[15:0] setup to rising edge WAIT# (read cycle)	0		0		ns
t13	Rising edge of RD0#, RD1# to D[15:0] tri-state (read cycle)	7	31	4	15	ns

7.1.2 Hitachi SH-4 Interface Timing

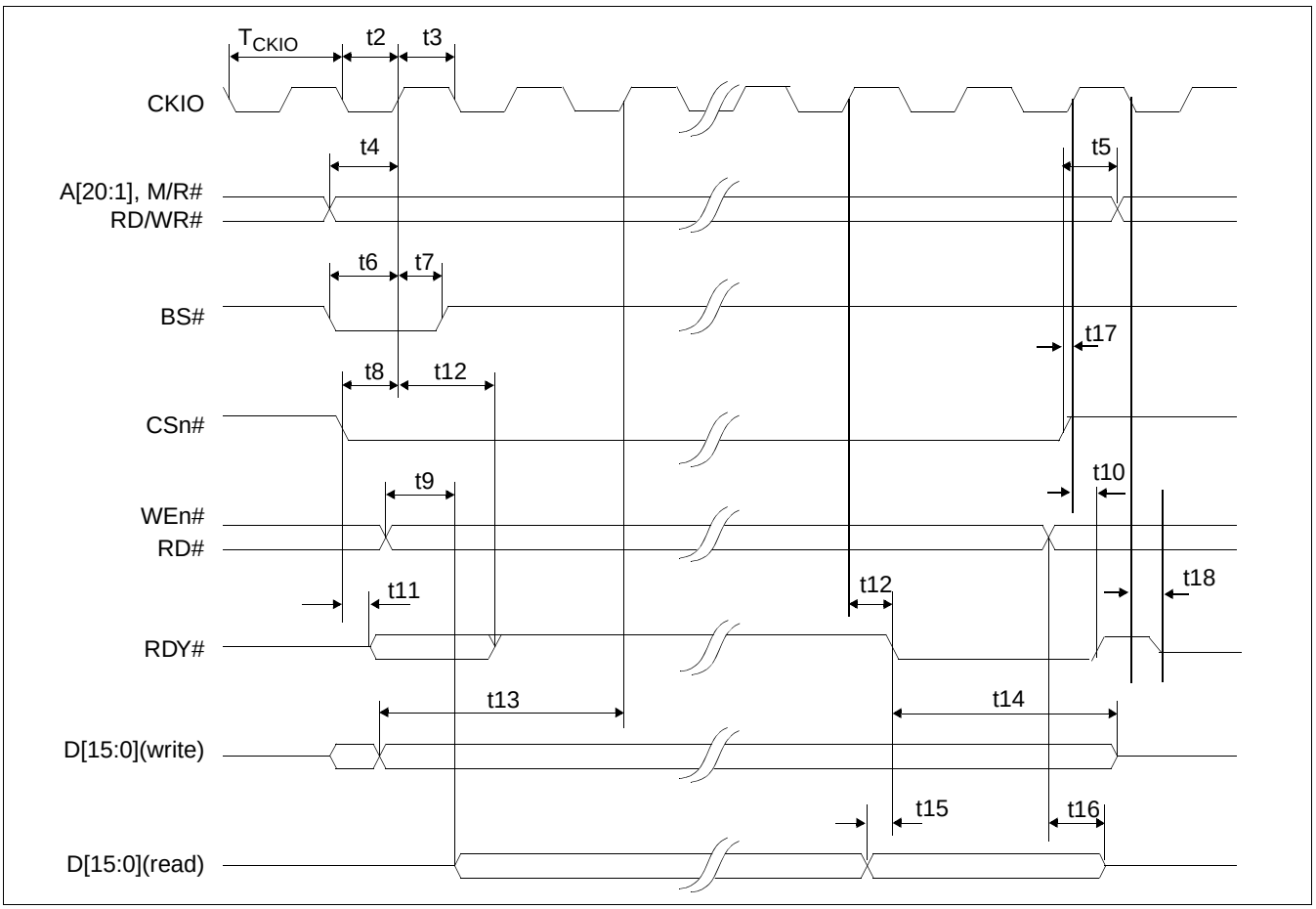

Figure 7-2: Hitachi SH-4 Timing

Note
BUSCLK cannot be divided by 2 in SH-4 interface mode. MD12 must be set to 0 (BUSCLK input is not divided).

Note
The SH-4 Wait State Control Register for the area in which the S1D13506 resides must be set to a non-zero value. The SH-4 read-to-write idle cycle transition must be set to a non-zero value (with reference to BUSCLK).

Table 7-2: Hitachi SH-4 Timing

		3.0V[1]		5.0V[2]		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{CKIO}	Clock frequency	0	66	0	66	MHz
T_{CKIO}	Clock period	$1/f_{CKIO}$		$1/f_{CKIO}$		
t2	Clock pulse width low	6		16		ns
t3	Clock pulse width high	6		6		ns
t4	A[20:1], M/R#, RD/WR# setup to CKIO	4		3		ns
t5	A[20:1], M/R#, RD/WR# hold from CSn#	0		0		ns
t6	BS# setup	4		3		ns
t7	BS# hold	3		2		ns
t8	CSn# setup	3		2		ns
t9	Falling edge RD# to D[15:0] driven	3		3		ns
t10	CKIO to RDY# high	4	21	3	13	ns
t11	Falling edge CSn# to RDY# driven	3	11	2	7	ns
t12	CKIO to RDY# delay	4	20	3	13	ns
t13	D[15:0] setup to 2nd CKIO after BS# (write cycle)	0		0		ns
t14	D[15:0] hold (write cycle)	0		0		ns
t15	D[15:0] valid to RDY# falling edge (read cycle)	0		0		ns
t16	Rising edge RD# to D[15:0] tri-state (read cycle)	6	30	3	16	ns
t17	CSn# high setup to CKIO	3		2		ns
t18	Falling edge CKIO to RDY# tri-state	3	14	2	10	ns

1. Two software WAIT states are required.
2. One software WAIT state is required.

7.1.3 Hitachi SH-3 Interface Timing

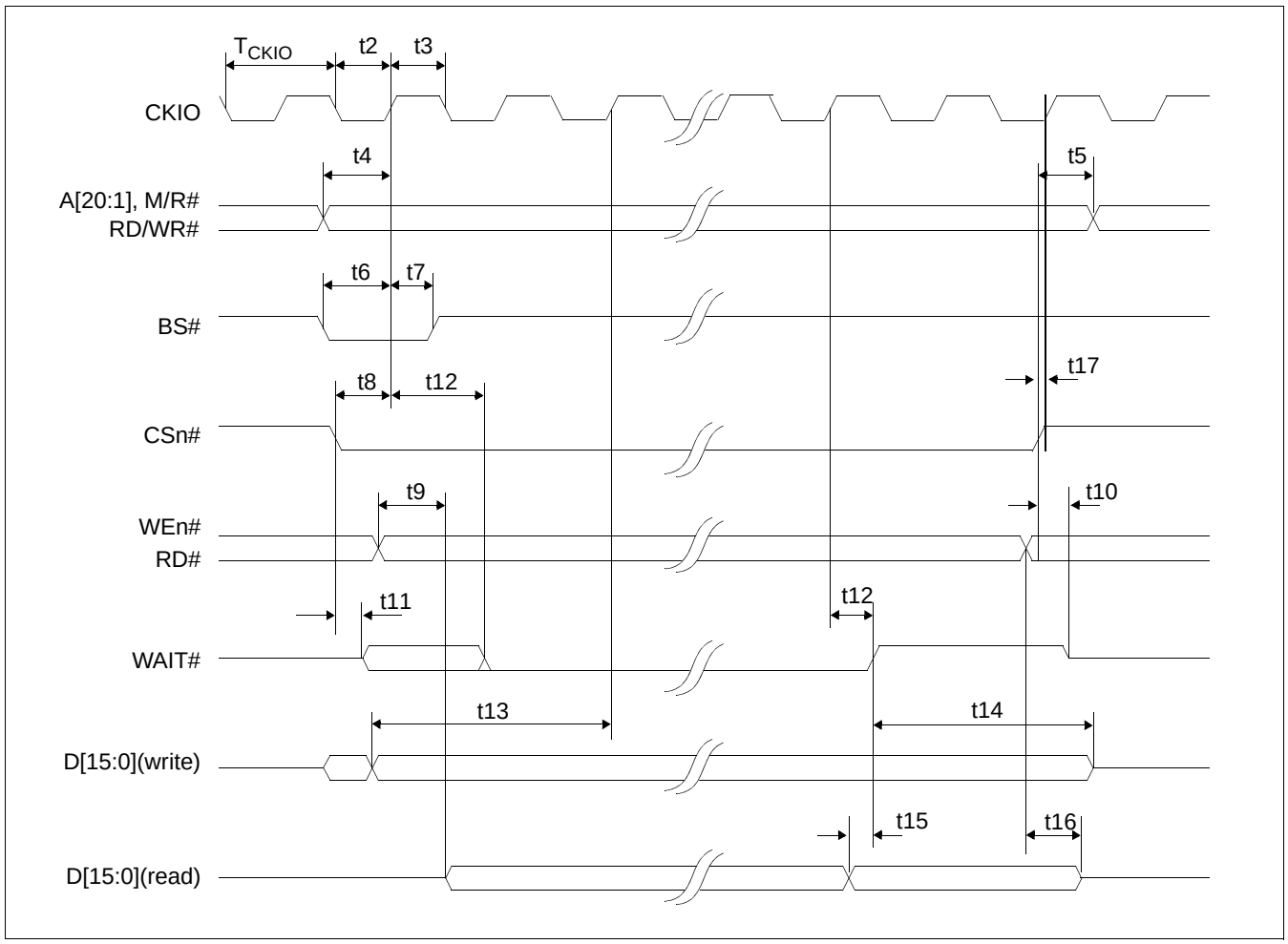

Figure 7-3: Hitachi SH-3 Timing

Note

BUSCLK cannot be divided by 2 in SH-3 interface mode. MD12 must be set to 0 (BUSCLK input is not divided).

Note

The SH-3 Wait State Control Register for the area in which the S1D13506 resides must be set to a non-zero value.

Table 7-3: Hitachi SH-3 Timing

		3.0V[1]		5.0V[2]		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{CKIO}	Clock frequency		66		66	MHz
T_{CKIO}	Clock period	$1/f_{CKIO}$		$1/f_{CKIO}$		ns
t2	Clock pulse width low	6		6		ns
t3	Clock pulse width high	6		6		ns
t4	A[20:1], M/R#, RD/WR# setup to CKIO	4		3		ns
t5	A[20:1], M/R#, RD/WR# hold from CSn#	0		0		ns
t6	BS# setup	4		3		ns
t7	BS# hold	3		2		ns
t8	CSn# setup	3		3		ns
t9	Falling edge RD# to D[15:0] driven	3		2		ns
t10	Rising edge CSn# to WAIT# tri-state	2	10	1	6	ns
t11	Falling edge CSn# to WAIT# driven	3	16	2	10	ns
t12	CKIO to WAIT# delay	4	20	3	13	ns
t13	D[15:0] setup to 2nd CKIO after BS# (write cycle)	0		0		ns
t14	D[15:0] hold (write cycle)	0		0		ns
t15	D[15:0] valid to WAIT# rising edge (read cycle)	0		0		ns
t16	Rising edge RD# to D[15:0] tri-state (read cycle)	6	30	3	15	ns
t17	CSn# high setup to CKIO	3		2		ns

1. Two software WAIT states are required when f_{CKIO} is greater than 33MHz.
2. One software WAIT state is required when f_{CKIO} is greater than 33MHz.

7.1.4 MIPS/ISA Interface Timing (e.g. NEC VR41xx)

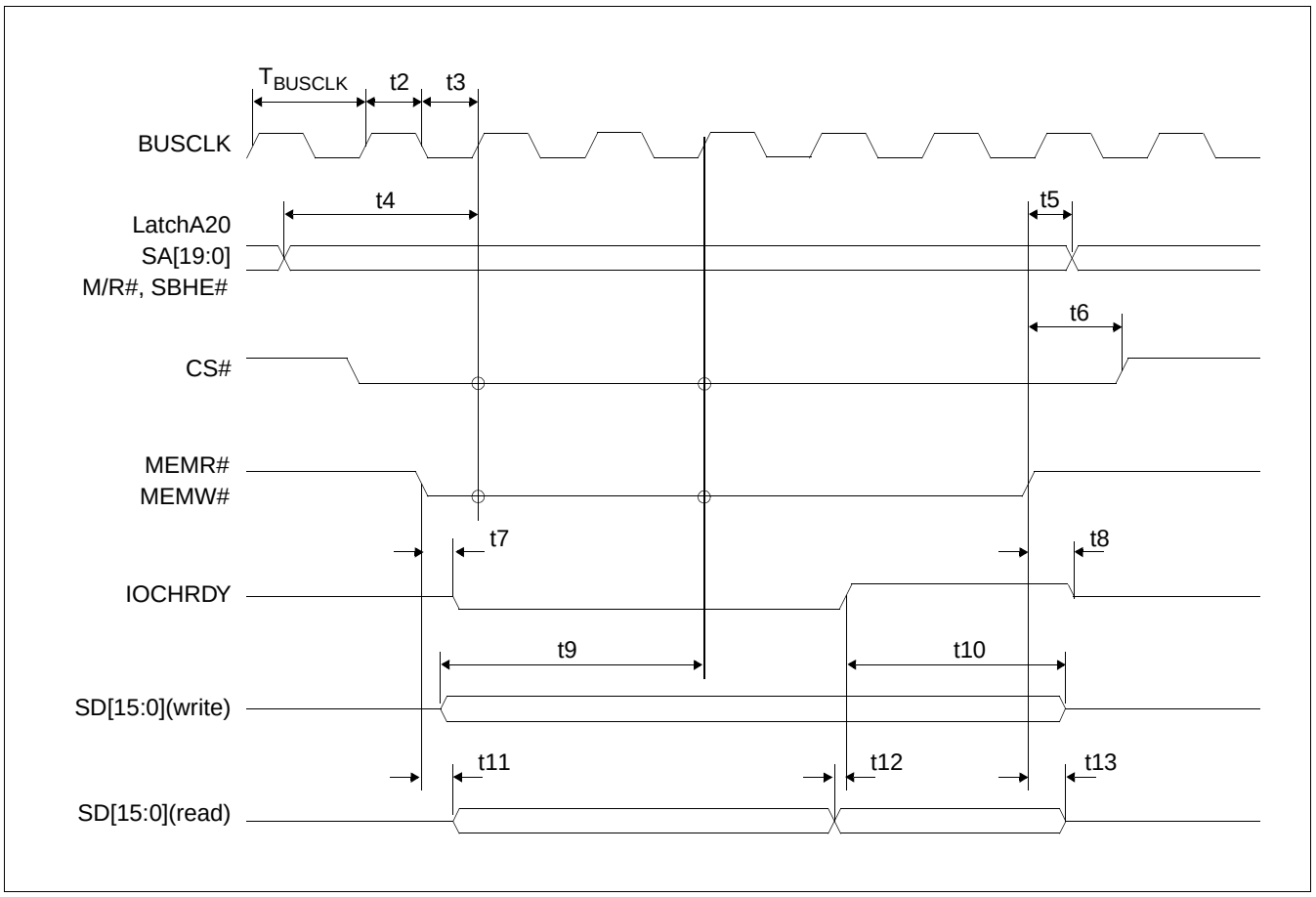

Figure 7-4: MIPS/ISA Timing

Note

The above timing diagram is not applicable if MD12 = 1 (BUSCLK divided by 2).

Table 7-4: MIPS/ISA Timing

		3.0V		5.0V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{BUSCLK}	Clock frequency		50		50	MHz
T_{BUSCLK}	Clock period	$1/f_{BUSCLK}$		$1/f_{BUSCLK}$		ns
t2	Clock pulse width high	6		6		ns
t3	Clock pulse width low	6		6		ns
t4	LatchA20, SA[19:0], M/R#, SBHE# setup to first BUSCLK where CS# = 0 and either MEMR# = 0 or MEMW# = 0	4		3		ns
t5	LatchA20, SA[19:0], M/R#, SBHE# hold from rising edge of either MEMR# or MEMW#	0		0		ns
t6	CS# hold from rising edge of either MEMR# or MEMW#	0		0		ns
t7	Falling edge of either MEMR# or MEMW# to IOCHRDY# driven low	2	17	2	10	ns
t8	Rising edge of either MEMR# or MEMW# to IOCHRDY# tri-state	2	12	1	7	ns
t9	SD[15:0] setup to third BUSCLK where CS# = 0 MEMW# = 0 (write cycle)	0		0		ns
t10	SD[15:0] hold (write cycle)	0		0		ns
t11	Falling edge MEMR# to SD[15:0] driven (read cycle)	4		3		ns
t12	SD[15:0] setup to rising edge IOCHRDY# (read cycle)	0		0		ns
t13	Rising edge of MEMR# toSD[15:0] tri-state (read cycle)	7	31	4	15	ns

7.1.5 Motorola MC68K Bus 1 Interface Timing (e.g. MC68000)

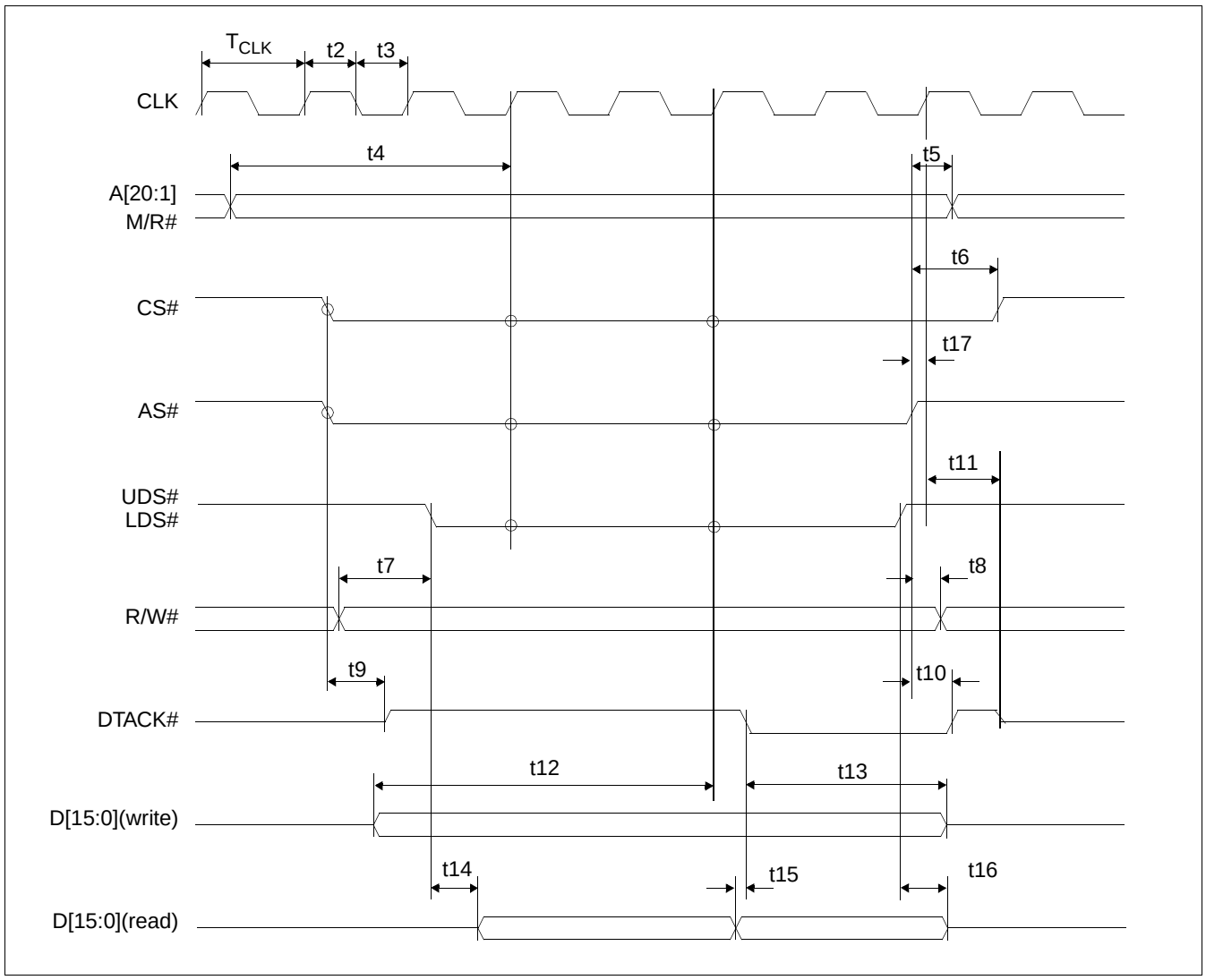

Figure 7-5: Motorola MC68000 Timing

Note

The above timing diagram is not applicable if MD12 = 1 (BUSCLK divided by 2).

Table 7-5: Motorola MC68000 Timing

		3.0V		5.0V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{CLK}	Clock frequency		50		50	MHz
T_{CLK}	Clock period	$1/f_{CLK}$		$1/f_{CLK}$		ns
t2	Clock pulse width high	6		6		ns
t3	Clock pulse width low	6		6		ns
t4	A[20:1], M/R# setup to first CLK where CS# = 0 AS# = 0, and either UDS#=0 or LDS# = 0	5		3		ns
t5	A[20:1], M/R# hold from AS#	0		0		ns
t6	CS# hold from AS#	0		0		ns
t7	R/W# setup to before to either UDS#=0 or LDS# = 0	10		10		ns
t8	R/W# hold from AS#	0		0		ns
t9	AS# = 0 and CS# = 0 to DTACK# driven high	1		1		ns
t10	AS# high to DTACK# high	4	18	3	11	ns
t11	First BCLK where AS# = 1 to DTACK# high impedance	3	15	2	10	ns
t12	D[15:0] valid to third CLK where CS# = 0 AS# = 0, and either UDS#=0 or LDS# = 0 (write cycle)	0		0		ns
t13	D[15:0] hold from falling edge of DTACK# (write cycle)	0		0		ns
t14	Falling edge of UDS#=0 or LDS# = 0 to D[15:0] driven (read cycle)	3		3		ns
t15	D[15:0] valid to DTACK# falling edge (read cycle)	0		0		ns
t16	UDS# and LDS# high to D[15:0] invalid/high impedance (read cycle)	6	31	4	15	ns
t17	AS# high setup to CLK	4		3		ns

7.1.6 Motorola MC68K Bus 2 Interface Timing (e.g. MC68030)

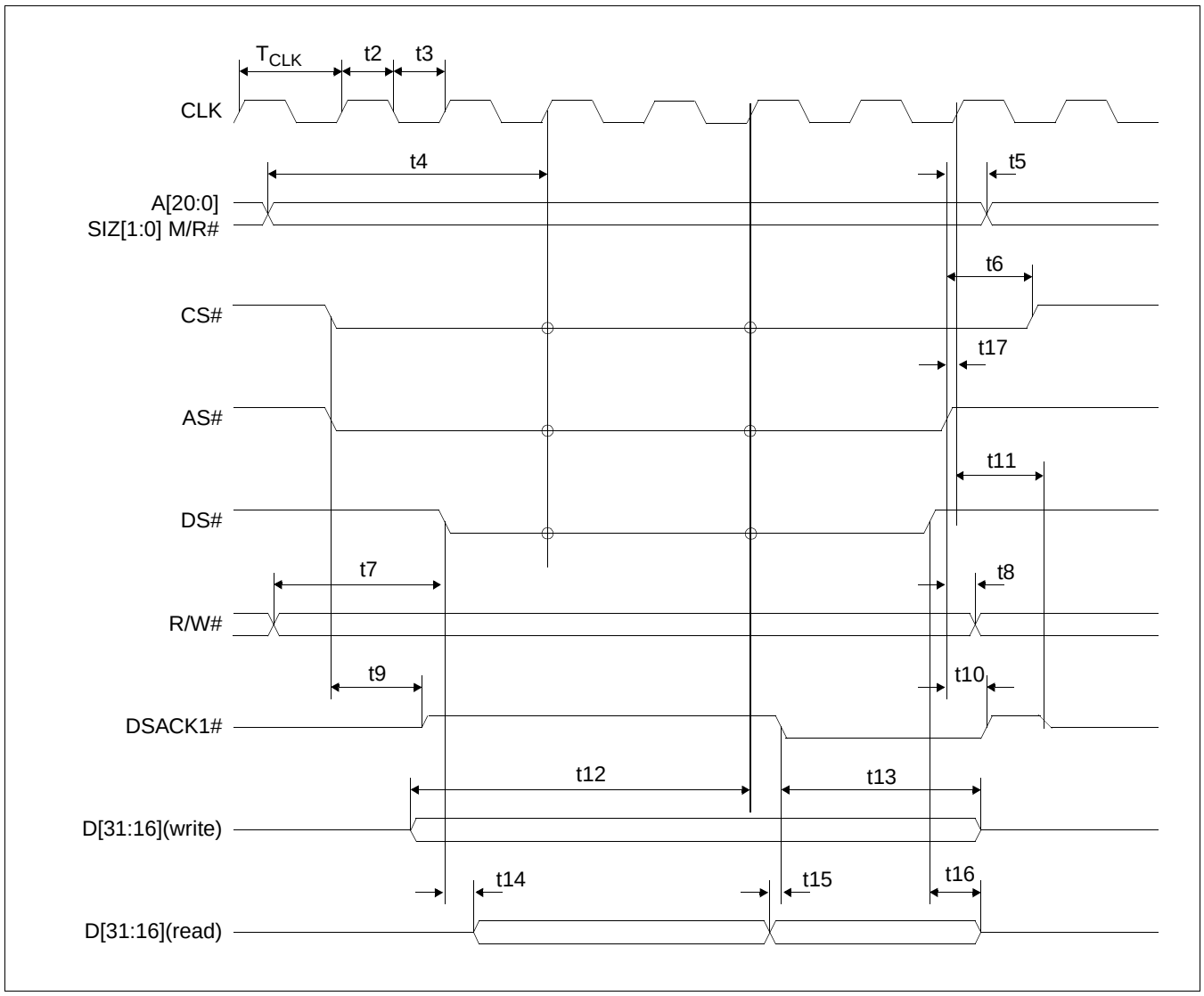

Figure 7-6: Motorola MC68030 Timing

Note

The above timing diagram is not applicable if MD12 = 1 (BUSCLK divided by 2).

Table 7-6: Motorola MC68030 Timing

		3.0V		5.0V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{CLK}	Clock frequency		50		50	MHz
T_{CLK}	Clock period	$1/f_{CLK}$		$1/f_{CLK}$		ns
t2	Clock pulse width high	6		6		ns
t3	Clock pulse width low	6		6		ns
t4	A[20:0], SIZ[1:0], M/R# setup to first CLK where CS# = 0, AS# = 0, and DS# = 0	5		3		ns
t5	A[20:0], SIZ[1:0], M/R# hold from AS#	0		0		ns
t6	CS# hold from AS#	0		0		ns
t7	R/W# setup to DS#	10		10		ns
t8	R/W# hold from AS#	0		0		ns
t9	AS# = 0 and CS# = 0 to DSACK1# driven high	1		1		ns
t10	AS# high to DSACK1# high	4	18	3	12	ns
t11	First BCLK where AS# = 1 to DSACK1# high impedance	3	15	2	14	ns
t12	D[31:16] valid to third CLK where CS# = 0, AS# = 0, and DS# = 0 (write cycle)	0		0		ns
t13	D[31:16] hold from falling edge of DSACK1# (write cycle)	0		0		ns
t14	Falling edge of DS# = 0 to D[31:16] driven (read cycle)	3		3		ns
t15	D[31:16] valid to DSACK1# falling edge (read cycle)	0		0		ns
t16	DS# high to D[31:16] invalid/high impedance (read cycle)	6	31	4	15	ns
t17	AS# high setup to CLK	4		3		ns

7.1.7 Motorola PowerPC Interface Timing (e.g. MPC8xx, MC68040, Coldfire)

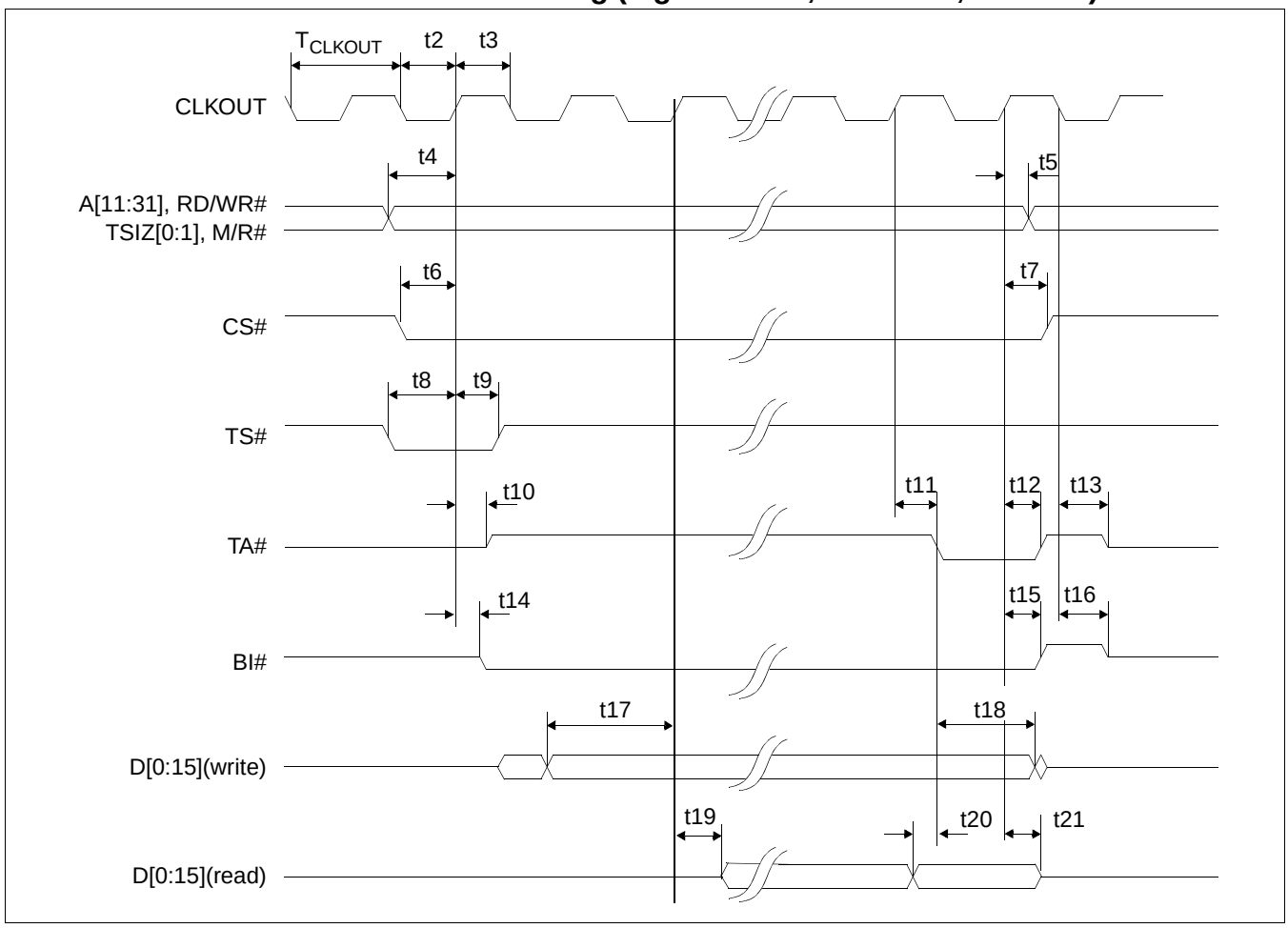

Figure 7-7: Motorola PowerPC Timing

Note

BUSCLK cannot be divided by 2 in PowerPC interface mode. MD12 must be set to 0 (BUSCLK input is not divided).

Table 7-7: Motorola PowerPC Timing

		3.0V		5.0V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{CLKOUT}	Clock frequency		45		50	MHz
T_{CLKOUT}	Clock period	$1/f_{CLKOUT}$		$1/f_{CLKOUT}$		ns
t2	Clock pulse width low	6		6		ns
t3	Clock pulse width high	6		6		ns
t4	AB[11:31], RD/WR#, TSIZ[0:1], M/R# setup	0		0		ns
t5	AB[11:31], RD/WR#, TSIZ[0:1], M/R# hold	0		0		ns
t6	CS# setup	1		0		ns
t7	CS# hold	0		1		ns
t8	TS# setup	1		1		ns
t9	TS# hold	0		1		ns
t10	CLKOUT to TA# driven	2		1		ns
t11	CLKOUT to TA# low	3	15	2	9	ns
t12	CLKOUT to TA# high	3	16	2	10	ns
t13	negative edge CLKOUT to TA# tri-state	3	14	2	9	ns
t14	CLKOUT to BI# driven	3	13	2	8	ns
t15	CLKOUT to BI# high	3	13	2	8	ns
t16	negative edge CLKOUT to BI# tri-state	3	14	2	8	ns
t17	DB[15:0] setup to 2nd CLKOUT after TS# = 0 (write cycle)	0		0		ns
t18	DB[15:0] hold (write cycle)	0		0		ns
t19	CLKOUT to DB driven (read cycle)	3		2		ns
t20	DB[15:0] valid to TA# falling edge (read cycle)	0		0		ns
t21	CLKOUT to DB[15:0] tri-state (read cycle)	3	14	2	9	ns

Note

Output pin loading on DB[15:0], TA#, BI# is 10pF.

7.1.8 PC Card Timing (e.g. StrongARM)

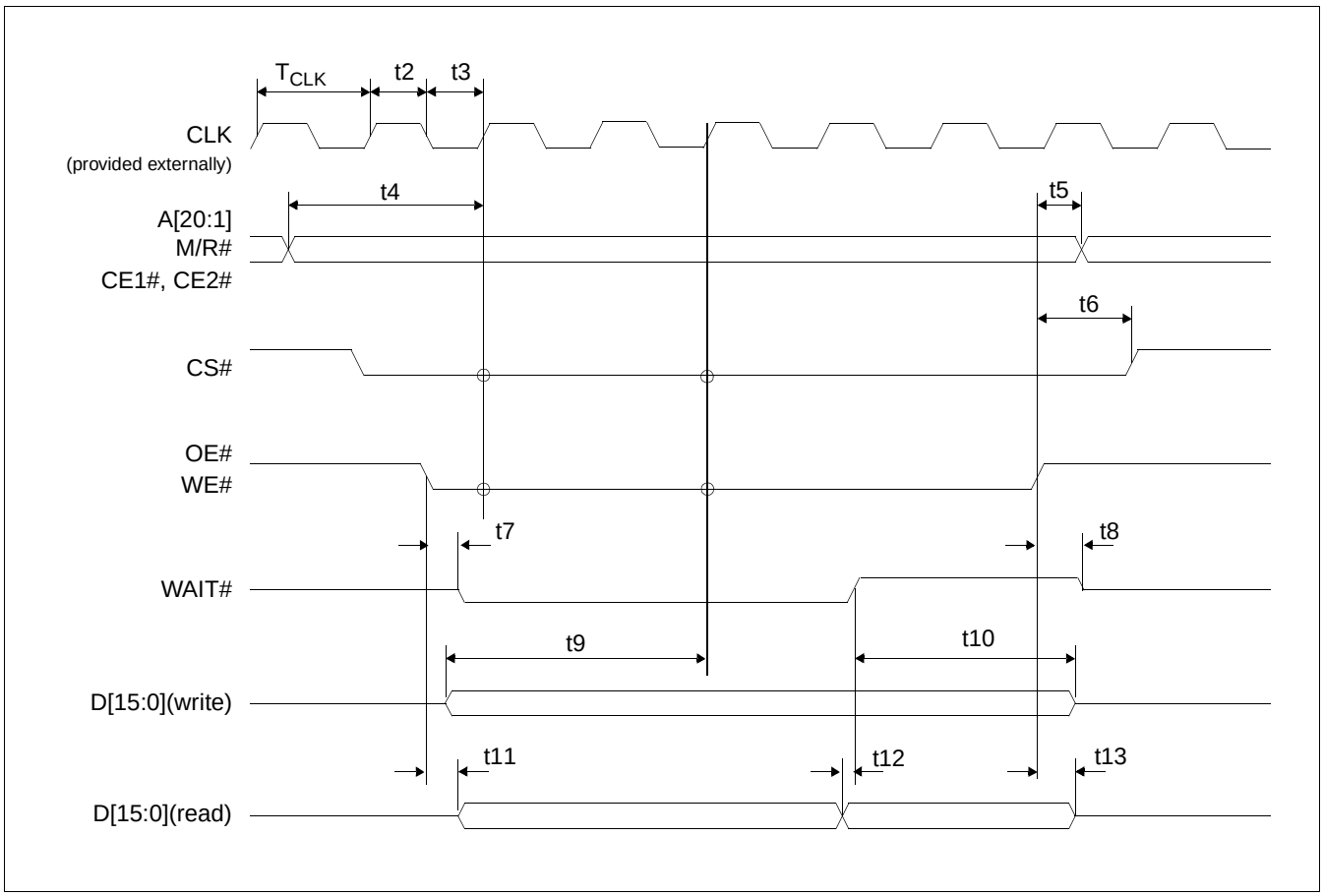

Figure 7-8: PC Card Timing

Note

The above timing diagram is not applicable if MD12 = 1 (BUSCLK divided by 2).

Table 7-8: PC Card Timing

		3.0V		5.0V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{CLK}	Clock frequency		50		50	MHz
T_{CLK}	Clock period	$1/f_{CLK}$		$1/f_{CLK}$		ns
t2	Clock pulse width high	6		6		ns
t3	Clock pulse width low	6		6		ns
t4	A[20:1], M/R# setup to first CLK where CE1# = 0 or CE2# = 0 **and** either OE# = 0 or WE# = 0	4		3		ns
t5	A[20:1], M/R# hold from rising edge of either OE# or WE#	0		0		ns
t6	CS# hold from rising edge of either OE# or WE#	0		0		ns
t7	Falling edge of either OE# or WE# to WAIT# driven low	2	21	2	9	ns
t8	Rising edge of either OE# or WE# to WAIT# tri-state	3	14	2	9	ns
t9	D[15:0] setup to third CLK where CE1# = 0, CE2# = 0 and WE# = 0 (write cycle)	0		0		ns
t10	D[15:0] hold (write cycle)	0		0		ns
t11	Falling edge OE# to D[15:0] driven (read cycle)	10		8		ns
t12	D[15:0] setup to rising edge WAIT# (read cycle)	0		0		ns
t13	Rising edge of OE# to D[15:0] tri-state (read cycle)	7	34	5	17	ns

7.1.9 Philips Interface Timing (e.g. PR31500/PR31700)

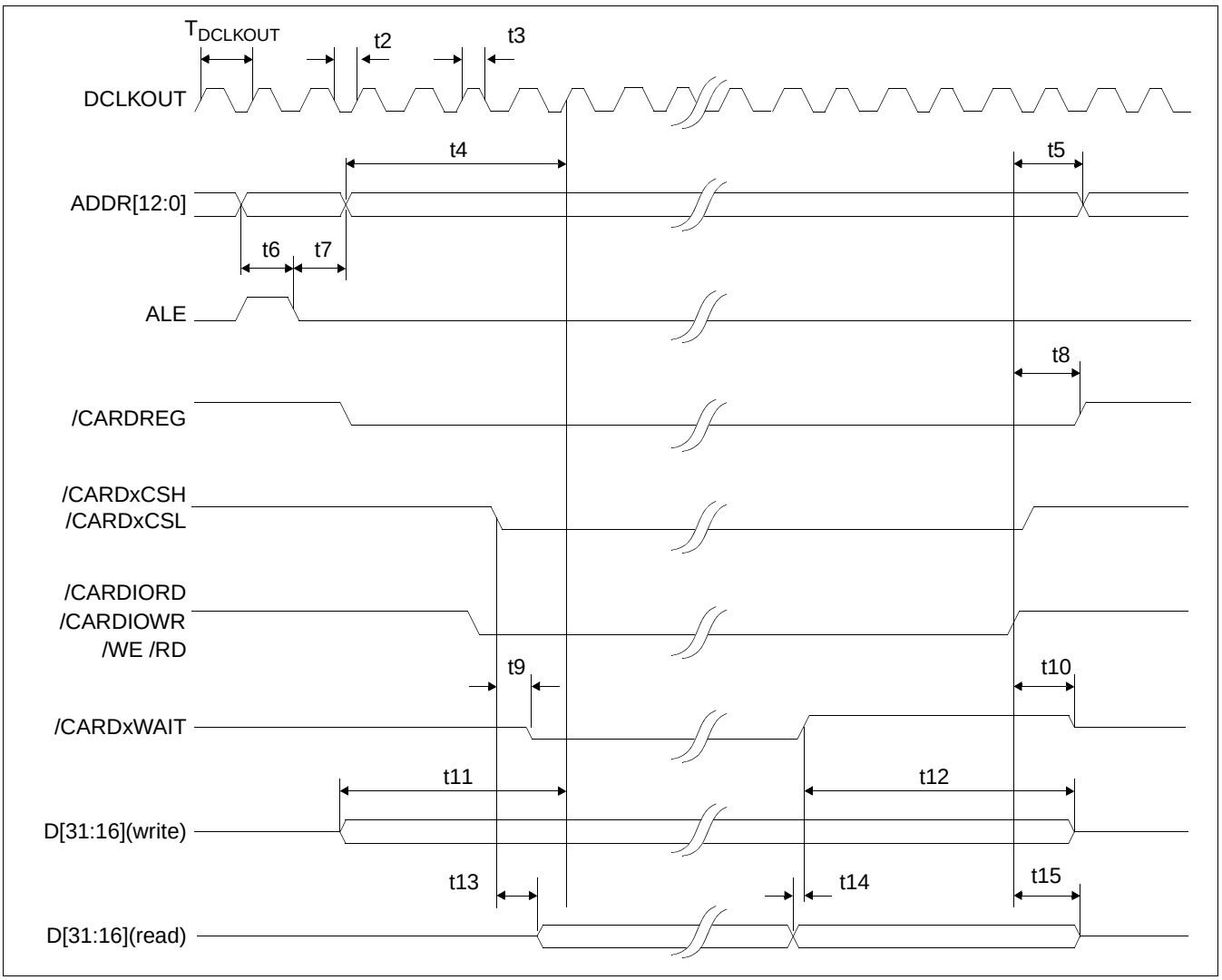

Figure 7-9: Philips Timing

Table 7-9: Philips Timing

		3.0V		5.0V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
$f_{DCLKOUT}$	Clock frequency		75		75	MHz
$T_{DCLKOUT}$	Clock period	$1/f_{DCLKOUT}$		$1/f_{DCLKOUT}$		ns
t2	Clock pulse width low	6		6		ns
t3	Clock pulse width high	6		6		ns
t4	ADDR[12:0] setup to first CLK of cycle	10		10		ns
t5	ADDR[12:0] hold from command invalid	0		0		ns
t6	ADDR[12:0] setup to falling edge ALE	10		10		ns
t7	ADDR[12:0] hold from falling edge ALE	5		5		ns
t8	/CARDREG hold from command invalid	0		0		ns
t9	Falling edge of chip select to /CARDxWAIT driven	2	14	1	9	ns
t10	Command invalid to /CARDxWAIT tri-state	2	13	2	12	ns
t11	D[31:16] valid to first CLK of cycle (write cycle)	10		10		ns
t12	D[31:16] hold from rising edge of /CARDxWAIT	0		0		
t13	Chip select to D[31:16] driven (read cycle)	4		3		ns
t14	D[31:16] setup to rising edge /CARDxWAIT (read cycle)	0		0		ns
t15	Command invalid to D[31:16] tri-state (read cycle)	7	30	4	16	ns

Note

If BUSCLK exceeds 37.5MHz, it must be divided by 2 using MD12 (see Table 5-6:, “Summary of Power-On/Reset Options,” on page 31).

7.1.10 Toshiba Interface Timing (e.g. TX39xx)

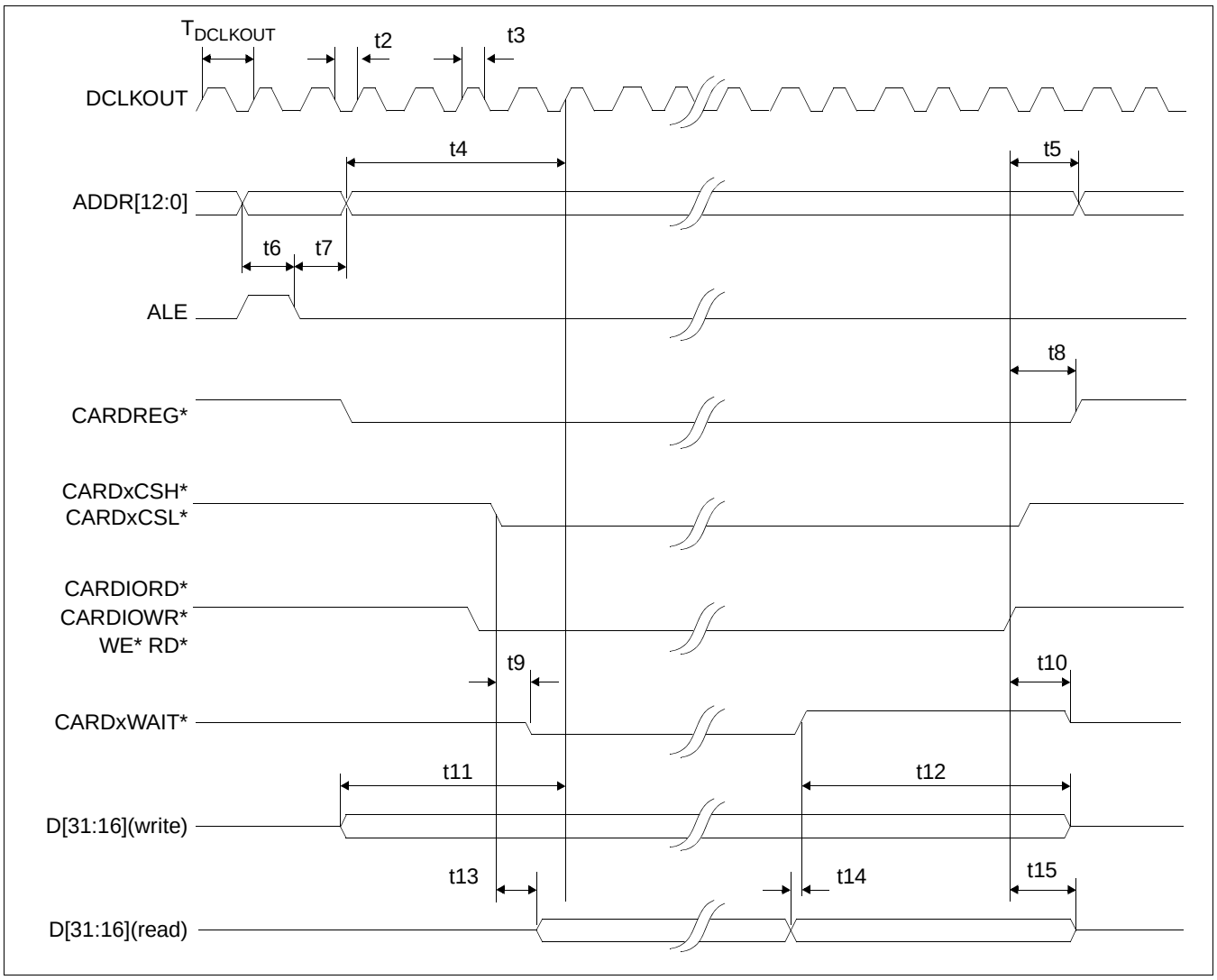

Figure 7-10: Toshiba Timing

Table 7-10: Toshiba Timing

		3.0V		5.0V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
$f_{DCLKOUT}$	Clock frequency		75		75	MHz
$T_{DCLKOUT}$	Clock period	$1/f_{DCLKOUT}$		$1/f_{DCLKOUT}$		ns
t2	Clock pulse width low	6		6		ns
t3	Clock pulse width high	6		6		ns
t4	ADDR[12:0] setup to first CLK of cycle	10		10		ns
t5	ADDR[12:0] hold from command invalid	0		0		ns
t6	ADDR[12:0] setup to falling edge ALE	10		10		ns
t7	ADDR[12:0] hold from falling edge ALE	5		5		ns
t8	CARDREG* hold from command invalid	0		0		ns
t9	Falling edge of chip select to CARDxWAIT* driven	2	14	1	9	ns
t10	Command invalid to CARDxWAIT* tri-state	2	13	2	12	ns
t11	D[31:16] valid to first CLK of cycle (write cycle)	10		10		ns
t12	D[31:16] hold from rising edge of CARDxWAIT*	0		0		
t13	Chip select to D[31:16] driven (read cycle)	4		3		ns
t14	D[31:16] setup to rising edge CARDxWAIT* (read cycle)	0		0		ns
t15	Command invalid to D[31:16] tri-state (read cycle)	7	30	4	16	ns

Note

If BUSCLK exceeds 37.5MHz, it must be divided by 2 using MD12 (see Table 5-6:, “Summary of Power-On/Reset Options,” on page 31).

7.2 Clock Timing

7.2.1 Input Clocks

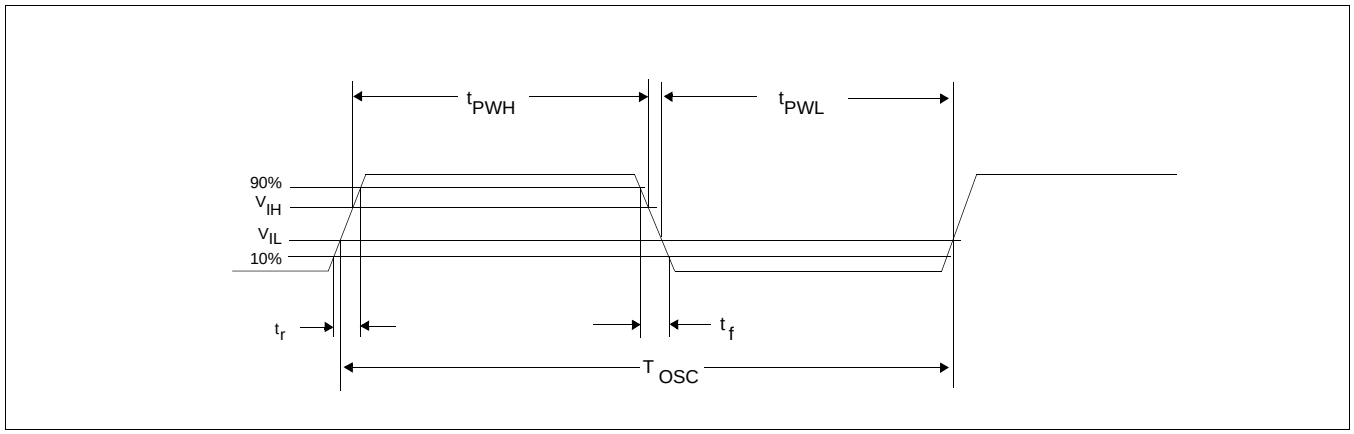

Figure 7-11: CLKI Clock Input Requirements

Table 7-11: Clock Input Requirements for CLKI/CLKI2/BUSCLK divided down internally

Symbol	Parameter	Min	Max	Units
f_{OSC}	Input Clock Frequency		80	MHz
T_{OSC}	Input Clock Period	$1/f_{OSC}$		ns
t_{PWH}	Input Clock Pulse Width High	5.6		ns
t_{PWL}	Input Clock Pulse Width Low	5.6		ns
t_f	Input Clock Fall Time (10% - 90%)		5	ns
t_r	Input Clock Rise Time (10% - 90%)		5	ns

Table 7-12: Clock Input Requirements for CLKI or BUSCLK if used directly for MCLK[1]

Symbol	Parameter	Min	Max	Units
f_{OSC}	Input Clock Frequency		40	MHz
T_{OSC}	Input Clock Period	$1/f_{OSC}$		ns
t_{PWH}	Input Clock Pulse Width High	11.3[1]		ns
t_{PWL}	Input Clock Pulse Width Low	11.3[1]		ns
t_f	Input Clock Fall Time (10% - 90%)		5	ns
t_r	Input Clock Rise Time (10% - 90%)		5	ns

Note

1. MCLK must have a duty cycle of 50% ± 5%.

7.2.2 Internal Clocks

Table 7-13: Internal Clock Requirements

Symbol	Parameter	Min	Max	Units
f_{MCLK}	Memory Clock Frequency	0	40	MHz
$f_{LCD\ PCLK}$	LCD Pixel Clock Frequency	0	40	MHz
$f_{CRT/TV\ PCLK}$	CRT/TV Pixel Clock Frequency	0	Note 1	MHz
$f_{MediaPlug\ Clock}$	MediaPlug Clock Frequency	0	10	MHz

1. The maximum CRT pixel clock is 40MHz.
   The TV pixel clock for NTSC output is fixed at 14.318MHz.
   The TV pixel clock for PAL output is fixed at 17.734MHz.

7.3 Memory Interface Timing

7.3.1 EDO-DRAM Read, Write, Read-Write Timing

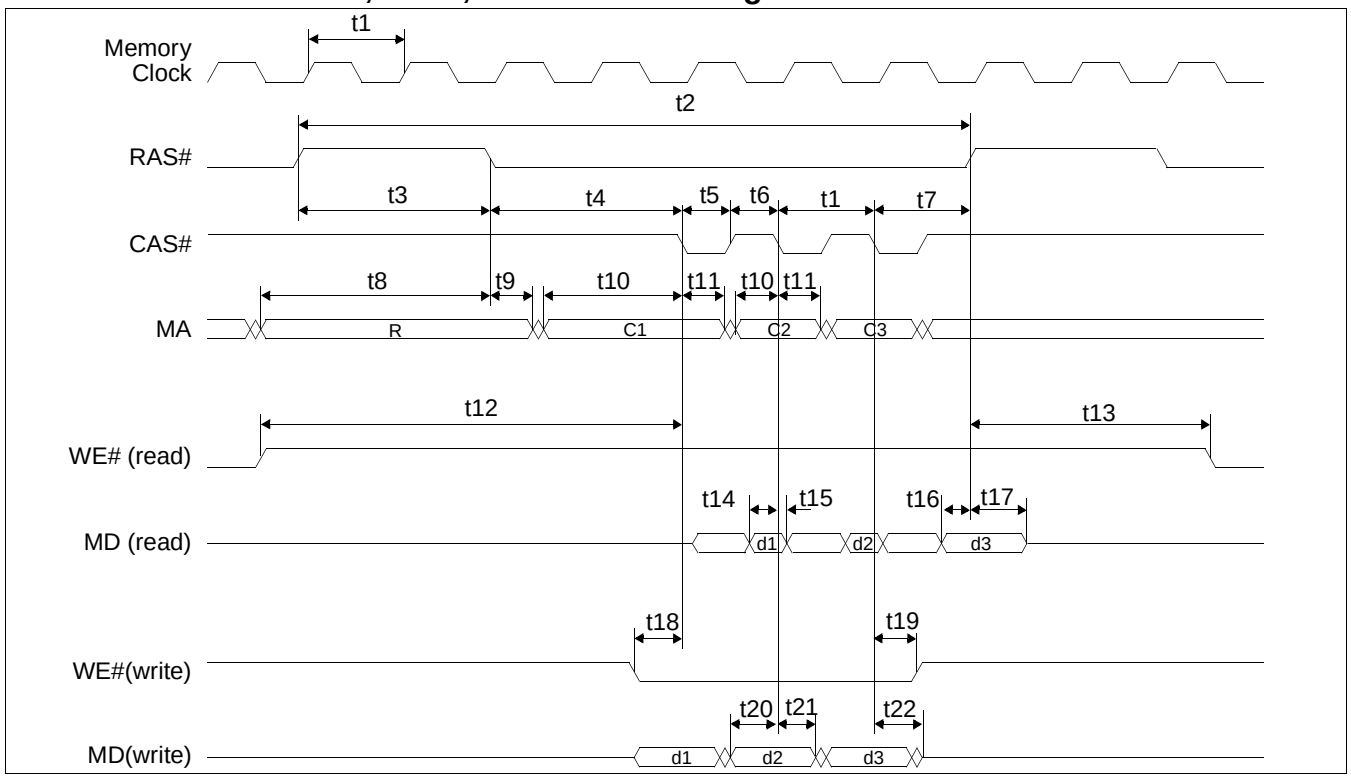

Figure 7-12: EDO-DRAM Page Mode Timing

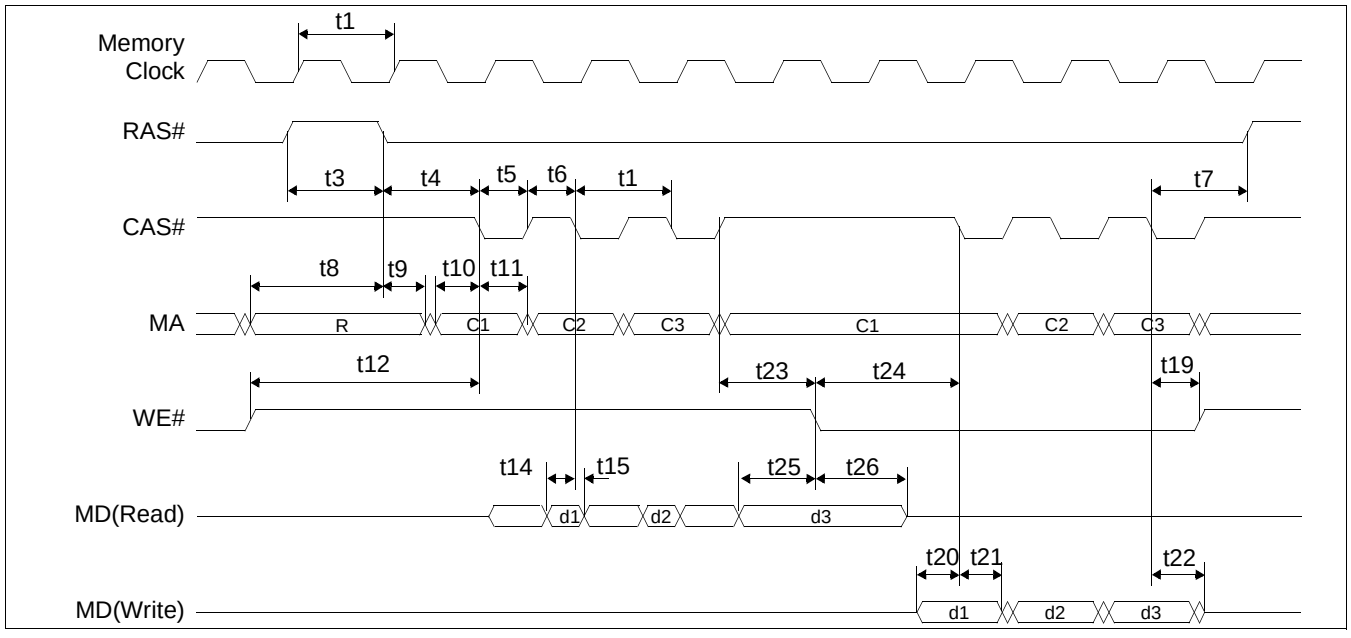

Figure 7-13: EDO-DRAM Read-Write Timing

Table 7-14: EDO-DRAM Read, Write, Read-Write Timing

Symbol	Parameter	Min	Max	Units
t1	Memory clock period	25		ns
t2	Random read or write cycle time (REG[02Bh] bits 1-0 = 00)	5 t1		ns
	Random read or write cycle time (REG[02Bh] bits 1-0 = 01)	4 t1		ns
	Random read or write cycle time (REG[02Bh] bits 1-0 = 10)	3 t1		ns
t3	RAS# precharge time (REG[02Ah] bits 1-0 = 00)	2 t1		ns
	RAS# precharge time (REG[02Ah] bits 1-0 = 01)	1.45 t1		ns
	RAS# precharge time (REG[02Ah] bits 1-0 = 10)	t1		ns
t4	RAS# to CAS# delay time (REG[02Ah] bit 4 = 0 and bits 1-0 = 00 or 10)	2 t1 - 3	2 t1	ns
	RAS# to CAS# delay time (REG[02Ah] bit 4 = 1 and bits 1-0 = 00 or 10)	t1 - 3	t1	ns
	RAS# to CAS# delay time (REG[02Ah] bits 1-0 = 01)	1.45 t1 - 3	1.55 t1	ns
t5	CAS# precharge time	0.45 t1		ns
t6	CAS# pulse width	0.45 t1 - 1		ns
t7	RAS# hold time	t1		ns
t8	Row address setup time (REG[02Ah] bits 1-0 = 00	2.45 t1 - 3		ns
	Row address setup time (REG[02Ah] bits 1-0 = 01)	2 t1 - 3		
	Row address setup time (REG[02Ah] bits 1-0 = 10)	1.45 t1 - 3		
t9	Row address hold time (REG[02Ah] bits 1-0 = 00 or 10)	0.45 t1 - 1		ns
	Row address hold time (REG[02Ah] bits 1-0 = 01)	t1 - 3		ns
t10	Column address setup time	0.45 t1 - 3		ns
t11	Column address hold time	0.45 t1 - 1		ns
t12	Read Command setup (REG[02Ah] bit 4 = 0 and bits 1-0 = 00)	4.45 t1 - 1		ns
	Read Command setup (REG[02Ah] bit 4 = 1 and bits 1-0 = 10)	2.45 t1 - 1		
	Read Command setup (all other REG[02Ah] values)	3.45 t1 - 1		
t13	Read Command hold (REG[02Ah] bit 4 = 0 and bits 1-0 = 00)	3.45 t1 - 1		
	Read Command hold (REG[02Ah] bit 4 = 1 and bits 1-0 = 10)	1.45 t1 - 1		
	Read Command hold (all other REG[02Ah] values)	2.45 t1 - 1		ns
t14	Read data setup referenced from CAS#	4		
t15	Read data hold referenced from CAS#	2		
t16	Last read data setup referenced from RAS#	3		
t17	Bus turn-off from RAS#	2		
t18	Write command setup time	0.45 t1 - 1		ns
t19	Write command hold time	0.45 t1 - 1		ns
t20	Write Data setup time	0.45 t1 - 4		ns
t21	Write Data hold time	0.45 t1		ns
t22	MD tri-state	0.45 t1	0.55 t1 + 19	ns
t23	CAS# to WE# active during read-write cycle	t1		ns
t24	Write command setup during read-write cycle	1.45 t1 - 1		ns
t25	Last read data setup referenced from WE# during read-write cycle	18		ns
t26	Bus tri-state from WE# during read-write cycle	0	t1 - 6	ns

7.3.2 EDO-DRAM CAS Before RAS Refresh Timing

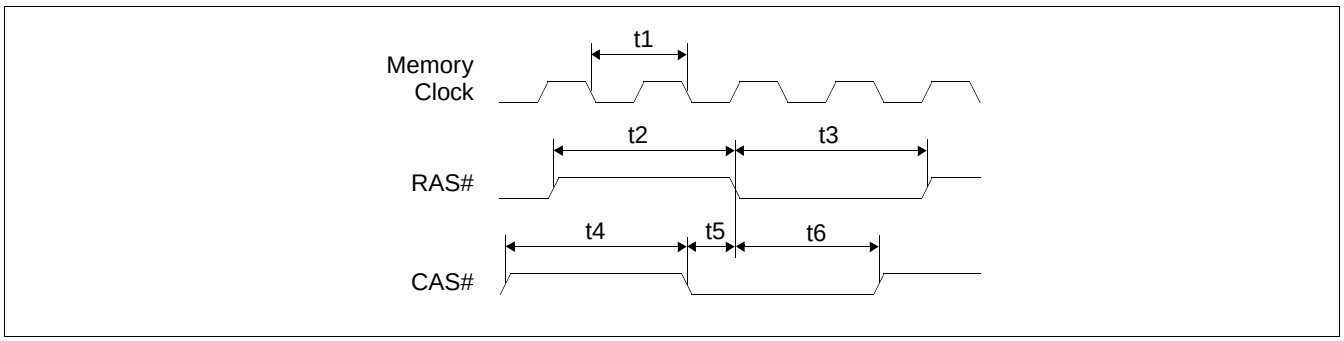

Figure 7-14: EDO-DRAM CAS Before RAS Refresh Timing

Table 7-15: EDO-DRAM CAS Before RAS Refresh Timing

Symbol	Parameter	Min	Max	Units
t1	Memory clock period	25		ns
t2	RAS# precharge time (REG[02Ah] bits 1-0 = 00)	2 t1		ns
	RAS# precharge time (REG[02Ah] bits 1-0 = 01)	1.45 t1		ns
	RAS# precharge time (REG[02Ah] bits 1-0 = 10)	t1		ns
t3	RAS# pulse width (REG[02Bh] bits 1-0 = 00, REG[02Ah] bits 1-0 = 00)	3 t1 - 7		ns
	RAS# pulse width (REG[02Bh] bits 1-0 = 00, REG[02Ah] bits 1-0 = 01)	3.45 t1 - 1		ns
	RAS# pulse width (REG[02Bh] bits 1-0 = 00, REG[02Ah] bits 1-0 = 10)	4 t1 - 7		ns
	RAS# pulse width (REG[02Bh] bits 1-0 = 01, REG[02Ah] bits 1-0 = 00)	2 t1 - 7		ns
	RAS# pulse width (REG[02Bh] bits 1-0 = 01, REG[02Ah] bits 1-0 = 01)	2.45 t1 - 1		ns
	RAS# pulse width (REG[02Bh] bits 1-0 = 01, REG[02Ah] bits 1-0 = 10)	3 t1 - 7		ns
	RAS# pulse width (REG[02Bh] bits 1-0 = 10, REG[02Ah] bits 1-0 = 00)	t1 - 7		ns
	RAS# pulse width (REG[02Bh] bits 1-0 = 10, REG[02Ah] bits 1-0 = 01)	1.45 t1 - 1		ns
	RAS# pulse width (REG[02Bh] bits 1-0 = 10, REG[02Ah] bits 1-0 = 10)	2 t1 - 7		ns
t4	CAS# precharge time (REG[02Ah] bits 1-0 = 00)	2 t1		ns
	CAS# precharge time (REG[02Ah] bits 1-0 = 01 or 10)	t1		ns
t5	CAS# setup time (REG[02Ah] bits 1-0 = 00 or 10)	0.45 t1		ns
	CAS# setup time (REG[02Ah] bits 1-0 = 01)	t1 - 4		ns
t6	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 00, REG[02Ah] bits 1-0 = 00)	2.45 t1 - 4		ns
	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 00, REG[02Ah] bits 1-0 = 01)	3 t1		ns
	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 00, REG[02Ah] bits 1-0 = 10)	3.45 t1 - 4		ns
	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 01, REG[02Ah] bits 1-0 = 00)	1.45 t1 - 4		ns
	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 01, REG[02Ah] bits 1-0 = 01)	2 t1		ns
	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 01, REG[02Ah] bits 1-0 = 10)	2.45 t1 - 4		ns
	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 10, REG[02Ah] bits 1-0 = 00)	0.45 t1 - 4		ns
	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 10, REG[02Ah] bits 1-0 = 01)	t1		ns
	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 10, REG[02Ah] bits 1-0 = 10)	1.45 t1 - 4		ns

7.3.3 EDO-DRAM Self-Refresh Timing

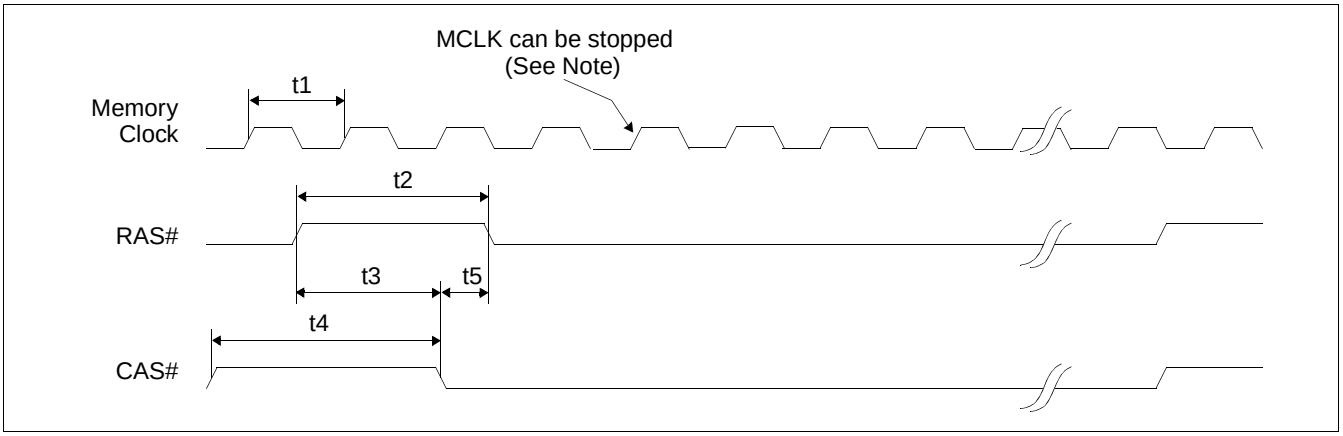

Figure 7-15: EDO - DRAM Self-Refresh Timing

Note
MCLK can be stopped. For timing see Section 7.4.2, “Power Save Mode” on page 71.

Table 7-16: EDO - DRAM Self-Refresh Timing

Symbol	Parameter	Min	Max	Units
t1	Memory clock period	25		ns
t2	RAS# precharge time (REG[02Ah] bits 1-0 = 00)	2 t1		ns
	RAS# precharge time (REG[02Ah] bits 1-0 = 01)	1.45 t1		ns
	RAS# precharge time (REG[02Ah] bits 1-0 = 10)	t1		ns
t3	RAS# to CAS# precharge time (REG[02Ah] bits 1-0 = 00)	1.45 t1		ns
	RAS# to CAS# precharge time (REG[02Ah] bits 1-0 = 01 or 10)	0.45 t1		ns
t4	CAS# precharge time (REG[02Ah] bits 1-0 = 00)	2 t1		ns
	CAS# precharge time (REG[02Ah] bits 1-0 = 01 or 10)	t1		ns
t5	CAS# setup time (REG[02Ah] bits 1-0 = 00 or 10)	0.45 t1		ns
	CAS# setup time (REG[02Ah] bits 1-0 = 01)	t1 - 4		ns

7.3.4 FPM-DRAM Read, Write, Read-Write Timing

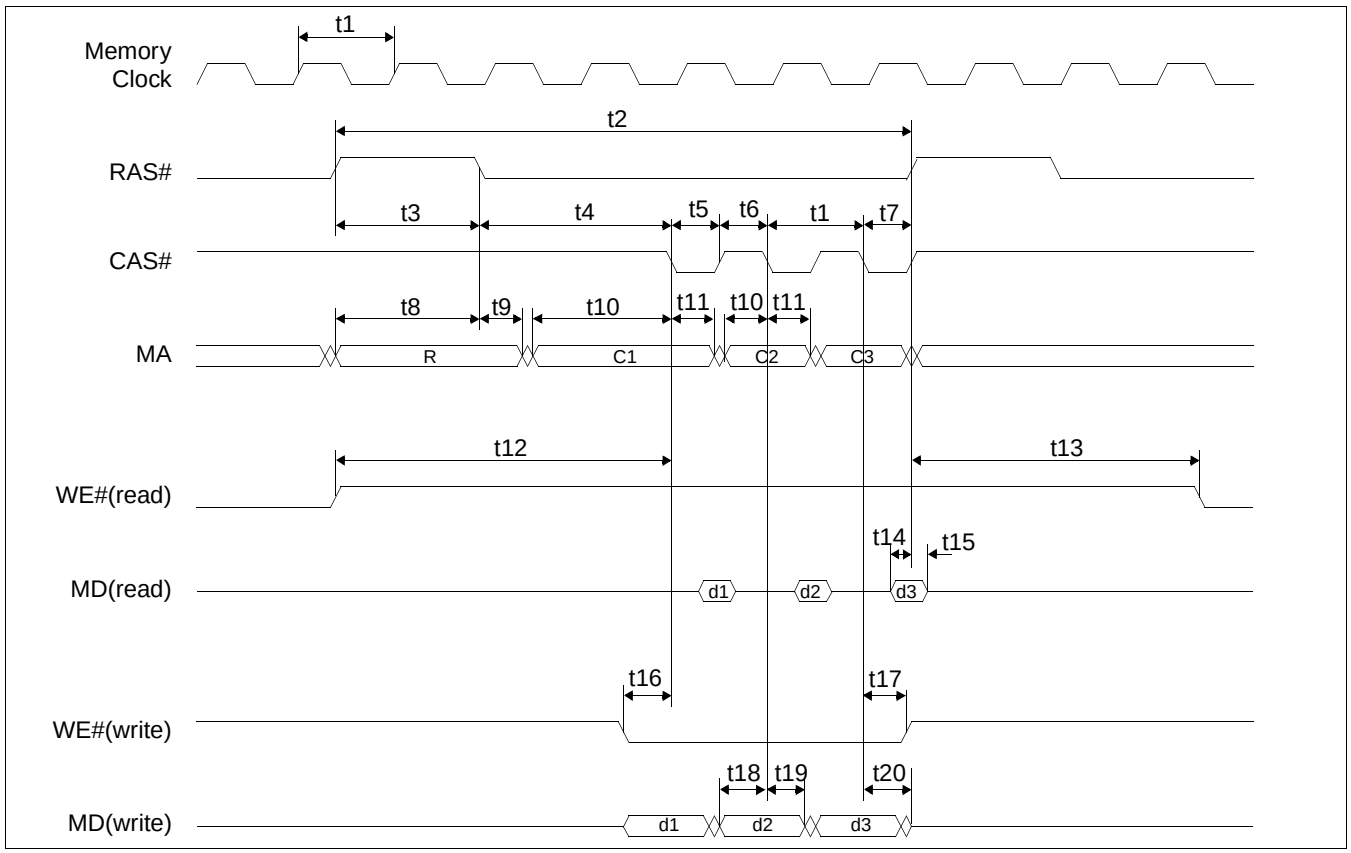

Figure 7-16: FPM-DRAM Page Mode Timing

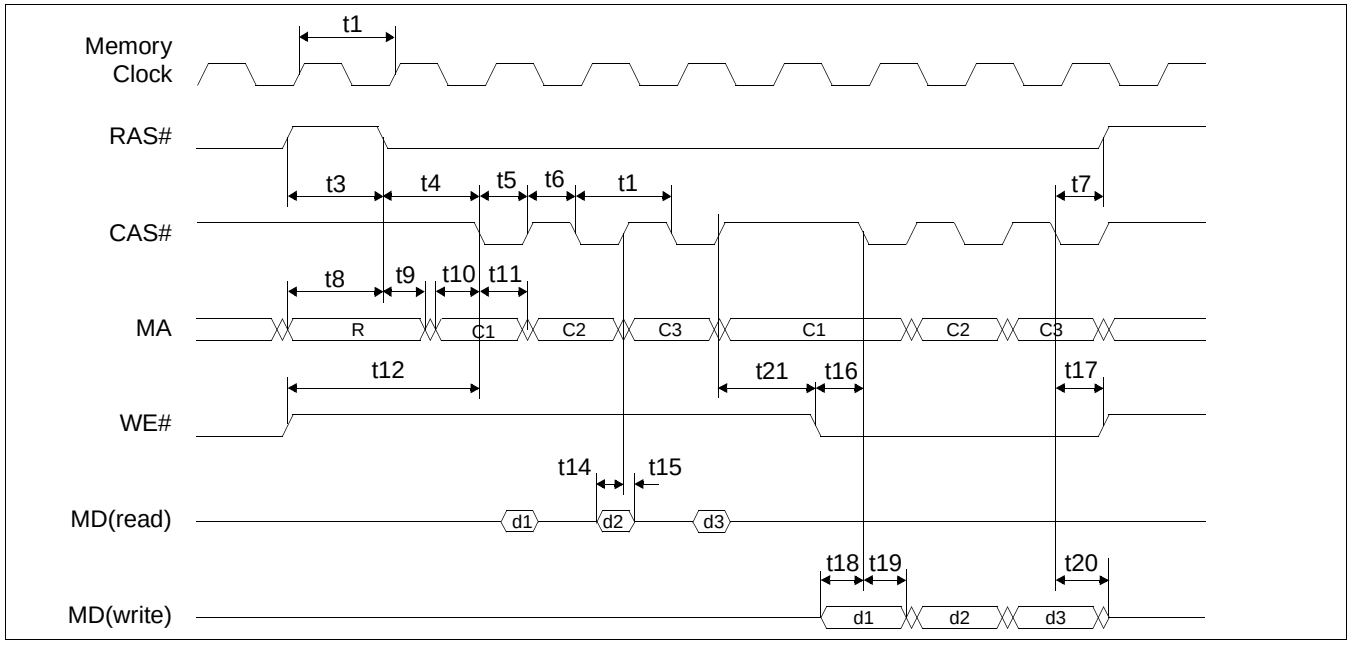

Figure 7-17: FPM-DRAM Read-Write Timing

Table 7-17: FPM-DRAM Read, Write, Read-Write Timing

Symbol	Parameter	Min	Max	Units
t1	Memory clock	40		ns
t2	Random read or write cycle time (REG[02Bh] bits 1-0 = 00)	5 t1		ns
	Random read or write cycle time (REG[02Bh] bits 1-0 = 01)	4 t1		ns
	Random read or write cycle time (REG[02Bh] bits 1-0 = 10)	3 t1		ns
t3	RAS# precharge time (REG[02Ah] bits 1-0 = 00)	2 t1		ns
	RAS# precharge time (REG[02Ah] bits 1-0 = 01)	1.45 t1		ns
	RAS# precharge time (REG[02Ah] bits 1-0 = 10)	t1		ns
t4	RAS# to CAS# delay time (REG[02Ah] bit 4 = 0 and bits 1-0 = 00 or 10)	2.45 t1 - 3	2.55 t1	ns
	RAS# to CAS# delay time (REG[02Ah] bit 4 = 1 and bits 1-0 = 00 or 10)	1.45 t1 - 3	1.55 t1	ns
	RAS# to CAS# delay time (REG[02Ah] bit 4 = 0 and bits 1-0 = 01)	2 t1 - 3	2 t1	ns
	RAS# to CAS# delay time (REG[02Ah] bit 4 = 1 and bits 1-0 = 01)	t1 - 3	t1	ns
t5	CAS# precharge time	0.45 t1		ns
t6	CAS# pulse width	0.45 t1 - 1		ns
t7	RAS# hold time	0.45 t1		ns
t8	Row address setup time (REG[02Ah] bits 1-0 = 00	2 t1 - 2		ns
	Row address setup time (REG[02Ah] bits 1-0 = 01)	1.45 t1 - 2		ns
	Row address setup time (REG[02Ah] bits 1-0 = 10)	t1 - 2		ns
t9	Row address hold time (REG[02Ah] bits 1-0 = 00 or 10)	t1 - 3		ns
	Row address hold time (REG[02Ah] bits 1-0 = 01)	0.45 t1 - 3		ns
t10	Column address set-up time	0.45 t1 - 3		ns
t11	Column address hold time	0.45 t1 - 1		ns
t12	Read Command setup (REG[02Ah] bit 4 = 0 and bits 1-0 = 00)	4.45 t1 - 1		ns
	Read Command setup (REG[02Ah] bit 4 = 1 and bits 1-0 = 01 or 10)	2.45 t1 - 1		ns
	Read Command setup (all other REG[02Ah] values)	3.45 t1 - 1		ns
t13	Read Command hold (REG[02Ah] bit 4 = 0 and bits 1-0 = 00)	4 t1 - 1		ns
	Read Command hold (REG[02Ah] bit 4 = 1 and bits 1-0 = 01 or 10)	2 t1 - 1		ns
	Read Command hold (all other REG[02Ah] values)	3 t1 - 1		ns
t14	Read data setup referenced from CAS#	3		ns
t15	Read Data turn-off from CAS#	3		ns
t16	Write command setup time	0.45 t1 - 1		ns
t17	Write command hold time	0.45 t1 - 1		ns
t18	Write Data setup time	0.45 t1 - 4		ns
t19	Write Data hold time	0.45 t1		ns
t20	MD tri-state	0.45 t1	0.55 t1 + 19	ns
t21	CAS# to WE# active during read-write cycle	0.45 t1		ns

7.3.5 FPM-DRAM CAS Before RAS Refresh Timing

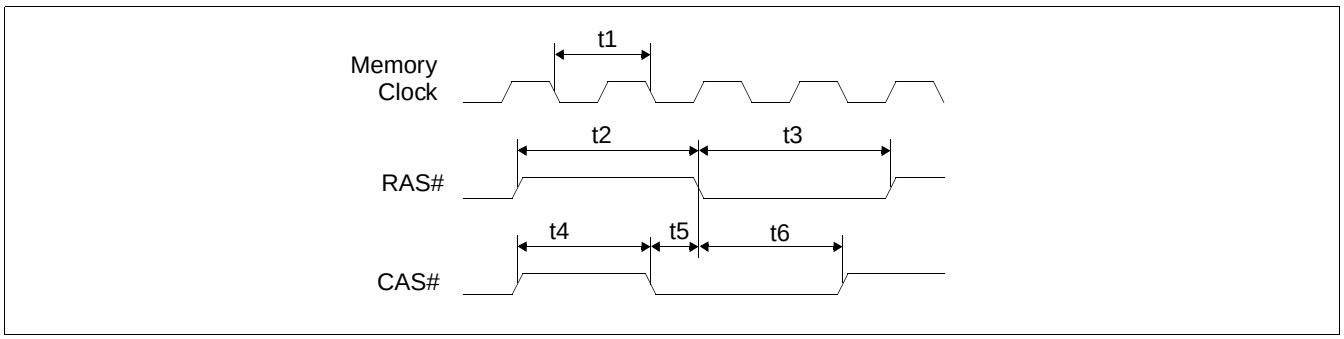

Figure 7-18: FPM-DRAM CAS Before RAS Refresh Timing

Table 7-18: FPM-DRAM CAS Before RAS Refresh Timing

Symbol	Parameter	Min	Max	Units
t1	Memory clock	40		ns
t2	RAS# precharge time (REG[02Ah] bits 1-0 = 00)	2.45 t1		ns
	RAS# precharge time (REG[02Ah] bits 1-0 = 01 or 10)	1.45 t1		ns
t3	RAS# pulse width (REG[02Bh] bits 1-0 = 00, REG[02Ah] bits 1-0 = 00)	2.45 t1 - 7		ns
	RAS# pulse width (REG[02Bh] bits 1-0 = 00, REG[02Ah] bits 1-0 = 01 or 10)	3.45 t1 - 7		ns
	RAS# pulse width (REG[02Bh] bits 1-0 = 01, REG[02Ah] bits 1-0 = 00)	1.45 t1 - 7		ns
	RAS# pulse width (REG[02Bh] bits 1-0 = 01, REG[02Ah] bits 1-0 = 01 or 10)	2.45 t1 - 7		ns
	RAS# pulse width (REG[02Bh] bits 1-0 = 10, REG[02Ah] bits 1-0 = 00)	0.45 t1 - 7		ns
	RAS# pulse width (REG[02Bh] bits 1-0 = 10, REG[02Ah] bits 1-0 = 01 or 10)	1.45 t1 - 7		ns
t4	CAS# precharge time (REG[02Ah] bits 1-0 = 00)	2 t1		ns
	CAS# precharge time (REG[02Ah] bits 1-0 = 01 or 10)	t1		ns
t5	CAS# setup time	0.45 t1		ns
t6	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 00, REG[02Ah] bits 1-0 = 00)	2.45 t1 - 4		ns
	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 00, REG[02Ah] bits 1-0 = 01 or 10)	3.45 t1 - 4		ns
	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 01, REG[02Ah] bits 1-0 = 00)	1.45 t1 - 4		ns
	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 01, REG[02Ah] bits 1-0 = 01 or 10)	2.45 t1 - 4		ns
	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 10, REG[02Ah] bits 1-0 = 00)	0.45 t1 - 4		ns
	CAS# hold to RAS# (REG[02Bh] bits 1-0 = 10, REG[02Ah] bits 1-0 = 01 or 10)	1.45 t1 - 4		ns

7.3.6 FPM-DRAM Self-Refresh Timing

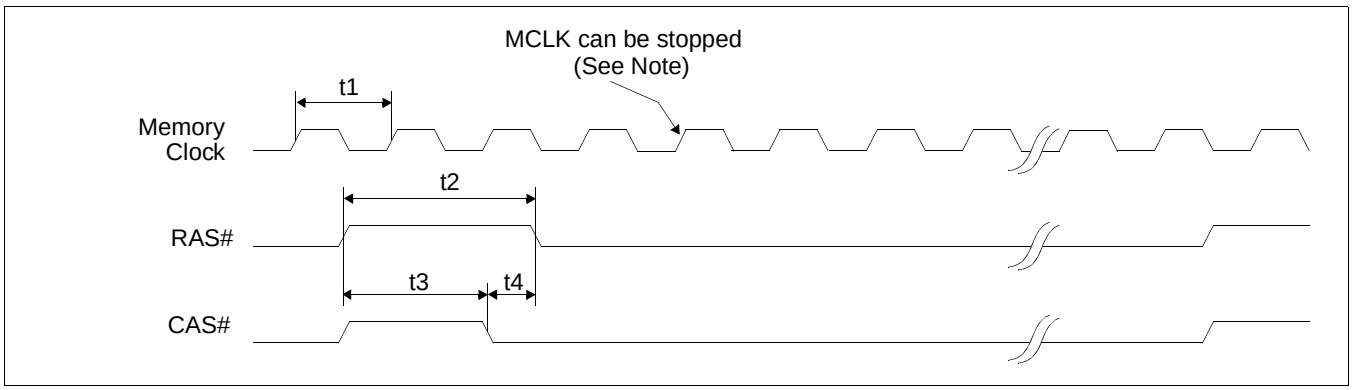

Figure 7-19: FPM - DRAM Self-Refresh Timing

Note
MCLK can be stopped. For timing see Section 7.4.2, “Power Save Mode” on page 71.

Table 7-19: FPM-DRAM Self-Refresh Timing

Symbol	Parameter	Min	Max	Units
t1	Memory clock	40		ns
t2	RAS# precharge time (REG[02Ah] bits 1-0 = 00)	2.45 t1		ns
	RAS# precharge time (REG[02Ah] bits 1-0 = 01 or 10)	1.45 t1		ns
t3	RAS# to CAS# precharge time (REG[02Ah] bits 1-0 = 00)	2 t1		ns
	RAS# to CAS# precharge time (REG[02Ah] bits 1-0 = 01 or 10)	t1		ns
t4	CAS# setup time	0.45 t1		ns

7.4 Power Sequencing

7.4.1 LCD Power Sequencing

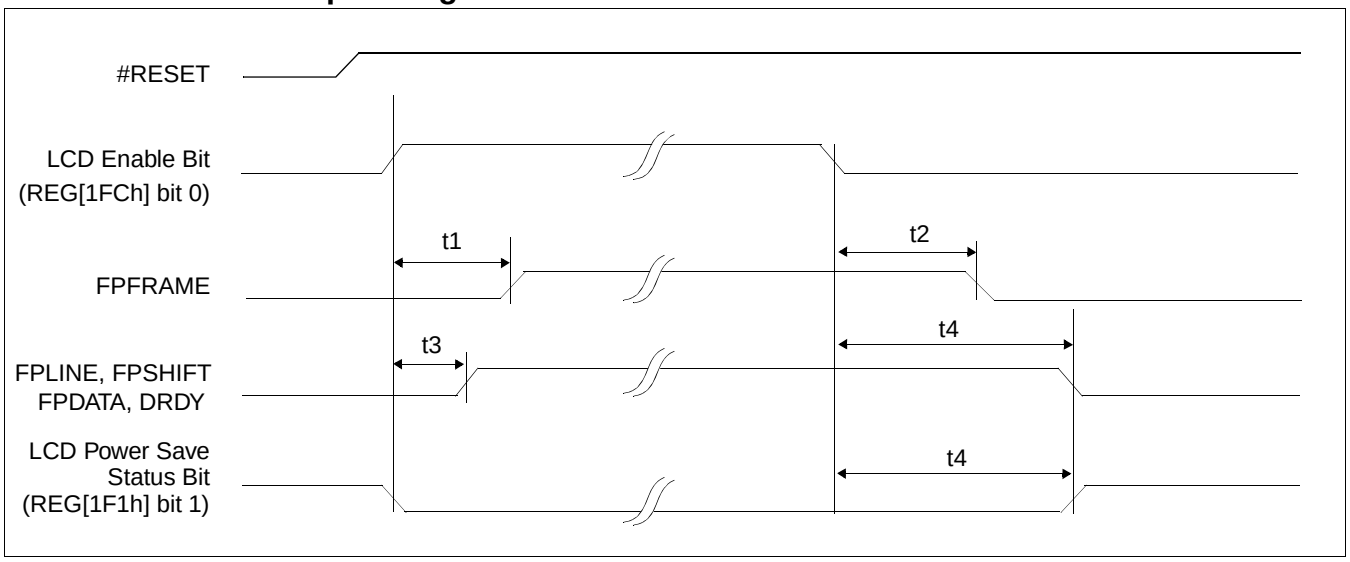

Figure 7-20: LCD Panel Power-off/Power-on Timing

Table 7-20: LCD Panel Power-off/Power-on Timing

Symbol	Parameter	Min	Max	Units
t1	LCD Enable Bit high to FPFRAME active		$T_{FPFRAME}$	ns
t2	FPFRAME inactive to LCD Power Save Status bit high		$5T_{FPFRAME}$	ns
t3	LCD Enable Bit high to FPLINE, FPSHIFT, FPDATA, DRDY active		$3T_{FPLINE}$	ns
t4	LCD Enable Bit low to FPLINE, FPSHIFT, FPDATA, DRDY active **and** LCD Power Save Status bit high		note 1	ns

1. t4 = $130T_{FPFRAME}$ for dual panels
   = $65T_{FPFRAME}$ for single panels

Note

Where $T_{FPFRAME}$ is the period of FPFRAME and T_{FPLINE} is the period of FPLINE.

7.4.2 Power Save Mode

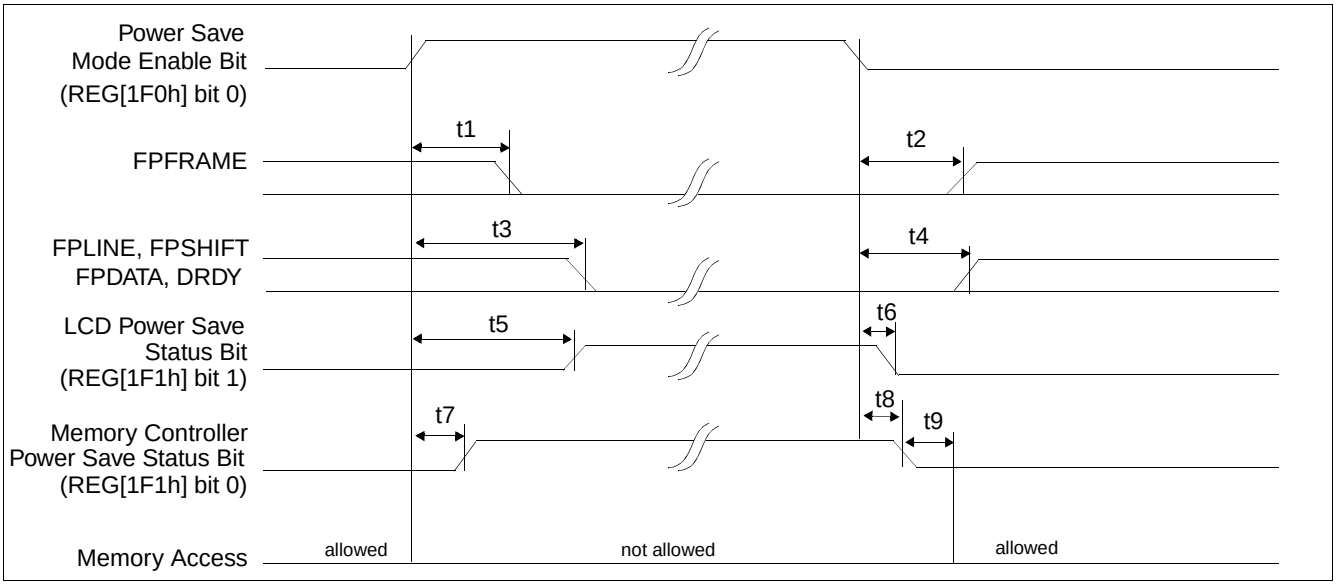

Figure 7-21: Power Save Mode Timing

Note
Memory accesses cannot be performed after a Power Save Mode has been initiated.

Note
The Memory Controller Power Save Status Bit will go high only if the Refresh Select Bits (REG[021h] bits 7-6) are set to Self-Refresh or No Refresh.

Table 7-21: Power Save Mode Timing

Symbol	Parameter	Min	Max	Units
t1	Power Save Mode Enable Bit high to FPFRAME inactive		$T_{FPFRAME} + T_{FPLINE}$	ns
t2	Power Save Mode Enable Bit low to FPFRAME active		$3T_{FPLINE}$	ns
t3	Power Save Mode Enable Bit high to FPLINE, FPSHIFT, FPDATA, DRDY inactive		$129T_{FPFRAME} + T_{FPLINE}$	ns
t4	Power Save Mode Enable Bit low to FPLINE, FPSHIFT, FPDATA, DRDY active		$T_{FPFRAME}$	ns
t5	Power Save Mode Enable Bit high to LCD Power Save Status Bit high	$128T_{FPFRAME}$	$129T_{FPRAME}$	ns
t6	Power Save Mode Enable Bit low to LCD Power Save Status Bit low		T_{PCLK}	ns
t7	Power Save Mode Enable Bit high to Memory Controller Power Save Status Bit high (self-refresh or no refresh selected)		note 1	ns
t8	Power Save Mode Enable Bit low to Memory Controller Power Save Status Bit low (self-refresh or no refresh selected)		$12T_{MCLK}$	ns
t9	Memory Controller Power Save Status Bit low to the earliest time where memory access is allowed (self-refresh or no refresh selected)		$8T_{MCLK}$	ns

1. $t7_{max}$ = (1 DRAM refresh clock period) + 12 MCLK periods

Note

Where $T_{FPFRAME}$ is the period of FPFRAME, T_{FPLINE} is the period of FPLINE, T_{PCLK} is the period of the pixel clock, and T_{MCLK} is the period of the memory clock.

Note

The DRAM refresh clock period is programmed using REG[021h].

7.5 Display Interface

7.5.1 Single Monochrome 4-Bit Panel Timing

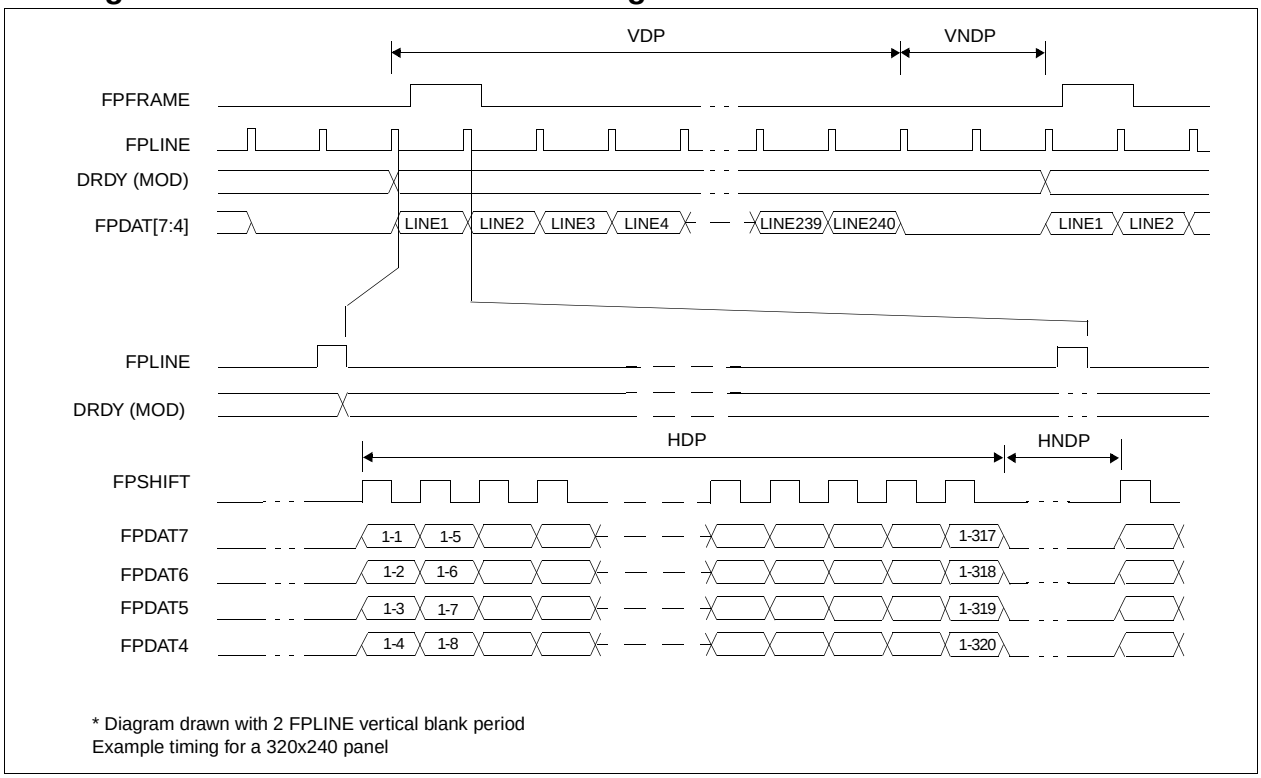

Figure 7-22: Single Monochrome 4-Bit Panel Timing

VDP = Vertical Display Period = (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8 Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8 Ts

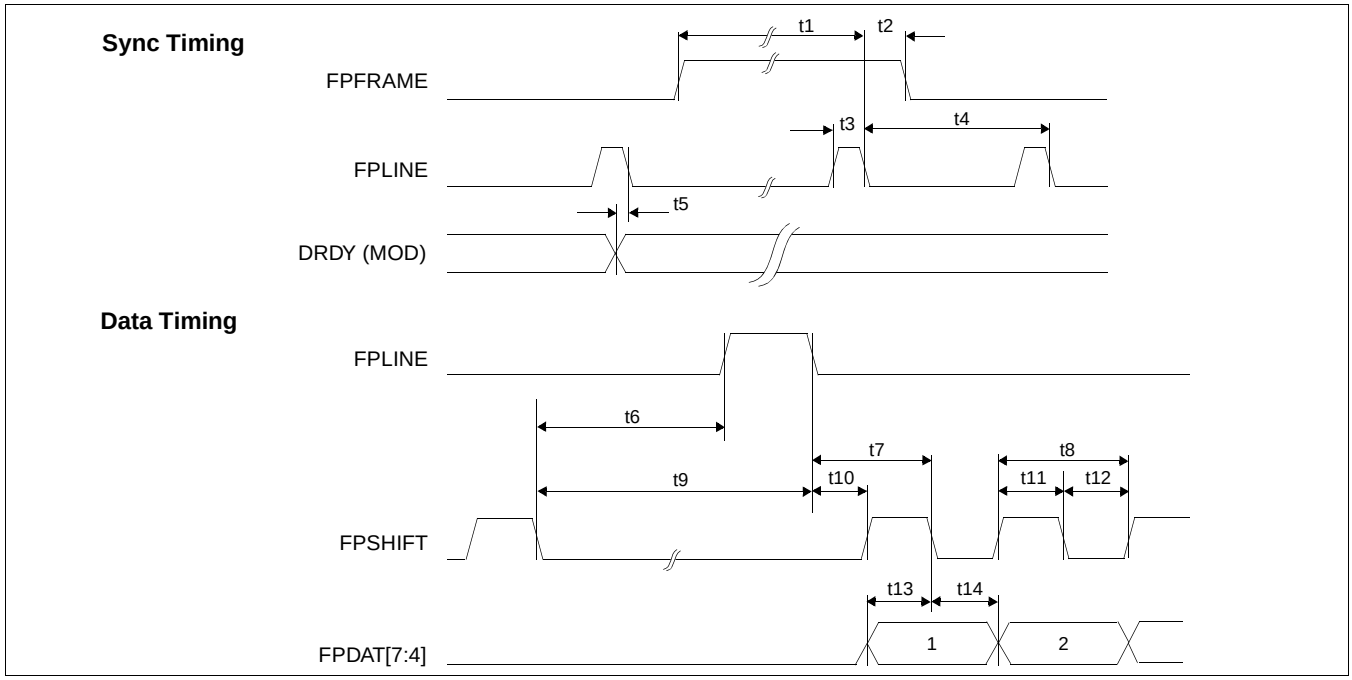

Figure 7-23: Single Monochrome 4-Bit Panel A.C. Timing

Table 7-22: Single Monochrome 4-Bit Panel A.C. Timing

Symbol	Parameter	Min. Setting	Typical	Max. Setting	Units
t1	FPFRAME setup to FPLINE falling edge	28	note 2	1268	Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge		12		Ts
t3	FPLINE pulse width		11		Ts
t4	FPLINE period	40	note 3	1280	Ts
t5	DRDY (MOD) delay from FPLINE falling edge	3	note 4	259	Ts
t6a	FPSHIFT falling edge to FPLINE rising edge, 4 bpp or 8 bpp	5	note 5	229	Ts
t6b	FPSHIFT falling edge to FPLINE rising edge, 15/16 bpp	7	note 5	231	Ts
t7a	FPLINE falling edge to FPSHIFT falling edge, 4 bpp or 8 bpp		20		Ts
t7b	FPLINE falling edge to FPSHIFT falling edge, 15/16 bpp		18		Ts
t8	FPSHIFT period		4		Ts
t9a	FPSHIFT falling edge to FPLINE falling edge, 4 bpp or 8 bpp	16	note 6	240	Ts
t9b	FPSHIFT falling edge to FPLINE falling edge, 15/16 bpp	18	note 6	242	Ts
t10a	FPLINE falling edge to FPSHIFT rising edge, 4 bpp or 8 bpp		18		Ts
t10b	FPLINE falling edge to FPSHIFT rising edge, 15/16 bpp		16		Ts
t11	FPSHIFT pulse width high		2		Ts
t12	FPSHIFT pulse width low		2		Ts
t13	FPDAT[7:4] setup to FPSHIFT falling edge		2		Ts
t14	FPDAT[7:4] hold to FPSHIFT falling edge		2		Ts

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. t1 = t4 - 12
3. t4 = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. t5 = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. t6 = [((REG[034h] bits [4:0]) + 1) × 8 - 27] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 25] for 15/16 bpp color depth
6. t9 = [((REG[034h] bits [4:0]) + 1) × 8 - 16] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 14] for 15/16 bpp color depth

7.5.2 Single Monochrome 8-Bit Panel Timing

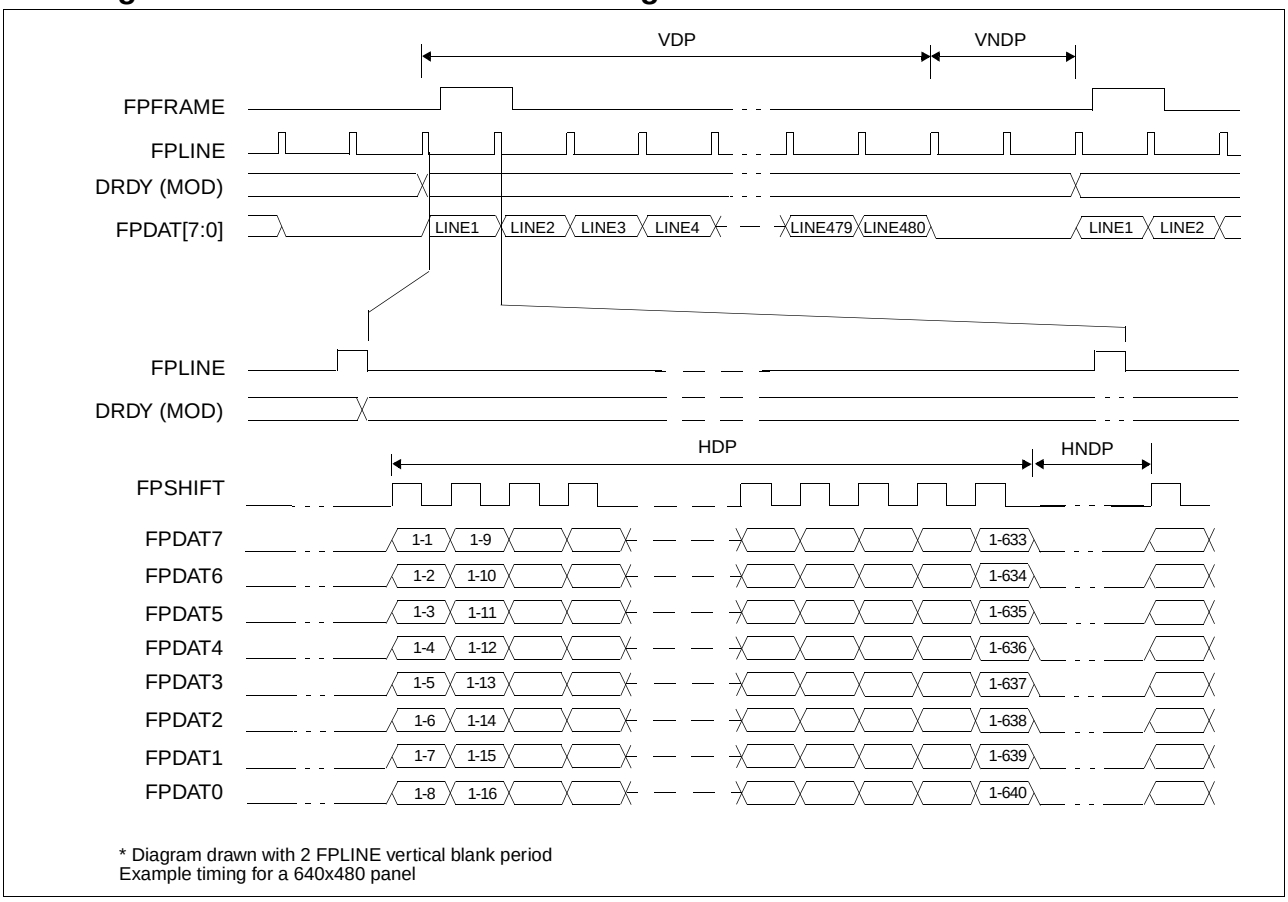

Figure 7-24: Single Monochrome 8-Bit Panel Timing

VDP = Vertical Display Period = (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8 Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8 Ts

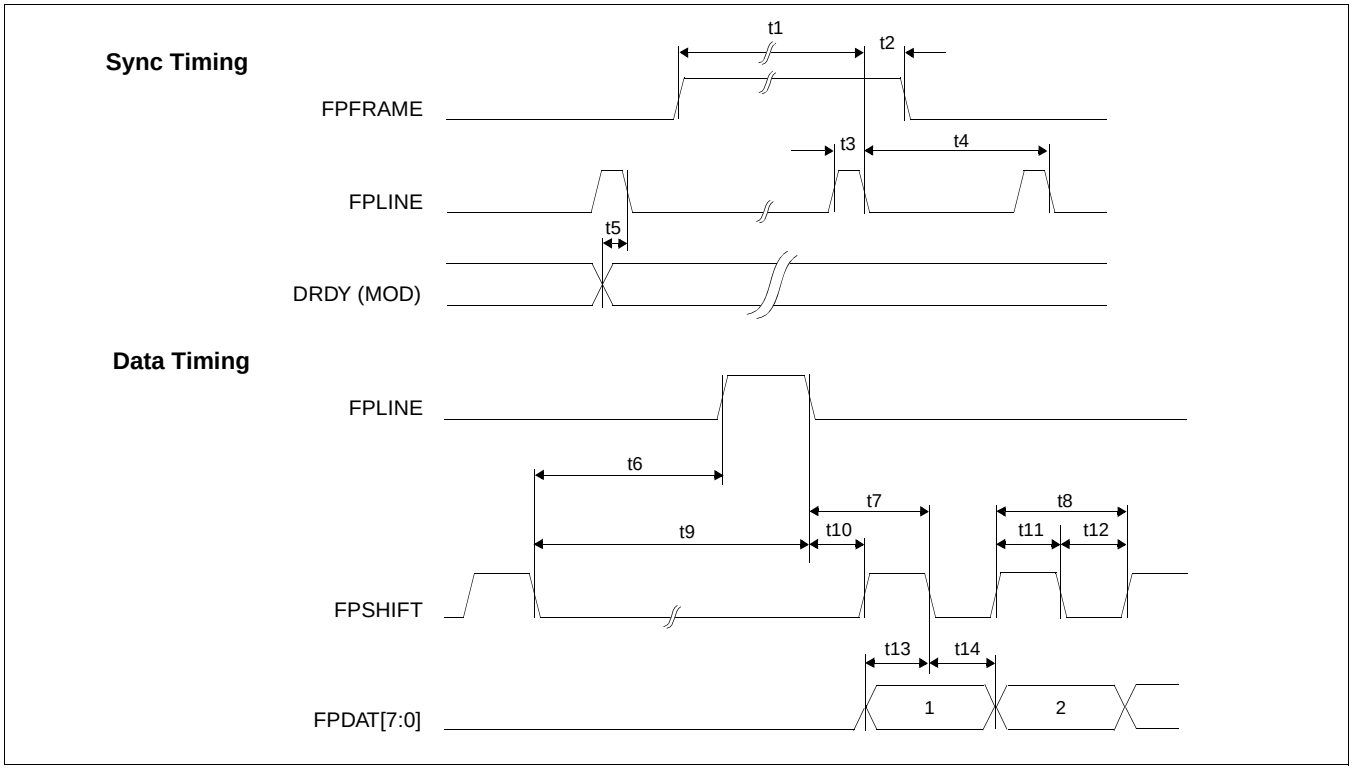

Figure 7-25: Single Monochrome 8-Bit Panel A.C. Timing

Table 7-23: Single Monochrome 8-Bit Panel A.C. Timing

Symbol	Parameter	Min. Setting	Typical	Max. Setting	Units
t1	FPFRAME setup to FPLINE falling edge	28	note 2	1268	Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge		12		Ts
t3	FPLINE pulse width		11		Ts
t4	FPLINE period	40	note 3	1280	Ts
t5	DRDY (MOD) delay from FPLINE falling edge	3	note 4	259	Ts
t6a	FPSHIFT falling edge to FPLINE rising edge, 4 bpp or 8 bpp	7	note 5	231	Ts
t6b	FPSHIFT falling edge to FPLINE rising edge, 15/16 bpp	9	note 5	233	Ts
t7a	FPLINE falling edge to FPSHIFT falling edge, 4 bpp or 8 bpp		22		Ts
t7b	FPLINE falling edge to FPSHIFT falling edge, 15/16 bpp		20		Ts
t8	FPSHIFT period		8		Ts
t9a	FPSHIFT falling edge to FPLINE falling edge, 4 bpp or 8 bpp	18	note 6	242	Ts
t9b	FPSHIFT falling edge to FPLINE falling edge, 15/16 bpp	20	note 6	244	Ts
t10a	FPLINE falling edge to FPSHIFT rising edge, 4 bpp or 8 bpp		18		Ts
t10b	FPLINE falling edge to FPSHIFT rising edge, 15/16 bpp		16		Ts
t11	FPSHIFT pulse width high		4		Ts
t12	FPSHIFT pulse width low		4		Ts
t13	FPDAT[7:0] setup to FPSHIFT falling edge		4		Ts
t14	FPDAT[7:0] hold to FPSHIFT falling edge		4		Ts

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. t1 = t4 - 12
3. t4 = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. t5 = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. t6 = [((REG[034h] bits [4:0]) + 1) × 8 - 25] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 23] for 15/16 bpp color depth
6. t9 = [((REG[034h] bits [4:0]) + 1) × 8 - 14] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 12] for 15/16 bpp color depth

7.5.3 Single Color 4-Bit Panel Timing

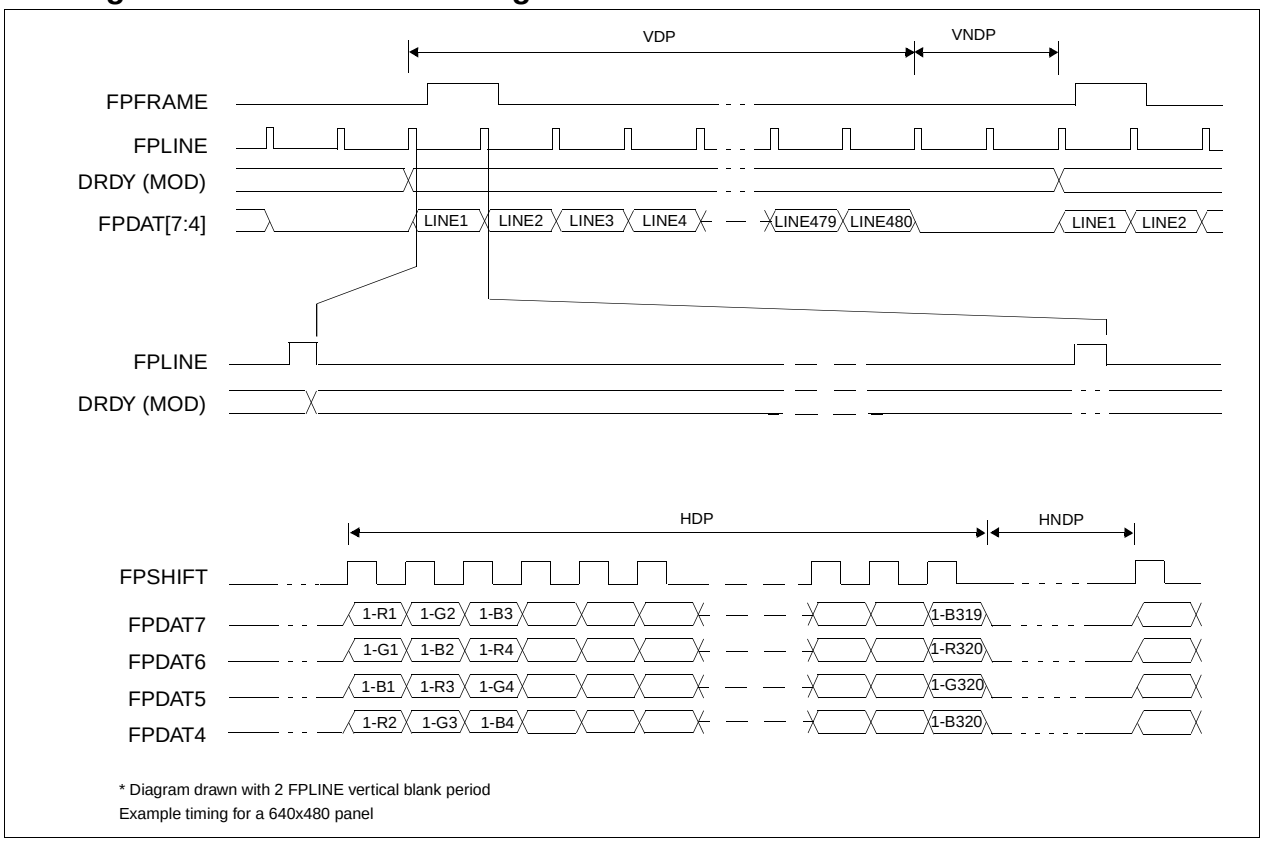

Figure 7-26: Single Color 4-Bit Panel Timing

VDP	= Vertical Display Period	= (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[03Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[032h] bits [6:0]) + 1) × 8 Ts
HNDP	= Horizontal Non-Display Period	= ((REG[034h] bits [4:0]) + 1) × 8 Ts

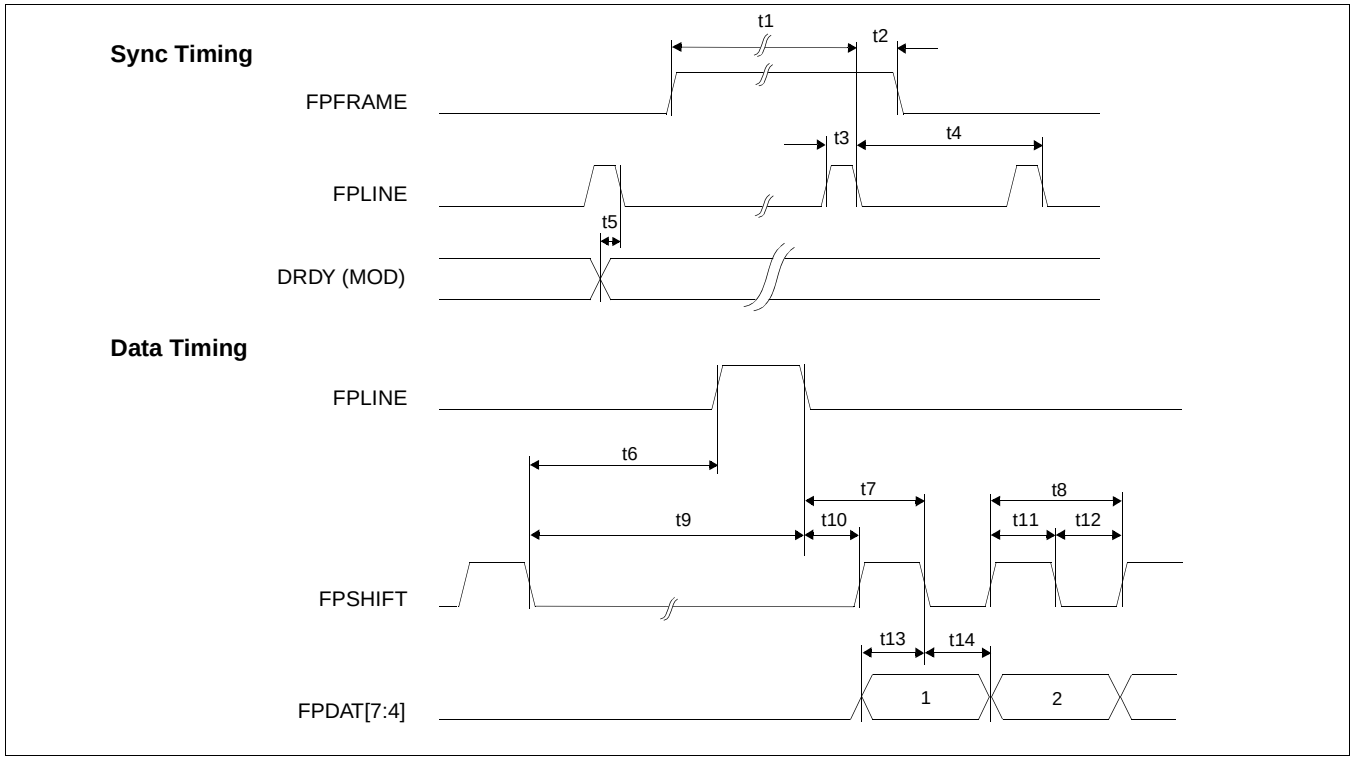

Figure 7-27: Single Color 4-Bit Panel A.C. Timing

Table 7-24: Single Color 4-Bit Panel A.C. Timing

Symbol	Parameter	Min. Setting	Typical	Max. Setting	Units
t1	FPFRAME setup to FPLINE falling edge	28	note 2	1268	Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge		12		Ts
t3	FPLINE pulse width		11		Ts
t4	FPLINE period	40	note 3	1280	Ts
t5	DRDY (MOD) delay from FPLINE falling edge	3	note 4	259	Ts
t6a	FPSHIFT falling edge to FPLINE rising edge, 4 bpp or 8 bpp	4.5	note 5	228.5	Ts
t6b	FPSHIFT falling edge to FPLINE rising edge, 15/16 bpp	6.5	note 5	230.5	Ts
t7a	FPLINE falling edge to FPSHIFT falling edge, 4 bpp or 8 bpp		19.5		Ts
t7b	FPLINE falling edge to FPSHIFT falling edge, 15/16 bpp		17.5		Ts
t8	FPSHIFT period		1		Ts
t9a	FPSHIFT falling edge to FPLINE falling edge, 4 bpp or 8 bpp	15.5	note 6	239.5	Ts
t9b	FPSHIFT falling edge to FPLINE falling edge, 15/16 bpp	17.5	note 6	241.5	Ts
t10a	FPLINE falling edge to FPSHIFT rising edge, 4 bpp or 8 bpp		19		Ts
t10b	FPLINE falling edge to FPSHIFT rising edge, 15/16 bpp		17		Ts
t11	FPSHIFT pulse width high		0.5		Ts
t12	FPSHIFT pulse width low		0.5		Ts
t13	FPDAT[7:4] setup to FPSHIFT falling edge		0.5		Ts
t14	FPDAT[7:4] hold from FPSHIFT falling edge		0.5		Ts

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. t1 = t4 - 12
3. t4 = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. t5 = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. t6 = [((REG[034h] bits [4:0]) + 1) × 8 - 27.5] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 25.5] for 15/16 bpp color depth
6. t9 = [((REG[034h] bits [4:0]) + 1) × 8 - 16.5] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 14.5] for 15/16 bpp color depth

7.5.4 Single Color 8-Bit Panel Timing (Format 1)

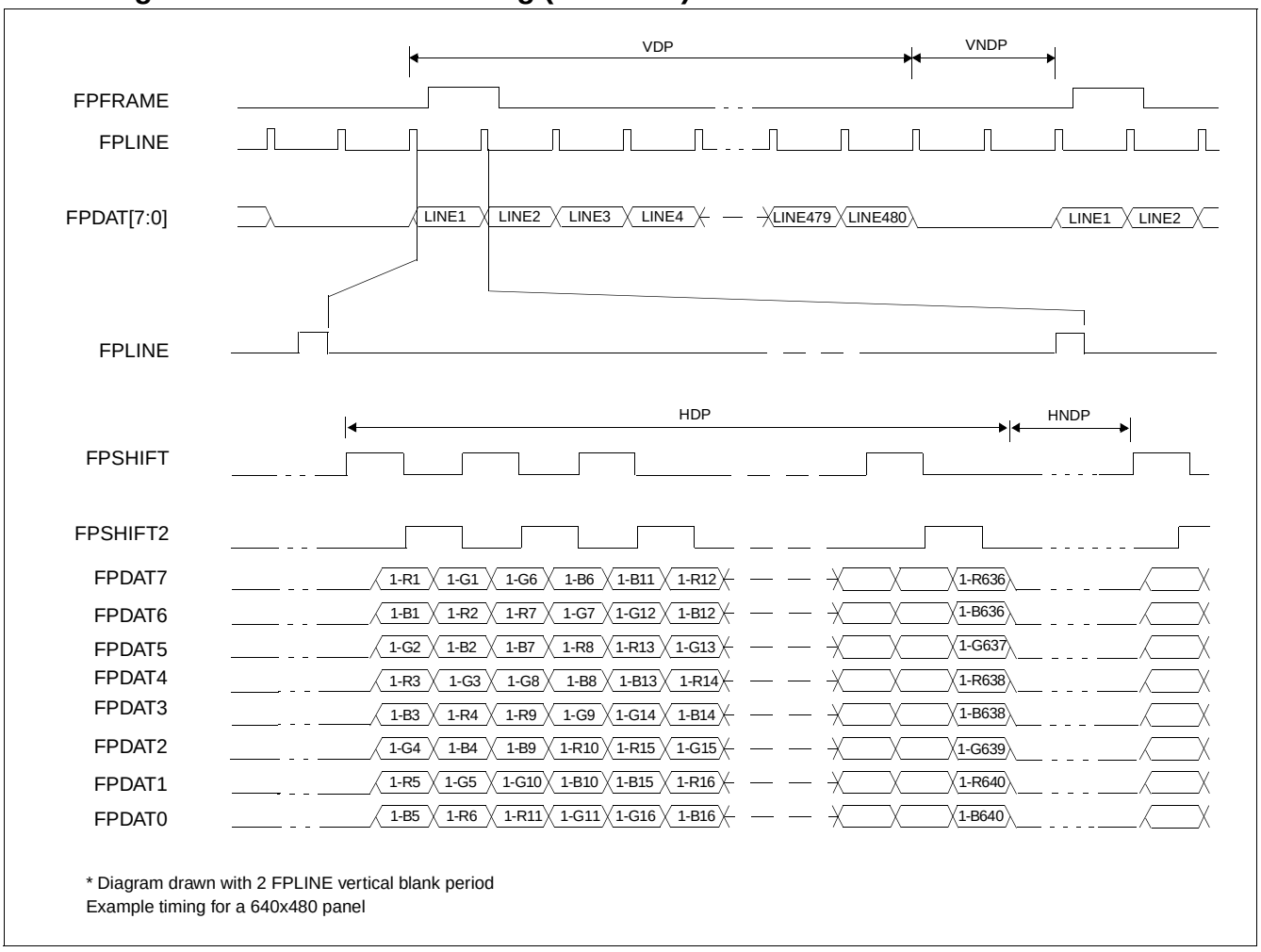

Figure 7-28: Single Color 8-Bit Panel Timing (Format 1)

VDP	= Vertical Display Period	= (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[03Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[032h] bits [6:0]) + 1) × 8 Ts
HNDP	= Horizontal Non-Display Period	= ((REG[034h] bits [4:0]) + 1) × 8 Ts

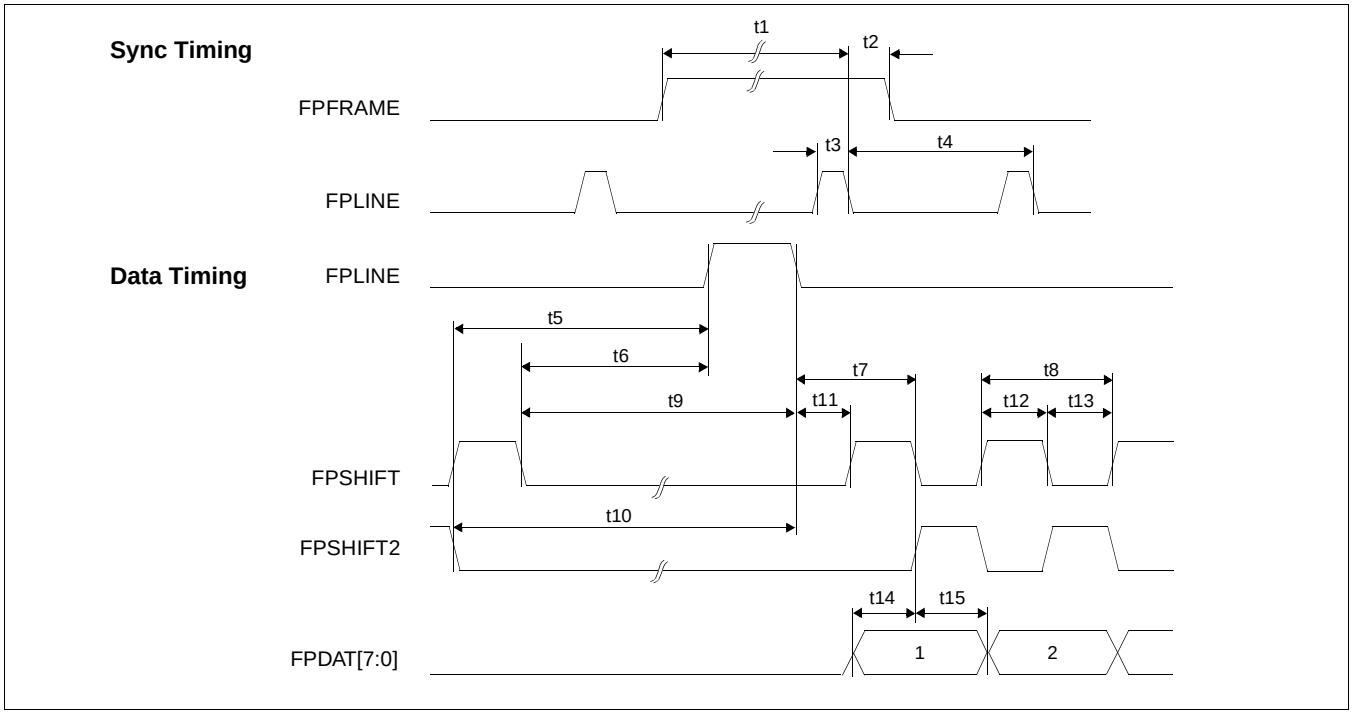

Figure 7-29: Single Color 8-Bit Panel A.C. Timing (Format 1)

Table 7-25: Single Color 8-Bit Panel A.C. Timing (Format 1)

Symbol	Parameter	Min. Setting	Typical	Max. Setting	Units
t1	FPFRAME setup to FPLINE falling edge	28	note 2	1268	Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge		12		Ts
t3	FPLINE pulse width		11		Ts
t4	FPLINE period	40	note 3	1280	Ts
t5a	FPSHIFT2 falling edge to FPLINE rising edge, 4 bpp or 8 bpp	5	note 4	229	Ts
t5b	FPSHIFT2 falling edge to FPLINE rising edge, 15/16 bpp	7	note 4	231	Ts
t6a	FPSHIFT falling edge to FPLINE rising edge, 4 bpp or 8 bpp	3	note 5	227	Ts
t6b	FPSHIFT falling edge to FPLINE rising edge, 15/16 bpp	5	note 5	229	Ts
t7a	FPLINE falling edge to FPSHIFT2 rising, FPSHIFT falling edge, 4/8 bpp		20		Ts
t7b	FPLINE falling edge to FPSHIFT2 rising, FPSHIFT falling edge, 15/16 bpp		18		Ts
t8	FPSHIFT2, FPSHIFT period		4		Ts
t9a	FPSHIFT falling edge to FPLINE falling edge, 4 bpp or 8 bpp	14	note 6	238	Ts
t9b	FPSHIFT falling edge to FPLINE falling edge, 15/16 bpp	16	note 6	240	Ts
t10a	FPSHIFT2 falling edge to FPLINE falling edge, 4 bpp or 8 bpp	16	note 7	240	Ts
t10b	FPSHIFT2 falling edge to FPLINE falling edge, 15/16 bpp	18	note 7	242	Ts
t11a	FPLINE falling edge to FPSHIFT rising edge, 4 bpp or 8 bpp		18		Ts
t11b	FPLINE falling edge to FPSHIFT rising edge, 15/16 bpp		16		Ts
t12	FPSHIFT2, FPSHIFT pulse width high		2		Ts
t13	FPSHIFT2, FPSHIFT pulse width low		2		Ts
t14	FPDAT[7:0] setup to FPSHIFT2 rising, FPSHIFT falling edge		1		Ts
t15	FPDAT[7:0] hold from FPSHIFT2 rising, FPSHIFT falling edge		1		Ts

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. t1 = t4 - 12
3. t4 = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. t5 = [((REG[034h] bits [4:0]) + 1) × 8 - 27] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 25] for 15/16 bpp color depth
5. t6 = [((REG[034h] bits [4:0]) + 1) × 8 - 29] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 27] for 15/16 bpp color depth
6. t9 = [((REG[034h] bits [4:0]) + 1) × 8 - 18] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 16] for 15/16 bpp color depth
7. t10 = [((REG[034h] bits [4:0]) + 1) × 8 - 16] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 14] for 15/16 bpp color depth

7.5.5 Single Color 8-Bit Panel Timing (Format 2)

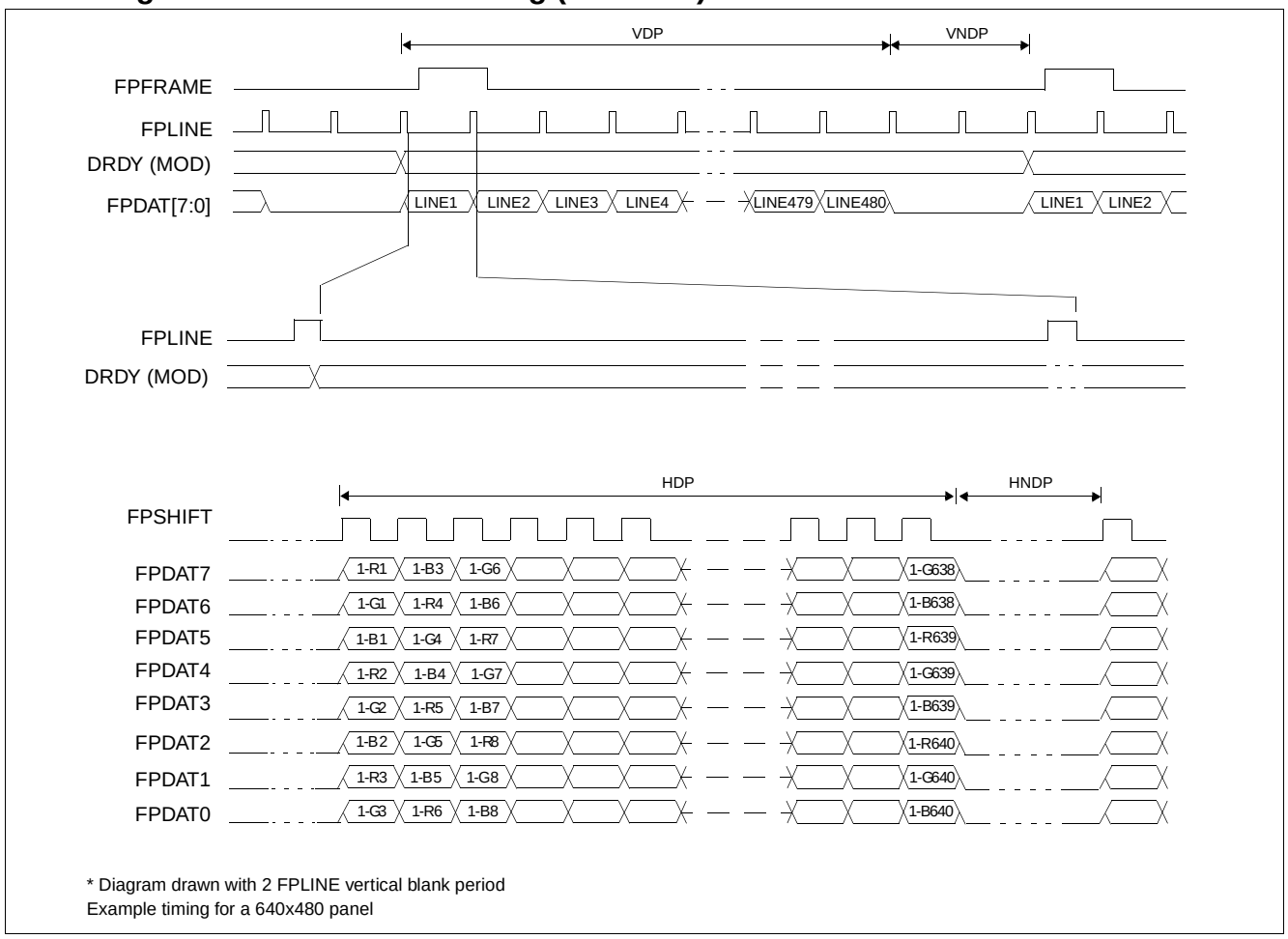

Figure 7-30: Single Color 8-Bit Panel Timing (Format 2)

VDP = Vertical Display Period = (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8 Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8 Ts

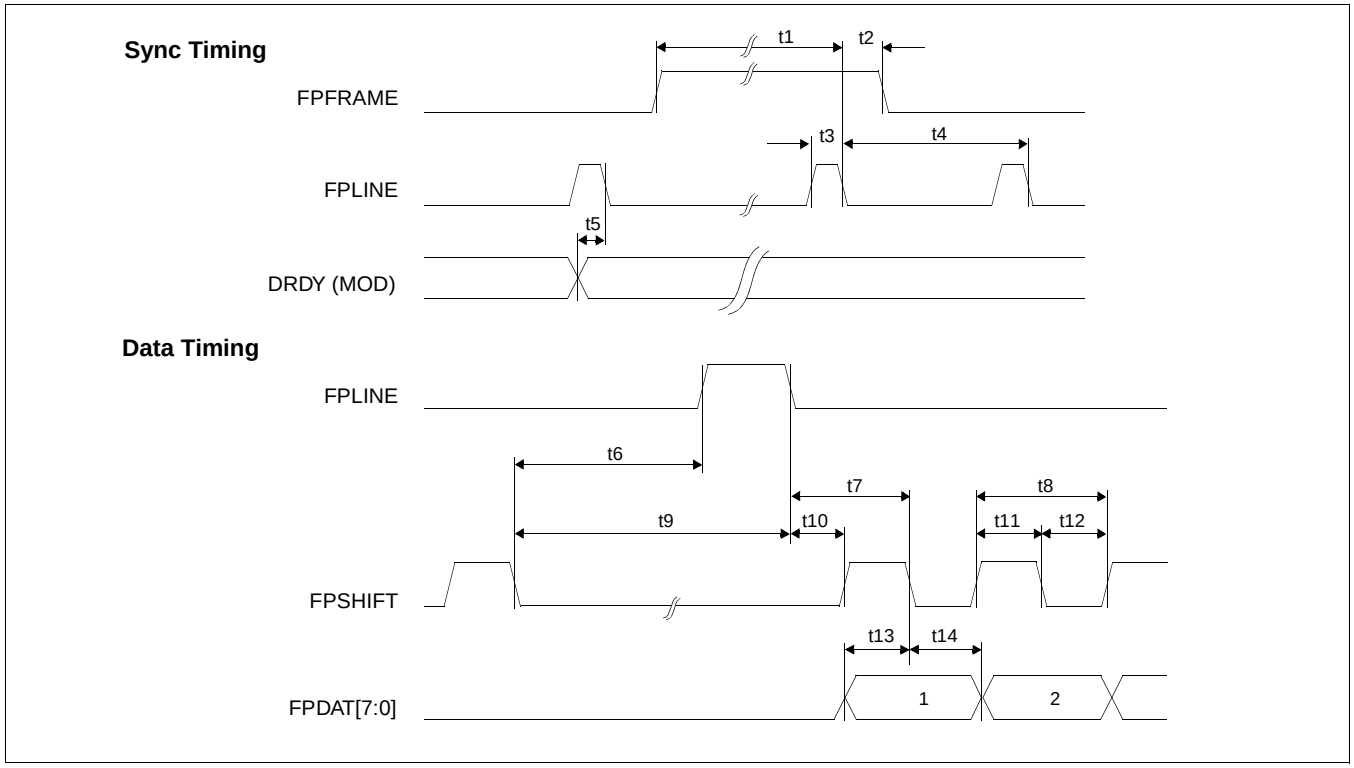

Figure 7-31: Single Color 8-Bit Panel A.C. Timing (Format 2)

Table 7-26: Single Color 8-Bit Panel A.C. Timing (Format 2)

Symbol	Parameter	Min. Setting	Typical	Max. Setting	Units
t1	FPFRAME setup to FPLINE falling edge	28	note 2	1268	Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge		12		Ts
t3	FPLINE pulse width		11		Ts
t4	FPLINE period	40	note 3	1280	Ts
t5	DRDY (MOD) delay from FPLINE falling edge	3	note 4	259	Ts
t6a	FPSHIFT falling edge to FPLINE rising edge, 4 bpp or 8 bpp	4	note 5	228	Ts
t6b	FPSHIFT falling edge to FPLINE rising edge, 15/16 bpp	6	note 5	230	Ts
t7a	FPLINE falling edge to FPSHIFT falling edge, 4 bpp or 8 bpp		20		Ts
t7b	FPLINE falling edge to FPSHIFT falling edge, 15/16 bpp		18		Ts
t8	FPSHIFT period		2		Ts
t9a	FPSHIFT falling edge to FPLINE falling edge, 4 bpp or 8 bpp	15	note 6	239	Ts
t9b	FPSHIFT falling edge to FPLINE falling edge, 15/16 bpp	17	note 6	241	Ts
t10a	FPLINE falling edge to FPSHIFT rising edge, 4 bpp or 8 bpp		18		Ts
t10b	FPLINE falling edge to FPSHIFT rising edge, 15/16 bpp		16		Ts
t11	FPSHIFT pulse width high		1		Ts
t12	FPSHIFT pulse width low		1		Ts
t13	FPDAT[7:0] setup to FPSHIFT falling edge		1		Ts
t14	FPDAT[7:0] hold to FPSHIFT falling edge		1		Ts

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. t1 = t4 - 12
3. t4 = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. t5 = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. t6 = [((REG[034h] bits [4:0]) + 1) × 8 - 28] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 26] for 15/16 bpp color depth
6. t9 = [((REG[034h] bits [4:0]) + 1) × 8 - 17] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 15] for 15/16 bpp color depth

7.5.6 Single Color 16-Bit Panel Timing

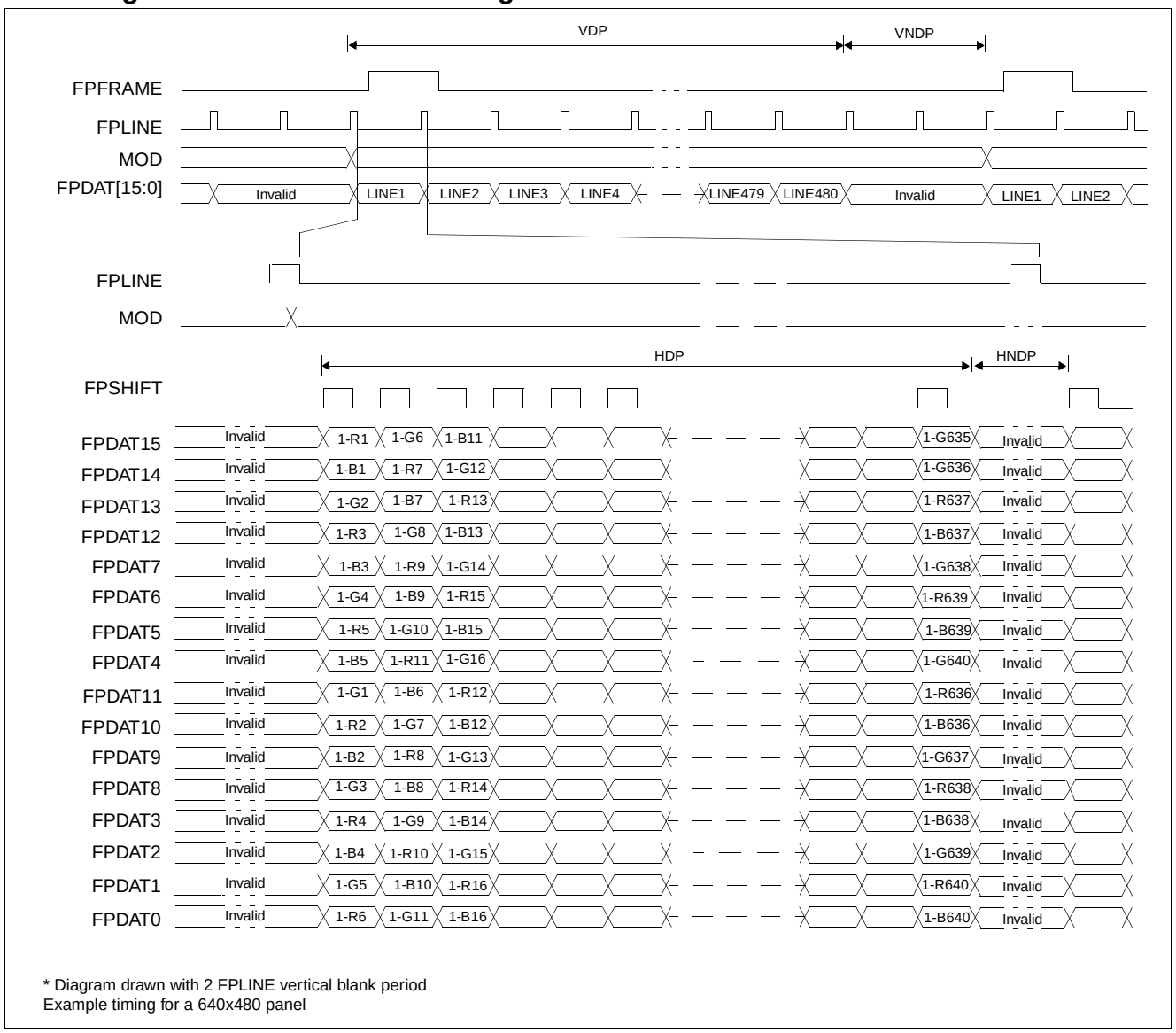

Figure 7-32: Single Color 16-Bit Panel Timing

VDP = Vertical Display Period = (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8 Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8 Ts

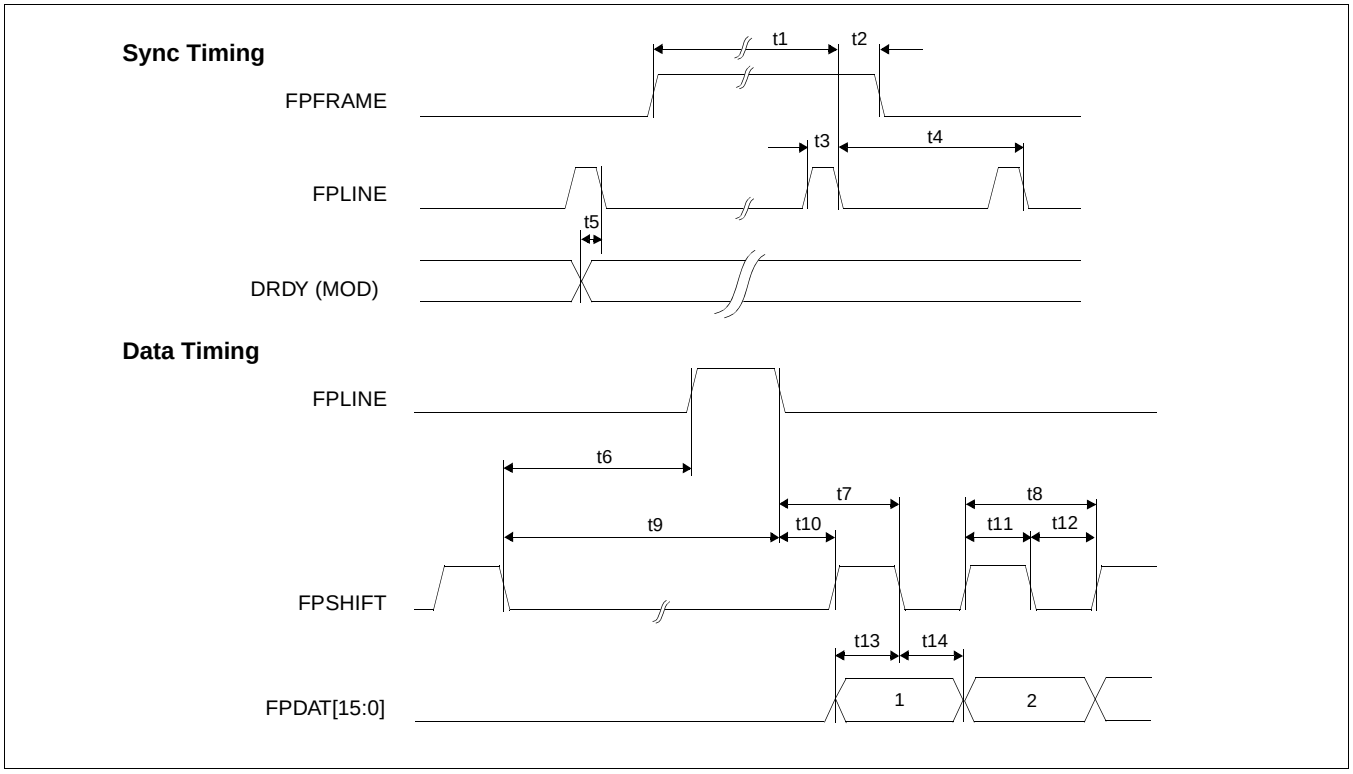

Figure 7-33: Single Color 16-Bit Panel A.C. Timing

Table 7-27: Single Color 16-Bit Panel A.C. Timing

Symbol	Parameter	Min. Setting	Typical	Max. Setting	Units
t1	FPFRAME setup to FPLINE falling edge	28	note 2	1268	Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge		12		Ts
t3	FPLINE pulse width		11		Ts
t4	FPLINE period	40	note 3	1280	Ts
t5	DRDY (MOD) delay from FPLINE falling edge	3	note 4	259	Ts
t6a	FPSHIFT falling edge to FPLINE rising edge, 4 bpp or 8 bpp	5	note 5	229	Ts
t6b	FPSHIFT falling edge to FPLINE rising edge, 15/16 bpp	7	note 5	231	Ts
t7a	FPLINE falling edge to FPSHIFT falling edge, 4 bpp or 8 bpp		21		Ts
t7b	FPLINE falling edge to FPSHIFT falling edge, 15/16 bpp		19		Ts
t8	FPSHIFT period		5		Ts
t9a	FPSHIFT falling edge to FPLINE falling edge, 4 bpp or 8 bpp	16	note 6	240	Ts
t9b	FPSHIFT falling edge to FPLINE falling edge, 15/16 bpp	18	note 6	242	Ts
t10a	FPLINE falling edge to FPSHIFT rising edge, 4 bpp or 8 bpp		18		Ts
t10b	FPLINE falling edge to FPSHIFT rising edge, 15/16 bpp		16		Ts
t11	FPSHIFT pulse width high		2		Ts
t12	FPSHIFT pulse width low		2		Ts
t13	FPDAT[15:0] setup to FPSHIFT falling edge		2		Ts
t14	FPDAT[15:0] hold to FPSHIFT falling edge		2		Ts

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. t1 = t4 - 12
3. t4 = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. t5 = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. t6 = [((REG[034h] bits [4:0]) + 1) × 8 - 27] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 25] for 15/16 bpp color depth
6. t9 = [((REG[034h] bits [4:0]) + 1) × 8 - 16] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 14] for 15/16 bpp color depth

7.5.7 Single Color 16-Bit Panel Timing with External Circuit

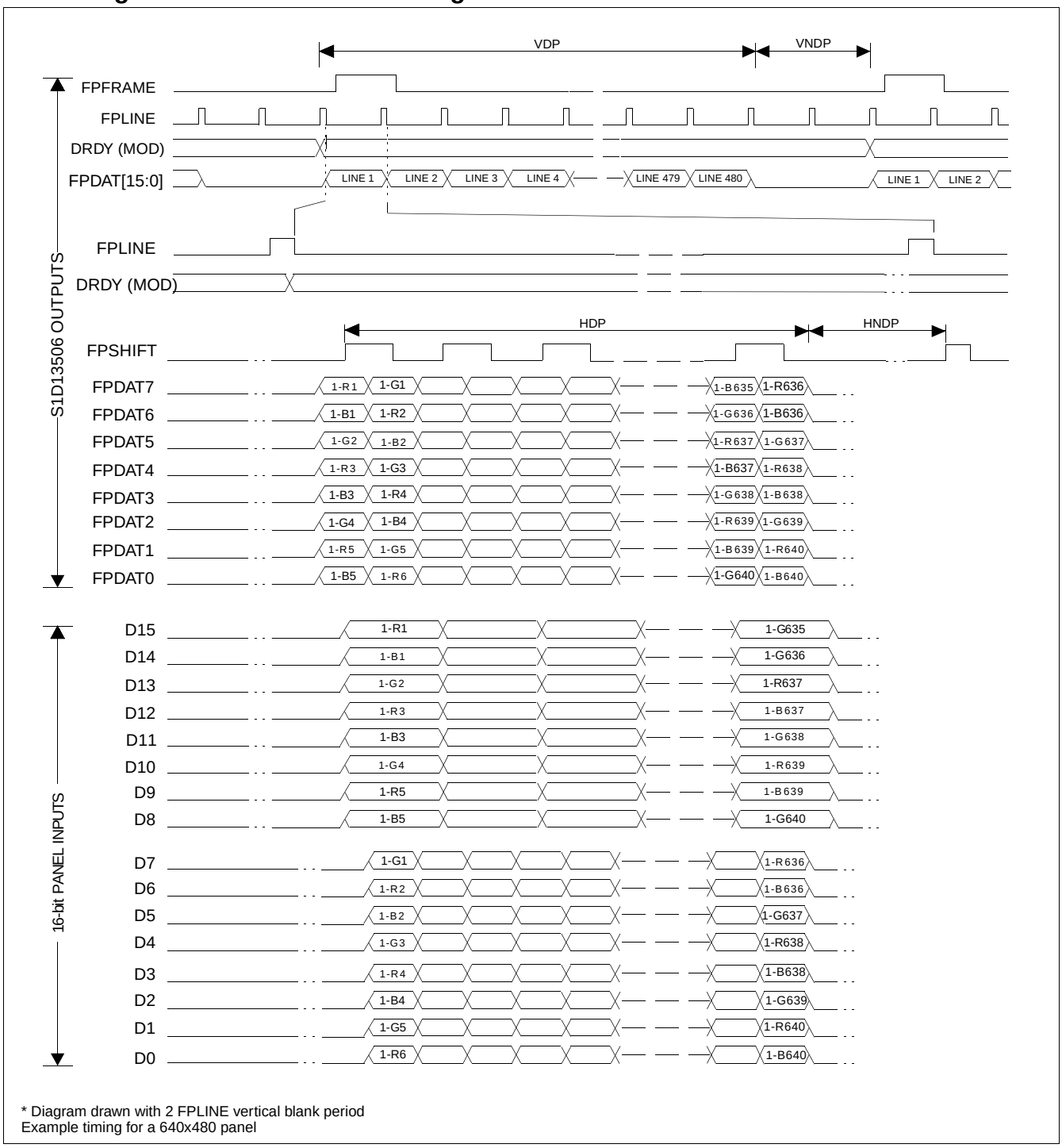

Figure 7-34: 16-Bit Single Color Panel Timing with External Circuit

VDP = Vertical Display Period = (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8 Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8 Ts

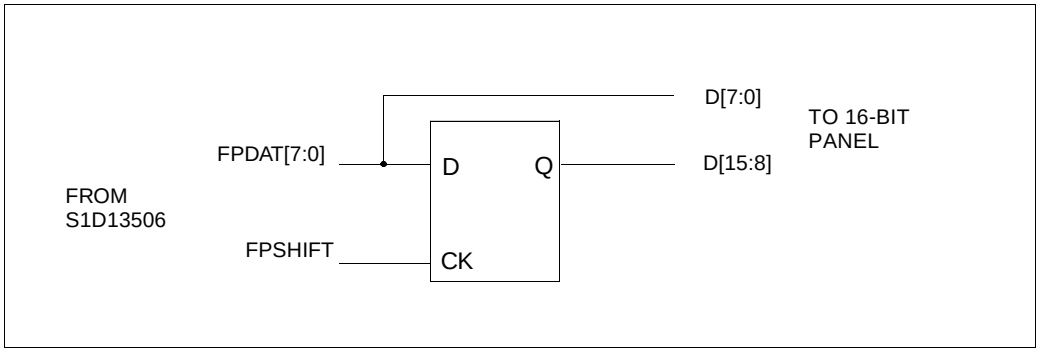

Figure 7-35: External Circuit for Color Single 16-Bit Panel When the Media Plug is Enabled

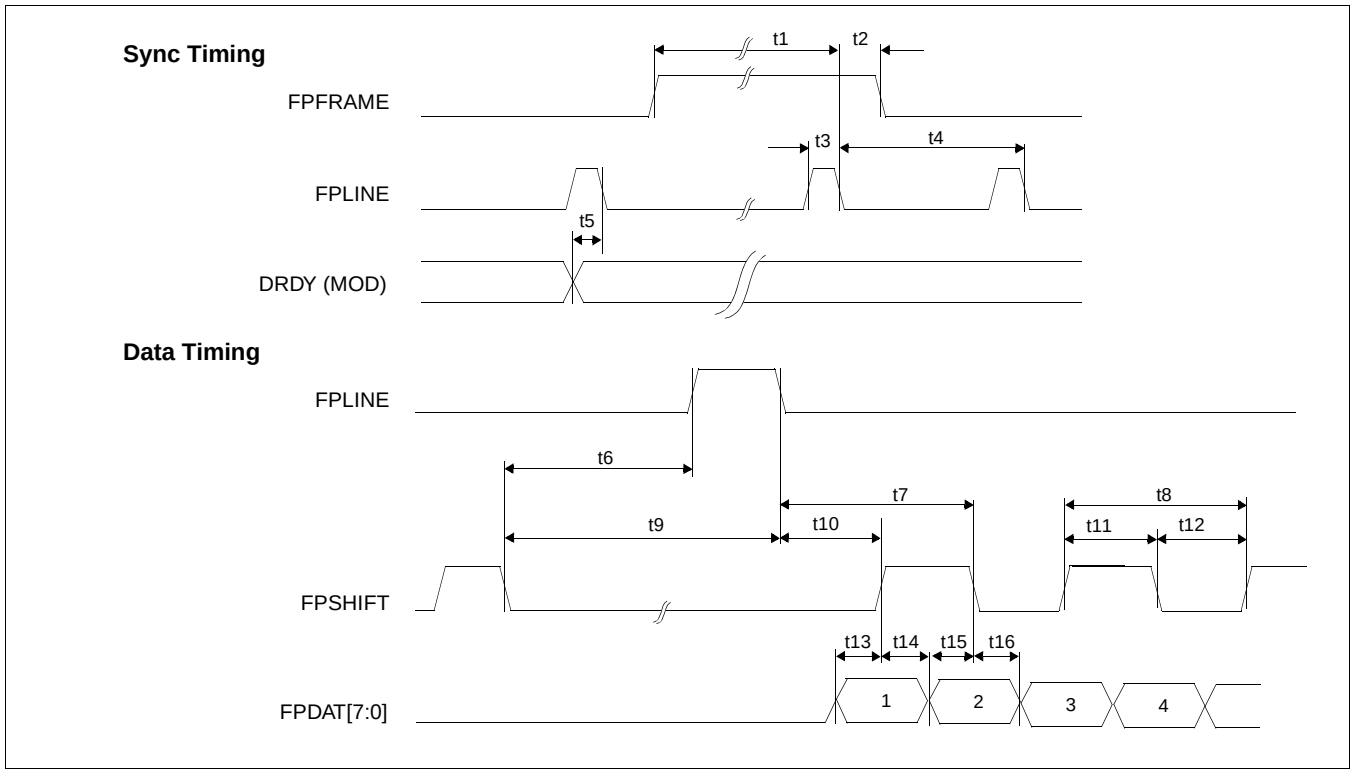

Figure 7-36: Single Color 16-Bit Panel (with External Circuit) A.C. Timing

Table 7-28: Single Color 16-Bit Panel (with External Circuit) A.C. Timing

Symbol	Parameter	Min. Setting	Nominal	Max. Setting	Units
t1	FPFRAME setup to FPLINE falling edge	28	note 2	1268	Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge		12		Ts
t3	FPLINE pulse width		11		Ts
t4	FPLINE period	40	note 3	1280	Ts
t5	DRDY (MOD) delay from FPLINE falling edge	3	note 4	259	Ts
t6a	FPSHIFT falling edge to FPLINE rising edge, 4 bpp or 8 bpp	5	note 5	229	Ts
t6b	FPSHIFT falling edge to FPLINE rising edge, 15/16 bpp	7	note 5	231	Ts
t7a	FPLINE falling edge to FPSHIFT falling edge, 4 bpp or 8 bpp		22		Ts
t7b	FPLINE falling edge to FPSHIFT falling edge, 15/16 bpp		20		Ts
t8	FPSHIFT period		4		Ts
t9a	FPSHIFT falling edge to FPLINE falling edge, 4 bpp or 8 bpp	16	note 6	240	Ts
t9b	FPSHIFT falling edge to FPLINE falling edge, 15/16 bpp	18	note 6	242	Ts
t10a	FPLINE falling edge to FPSHIFT rising edge, 4 bpp or 8 bpp		20		Ts
t10b	FPLINE falling edge to FPSHIFT rising edge, 15/16 bpp		18		Ts
t11	FPSHIFT pulse width high		2		Ts
t12	FPSHIFT pulse width low		2		Ts
t13	FPDAT[7:0] setup to FPSHIFT rising edge		1		Ts
t14	FPDAT[7:0] hold to FPSHIFT rising edge		1		Ts
t15	FPDAT[7:0] setup to FPSHIFT falling edge		1		Ts
t16	FPDAT[7:0] hold to FPSHIFT falling edge		1		Ts

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. t1 = t4 - 12
3. t4 = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. t5 = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. t6 = [((REG[034h] bits [4:0]) + 1) × 8 - 27] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 25] for 15/16 bpp color depth
6. t9 = [((REG[034h] bits [4:0]) + 1) × 8 - 16] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 14] for 15/16 bpp color depth

7.5.8 Dual Monochrome 8-Bit Panel Timing

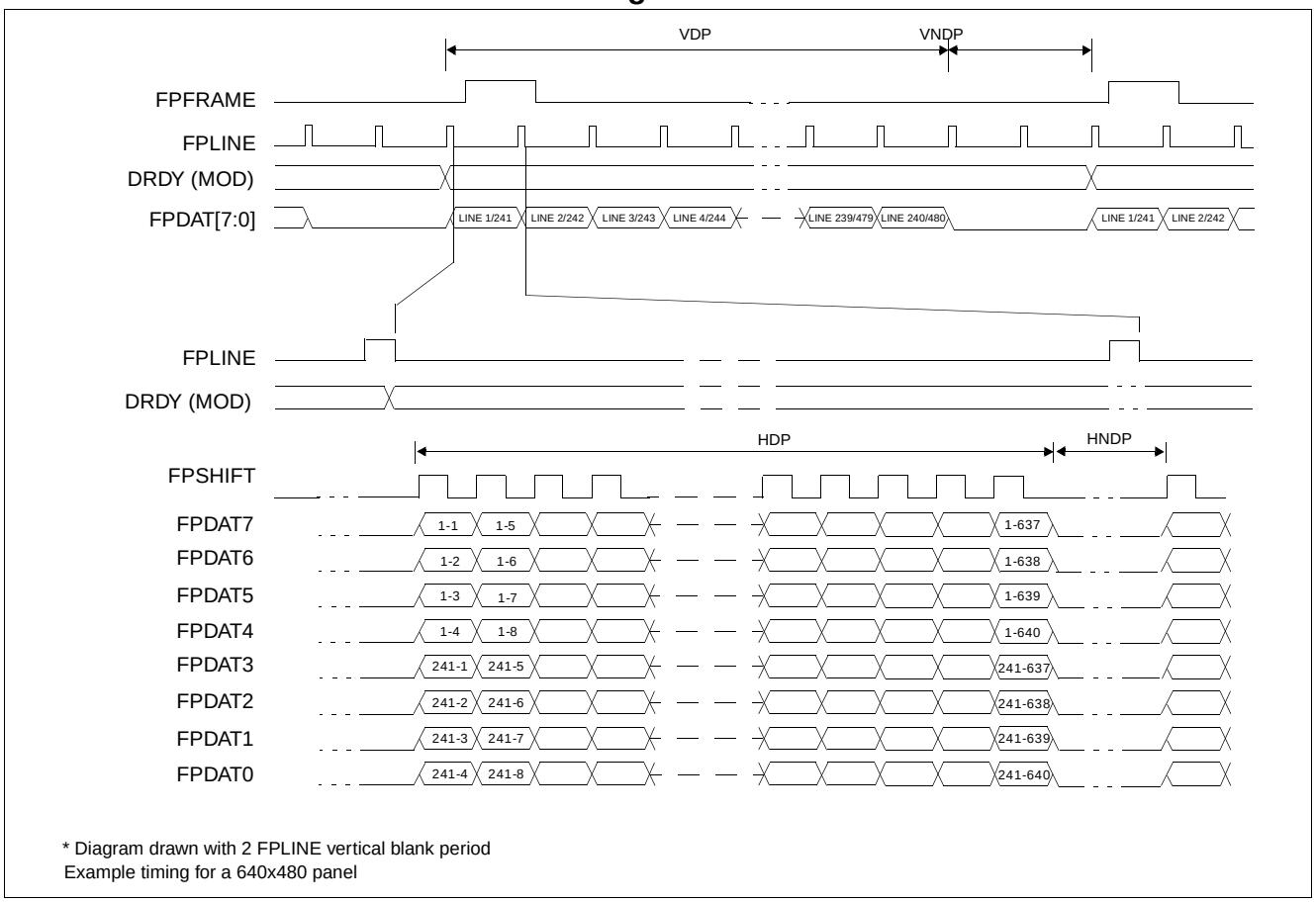

Figure 7-37: Dual Monochrome 8-Bit Panel Timing

VDP = Vertical Display Period = (REG[039h] bits [1:0], REG[038h] bits [7:1])
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8 Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8 Ts

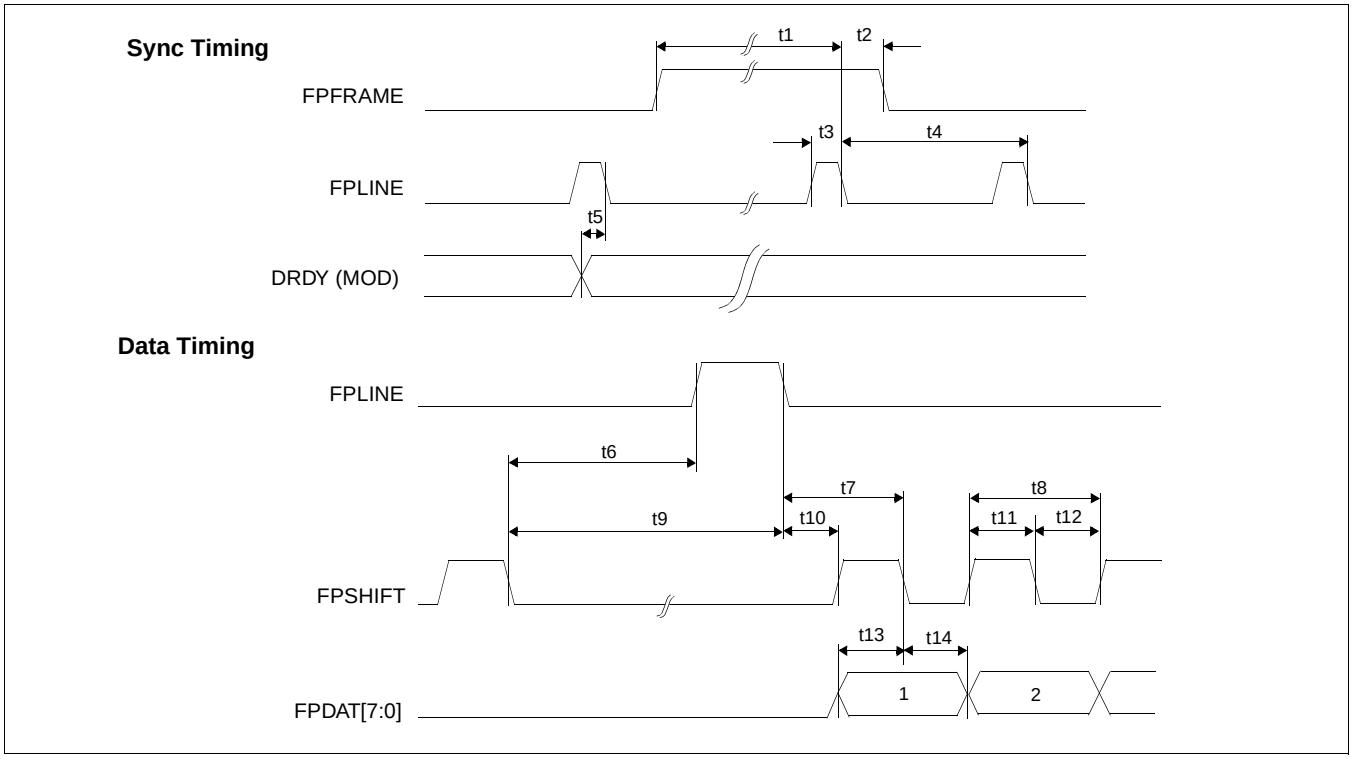

Figure 7-38: Dual Monochrome 8-Bit Panel A.C. Timing

Table 7-29: Dual Monochrome 8-Bit Panel A.C. Timing

Symbol	Parameter	Min. Setting	Typical	Max. Setting	Units
t1	FPFRAME setup to FPLINE falling edge	28	note 2	1268	Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge		12		Ts
t3	FPLINE pulse width		11		Ts
t4	FPLINE period	40	note 3	1280	Ts
t5	DRDY (MOD) delay from FPLINE falling edge	3	note 4	259	Ts
t6a	FPSHIFT falling edge to FPLINE rising edge, 4 bpp or 8 bpp	13	note 5	237	Ts
t6b	FPSHIFT falling edge to FPLINE rising edge, 15/16 bpp	15	note 5	239	Ts
t7a	FPLINE falling edge to FPSHIFT falling edge, 4 bpp or 8 bpp		12		Ts
t7b	FPLINE falling edge to FPSHIFT falling edge, 15/16 bpp		10		Ts
t8	FPSHIFT period		4		Ts
t9a	FPSHIFT falling edge to FPLINE falling edge, 4 bpp or 8 bpp	24	note 6	248	Ts
t9b	FPSHIFT falling edge to FPLINE falling edge, 15/16 bpp	26	note 6	250	Ts
t10a	FPLINE falling edge to FPSHIFT rising edge, 4 bpp or 8 bpp		10		Ts
t10b	FPLINE falling edge to FPSHIFT rising edge, 15/16 bpp		8		Ts
t12	FPSHIFT pulse width low		2		Ts
t11	FPSHIFT pulse width high		2		Ts
t13	FPDAT[7:0] setup to FPSHIFT falling edge		2		Ts
t14	FPDAT[7:0] hold to FPSHIFT falling edge		2		Ts

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. t1 = t4 - 12
3. t4 = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. t5 = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. t6 = [((REG[034h] bits [4:0]) + 1) × 8 - 19] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 17] for 15/16 bpp color depth
6. t9 = [((REG[034h] bits [4:0]) + 1) × 8 - 8] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 6] for 15/16 bpp color depth

7.5.9 Dual Color 8-Bit Panel Timing

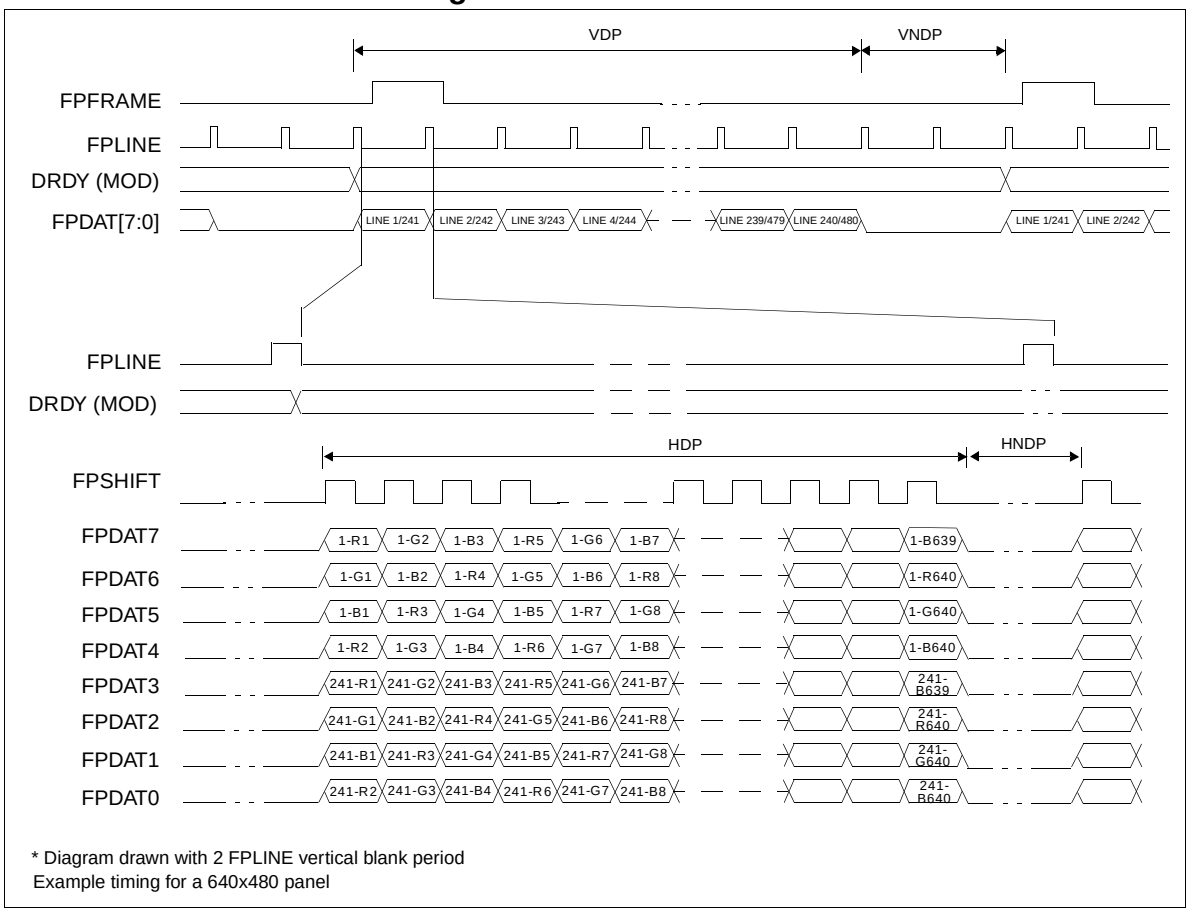

Figure 7-39: Dual Color 8-Bit Panel Timing

VDP = Vertical Display Period = ((REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1) /2
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8 Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8 Ts

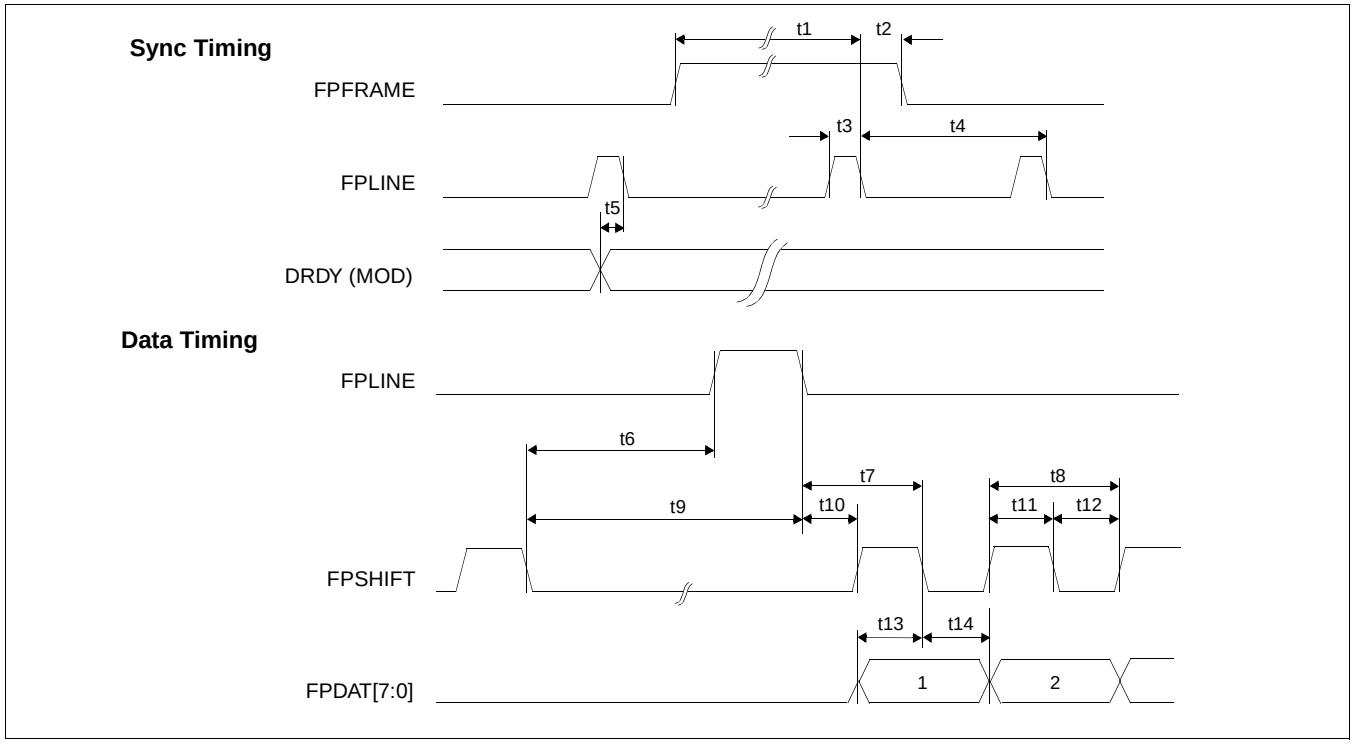

Figure 7-40: Dual Color 8-Bit Panel A.C. Timing

Table 7-30: Dual Color 8-Bit Panel A.C. Timing

Symbol	Parameter	Min. Setting	Typical	Max. Setting	Units
t1	FPFRAME setup to FPLINE falling edge	28	note 2	1268	Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge		12		Ts
t3	FPLINE pulse width		11		Ts
t4	FPLINE period	40	note 3	1280	Ts
t5	DRDY (MOD) delay from FPLINE falling edge	3	note 4	259	Ts
t6a	FPSHIFT falling edge to FPLINE rising edge, 4 bpp or 8 bpp	12	note 5	236	Ts
t6b	FPSHIFT falling edge to FPLINE rising edge, 15/16 bpp	14	note 5	238	Ts
t7a	FPLINE falling edge to FPSHIFT falling edge, 4 bpp or 8 bpp		10.5		Ts
t7b	FPLINE falling edge to FPSHIFT falling edge, 15/16 bpp		8.5		Ts
t8	FPSHIFT period		1		Ts
t9a	FPSHIFT falling edge to FPLINE falling edge, 4 bpp or 8 bpp	23	note 6	247	Ts
t9b	FPSHIFT falling edge to FPLINE falling edge, 15/16 bpp	25	note 6	249	Ts
t10a	FPLINE falling edge to FPSHIFT rising edge, 4 bpp or 8 bpp		11		Ts
t10b	FPLINE falling edge to FPSHIFT rising edge, 15/16 bpp		9		Ts
t11	FPSHIFT pulse width high		0.5		Ts
t12	FPSHIFT pulse width low		0.5		Ts
t13	FPDAT[7:0] setup to FPSHIFT falling edge		0.5		Ts
t14	FPDAT[7:0] hold to FPSHIFT falling edge		0.5		Ts

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. t1 = t4 - 12
3. t4 = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. t5 = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. t6 = [((REG[034h] bits [4:0]) + 1) × 8 - 20] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 18] for 15/16 bpp color depth
6. t9 = [((REG[034h] bits [4:0]) + 1) × 8 - 9] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 7] for 15/16 bpp color depth

7.5.10 Dual Color 16-Bit Panel Timing

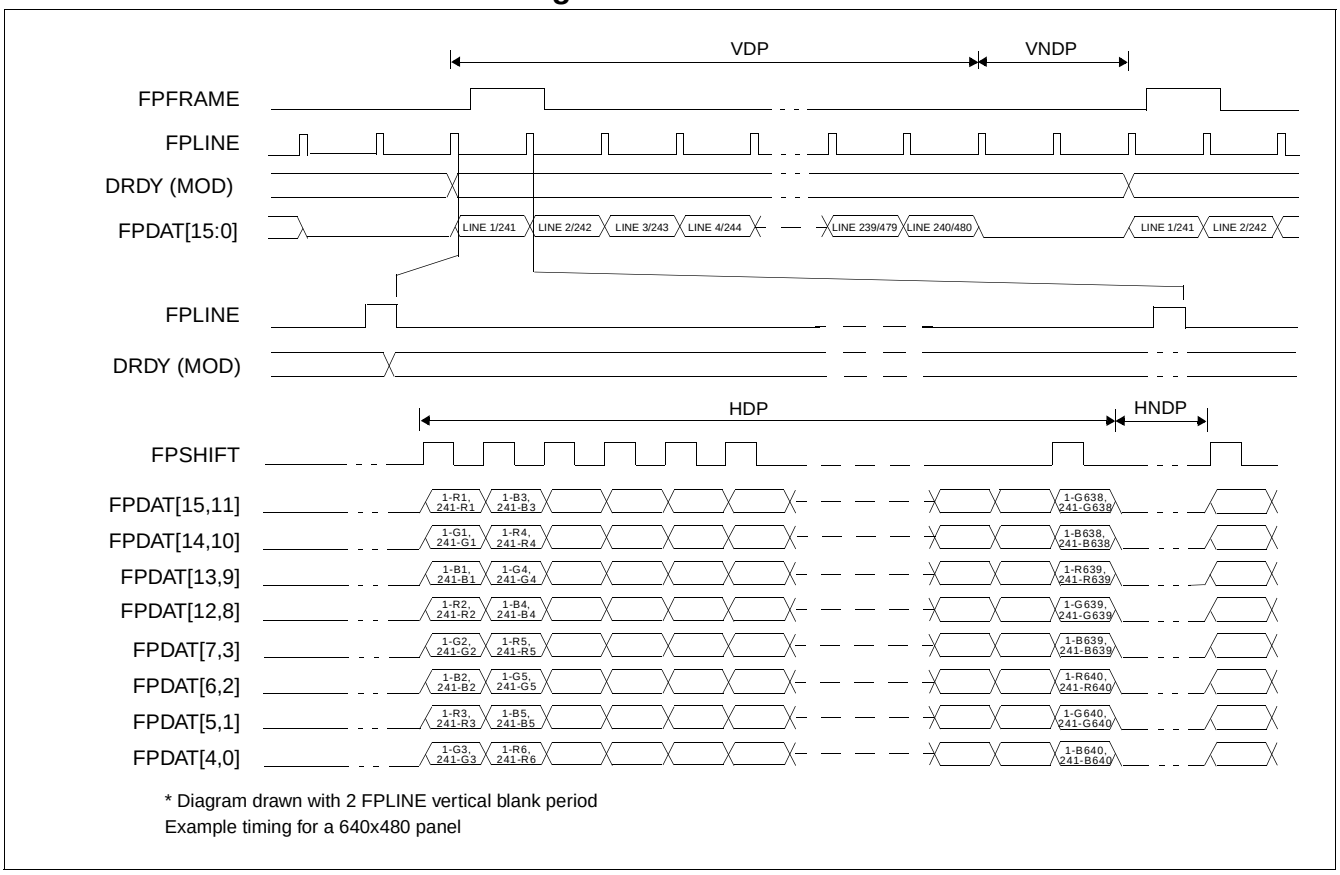

Figure 7-41: Dual Color 16-Bit Panel Timing

VDP = Vertical Display Period = ((REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1) /2
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8 Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8 Ts

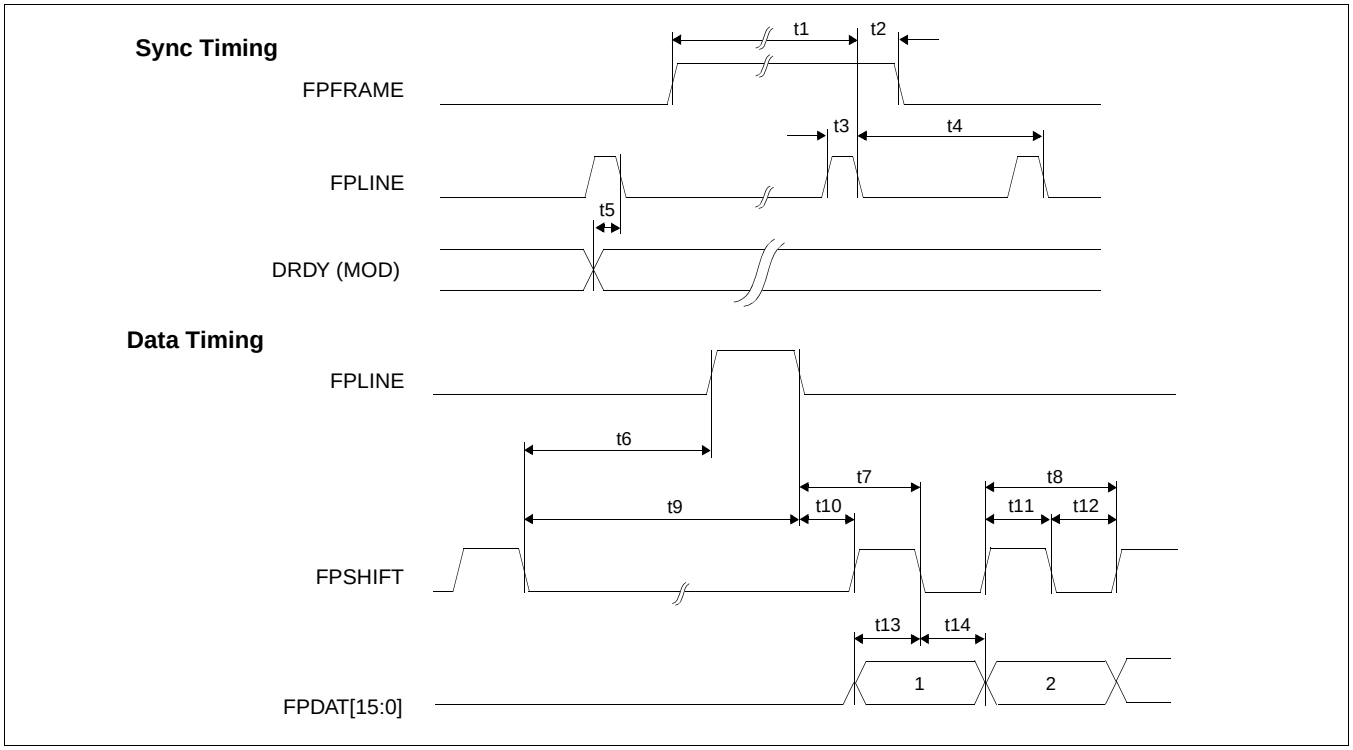

Figure 7-42: Dual Color 16-Bit Panel A.C. Timing

Table 7-31: Dual Color 16-Bit Panel A.C. Timing

Symbol	Parameter	Min. Setting	Typical	Max. Setting	Units
t1	FPFRAME setup to FPLINE falling edge	28	note 2	1268	Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge		12		Ts
t3	FPLINE pulse width		11		Ts
t4	FPLINE period	40	note 3	1280	Ts
t5	DRDY (MOD) delay from FPLINE falling edge	3	note 4	259	Ts
t6a	FPSHIFT falling edge to FPLINE rising edge, 4 bpp or 8 bpp	12	note 5	236	Ts
t6b	FPSHIFT falling edge to FPLINE rising edge, 15/16 bpp	14	note 5	238	Ts
t7a	FPLINE falling edge to FPSHIFT falling edge, 4 bpp or 8 bpp		12		Ts
t7b	FPLINE falling edge to FPSHIFT falling edge, 15/16 bpp		10		Ts
t8	FPSHIFT period		2		Ts
t9a	FPSHIFT falling edge to FPLINE falling edge, 4 bpp or 8 bpp	23	note 6	247	Ts
t9b	FPSHIFT falling edge to FPLINE falling edge, 15/16 bpp	25	note 6	249	Ts
t10a	FPLINE falling edge to FPSHIFT rising edge, 4 bpp or 8 bpp		10		Ts
t10b	FPLINE falling edge to FPSHIFT rising edge, 15/16 bpp		8		Ts
t11	FPSHIFT pulse width high		1		Ts
t12	FPSHIFT pulse width low		1		Ts
t13	FPDAT[15:0] setup to FPSHIFT falling edge		1		Ts
t14	FPDAT[15:0] hold to FPSHIFT falling edge		1		Ts

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. t1 = t4 - 12
3. t4 = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. t5 = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. t6 = [((REG[034h] bits [4:0]) + 1) × 8 - 20] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 18] for 15/16 bpp color depth
6. t9 = [((REG[034h] bits [4:0]) + 1) × 8 - 9] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 7] for 15/16 bpp color depth

7.5.11 Dual Color 16-Bit Panel Timing with External Circuit

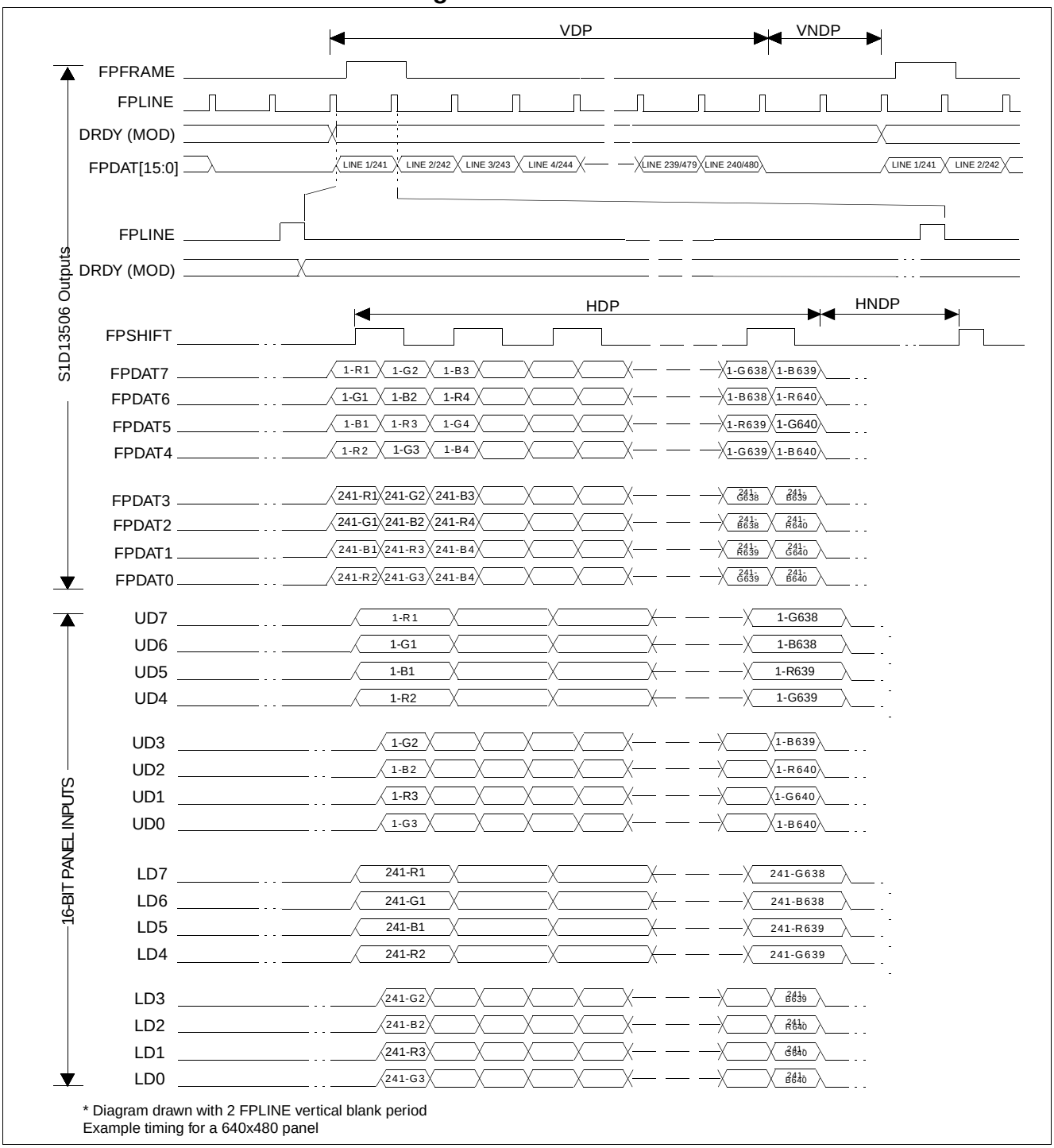

Figure 7-43: 16-Bit Dual Color Panel Timing with External Circuit

VDP	= Vertical Display Period	= ((REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1) /2
VNDP	= Vertical Non-Display Period	= (REG[03Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[032h] bits [6:0]) + 1) × 8 Ts
HNDP	= Horizontal Non-Display Period	= ((REG[034h] bits [4:0]) + 1) × 8 Ts

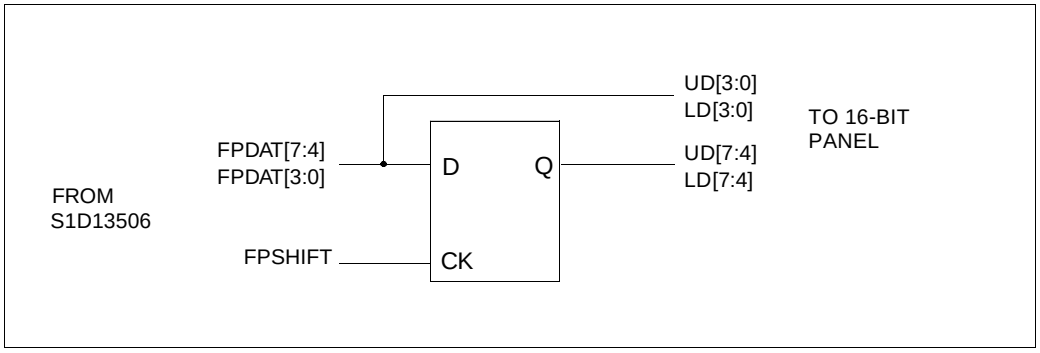

Figure 7-44: External Circuit for Color Dual 16-Bit Panel When the Media Plug is Enabled

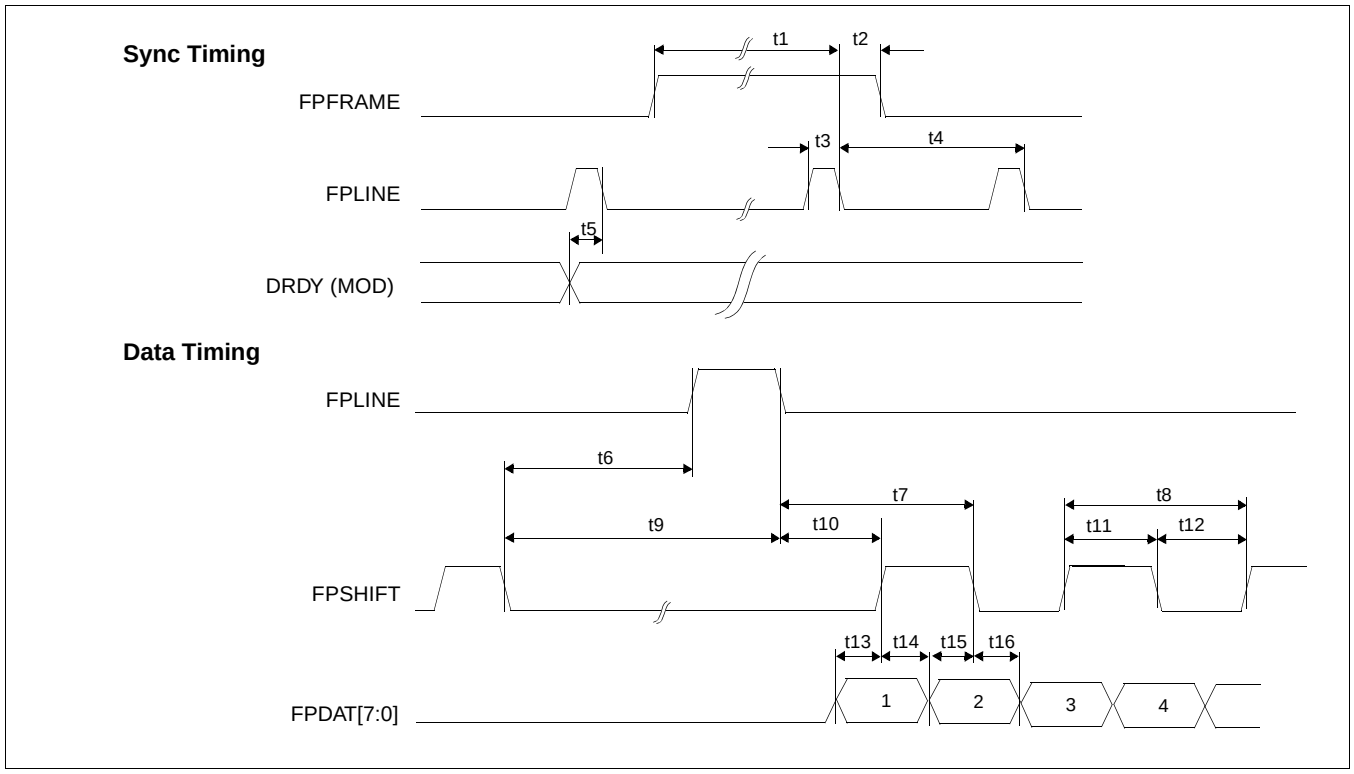

Figure 7-45: Dual Color 16-Bit Panel (with External Circuit) A.C. Timing

Table 7-32: Dual Color 16-Bit Panel (with External Circuit) A.C. Timing

Symbol	Parameter	Min. Setting	Typical	Max. Setting	Units
t1	FPFRAME setup to FPLINE falling edge	28	note 2	1268	Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge		12		Ts
t3	FPLINE pulse width		11		Ts
t4	FPLINE period	40	note 3	1280	Ts
t5	DRDY (MOD) delay from FPLINE falling edge	3	note 4	259	Ts
t6a	FPSHIFT falling edge to FPLINE rising edge, 4 bpp or 8 bpp	12.5	note 5	236.5	Ts
t6b	FPSHIFT falling edge to FPLINE rising edge, 15/16 bpp	14.5	note 5	238.5	Ts
t7a	FPLINE falling edge to FPSHIFT falling edge, 4 bpp or 8 bpp		12.5		Ts
t7b	FPLINE falling edge to FPSHIFT falling edge, 15/16 bpp		10.5		Ts
t8	FPSHIFT period		2		Ts
t9a	FPSHIFT falling edge to FPLINE falling edge, 4 bpp or 8 bpp	23.5	note 6	247.5	Ts
t9b	FPSHIFT falling edge to FPLINE falling edge, 15/16 bpp	25.5	note 6	249.5	Ts
t10a	FPLINE falling edge to FPSHIFT rising edge, 4 bpp or 8 bpp		11.5		Ts
t10b	FPLINE falling edge to FPSHIFT rising edge, 15/16 bpp		9.5		Ts
t11	FPSHIFT pulse width high		1		Ts
t12	FPSHIFT pulse width low		1		Ts
t13	FPDAT[7:0] setup to FPSHIFT rising edge		0.5		Ts
t14	FPDAT[7:0] hold to FPSHIFT rising edge		0.5		Ts
t15	FPDAT[7:0] setup to FPSHIFT falling edge		0.5		Ts
t16	FPDAT[7:0] hold to FPSHIFT falling edge		0.5		Ts

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. t1 = t4 - 12
3. t4 = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. t5 = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. t6 = [((REG[034h] bits [4:0]) + 1) × 8 - 19.5] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 17.5] for 15/16 bpp color depth
6. t9 = [((REG[034h] bits [4:0]) + 1) × 8 - 8.5] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 6.5] for 15/16 bpp color depth

7.5.12 TFT/D-TFD Panel Timing

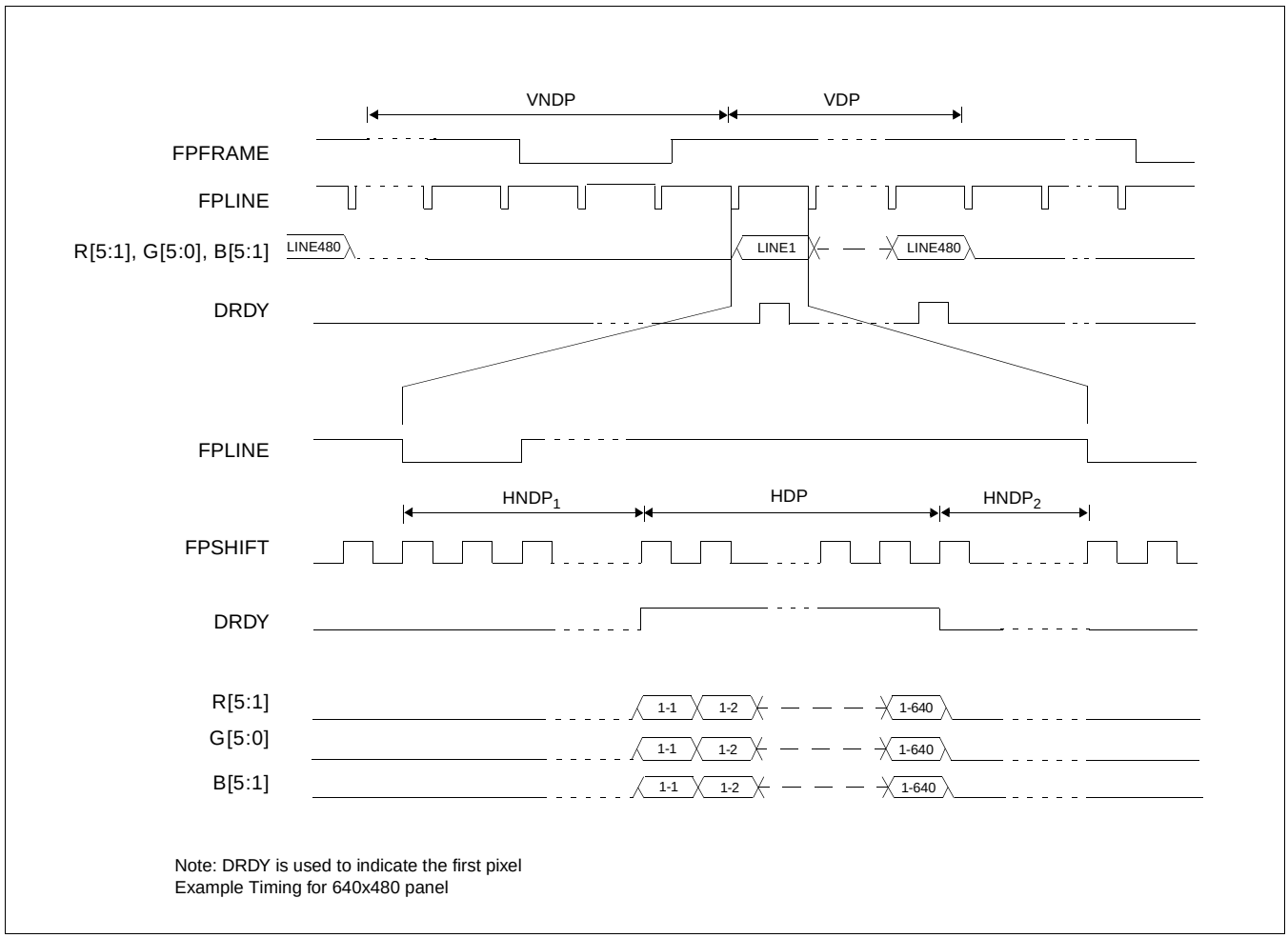

Figure 7-46: TFT/D-TFD Panel Timing

VDP	= Vertical Display Period	= (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[03Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[032h] bits [6:0]) + 1) × 8 Ts
HNDP	= Horizontal Non-Display Period	= $HNDP_1$ + $HNDP_2$ = ((REG[034h] bits [4:0]) + 1) × 8 Ts

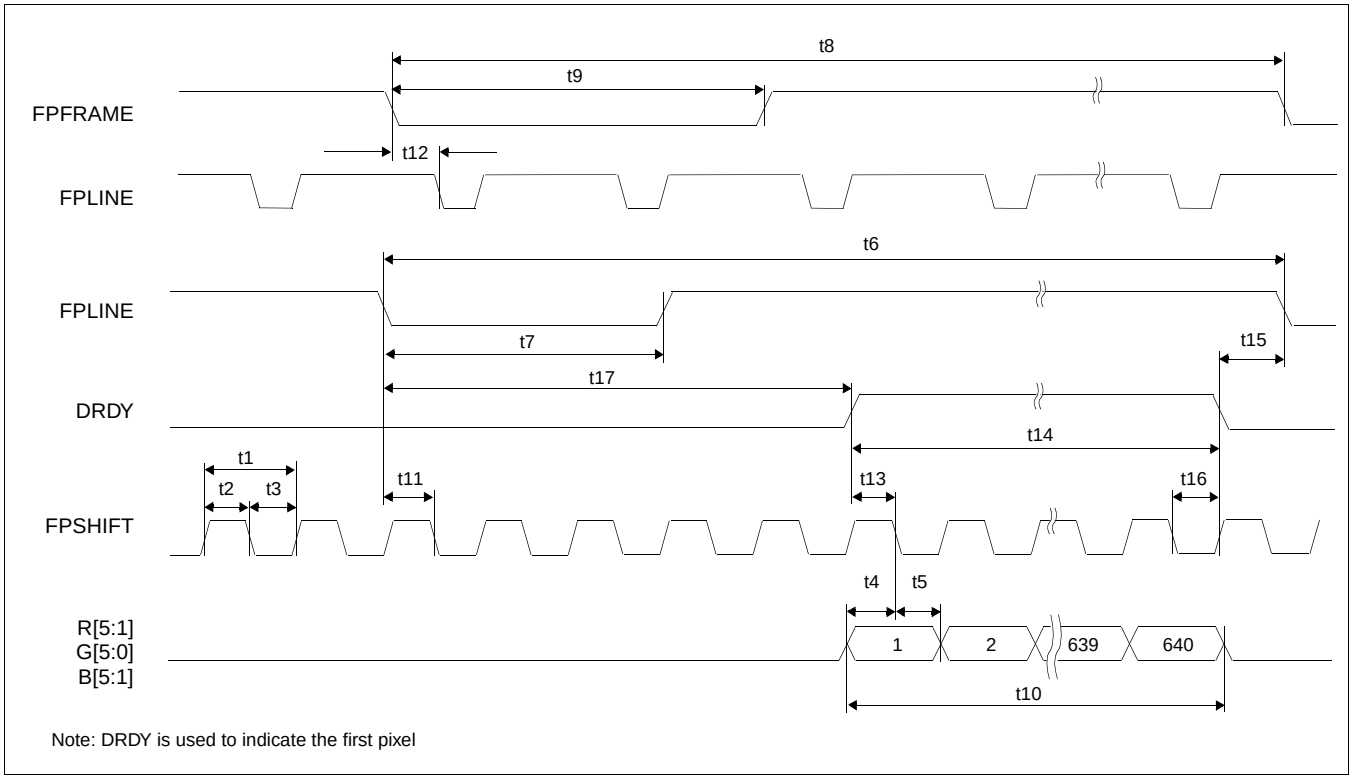

Figure 7-47: TFT/D-TFD A.C. Timing

Table 7-33: TFT/D-TFD A.C. Timing

Symbol	Parameter	Min. Setting	Typical	Max. Setting	Units
t1	FPSHIFT period		1		Ts (note 1)
t2	FPSHIFT pulse width high		0.5		Ts
t3	FPSHIFT pulse width low		0.5		Ts
t4	data setup to FPSHIFT falling edge		0.5		Ts
t5	data hold from FPSHIFT falling edge		0.5		Ts
t6	FPLINE cycle time	40	note 2	1280	Ts
t7	FPLINE pulse width low	8	note 3	128	Ts
t8	FPFRAME cycle time	2	note 4	1088	lines
t9	FPFRAME pulse width low	1	note 5	8	lines
t10	horizontal display period	8	note 6	1024	Ts
t11	FPLINE setup to FPSHIFT falling edge		0.5		Ts
t12	FPFRAME falling edge to FPLINE falling edge phase difference	1	note 7	249	Ts
t13	DRDY to FPSHIFT falling edge setup time		0.5		Ts
t14	DRDY pulse width	8	note 8	1024	Ts
t15a	DRDY falling edge to FPLINE falling edge, 4 bpp or 8 bpp	4	note 9	252	Ts
t15b	DRDY falling edge to FPLINE falling edge, 15/16 bpp	6	note 9	254	Ts
t16	DRDY hold from FPSHIFT falling edge		0.5		Ts
t17a	FPLINE Falling edge to DRDY active, 4 bpp or 8 bpp	-6	note 10	250	Ts
t17b	FPLINE Falling edge to DRDY active, 15/16 bpp	-8	note 10	248	Ts

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. t6 = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
3. t7 = [((REG[036h] bits [3:0]) + 1) × 8]
4. t8 = [((REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1) + ((REG[03Ah] bits [5:0]) + 1)]
5. t9 = [((REG[03Ch] bits [2:0]) + 1)]
6. t10 = [((REG[032h] bits [6:0]) + 1) × 8]
7. t12 = [(REG[035h] bits [4:0]) × 8 + 1]
8. t14 = [((REG[032h] bits [6:0]) + 1) × 8]
9. t15 = [(REG[035h] bits [4:0]) × 8 + 4] for 4 bpp or 8 bpp color depth
   = [(REG[035h] bits [4:0]) × 8 + 6] for 15/16 bpp color depth
10. t17 = [((REG[034h] bits [4:0]) + 1) × 8 - (REG[035h] bits [4:0]) × 8 - 4] for 4 bpp or 8 bpp color depth
    = [((REG[034h] bits [4:0]) + 1) × 8 - (REG[035h] bits [4:0]) × 8 - 6] for 15/16 bpp color depth

7.5.13 CRT Timing

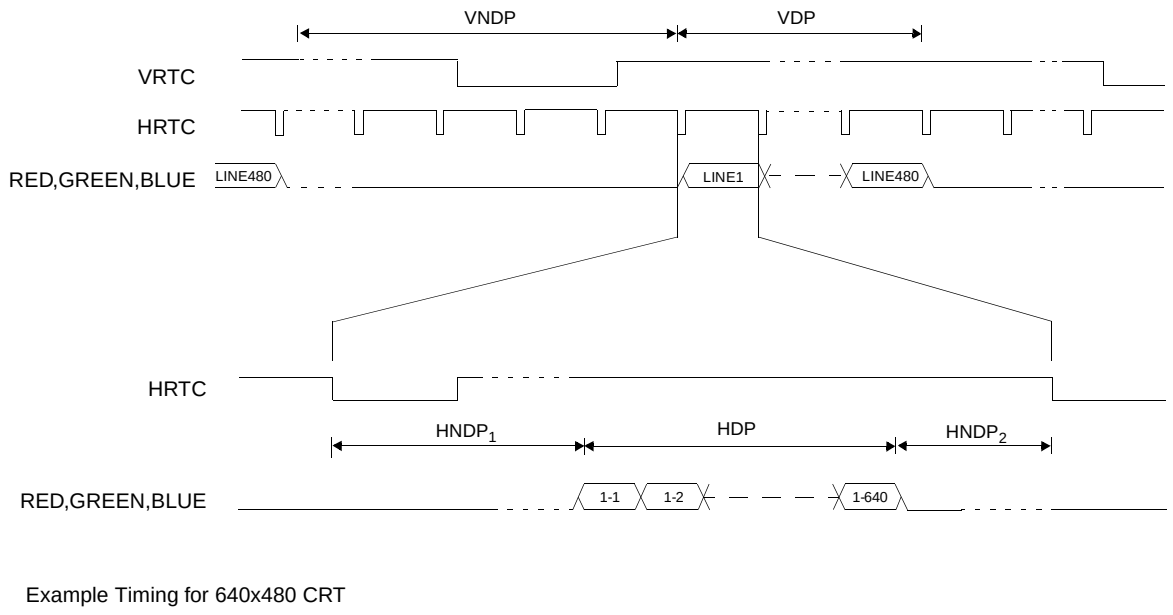

Figure 7-48: CRT Timing

VDP	= Vertical Display Period	= (REG[057h] bits [1:0], REG[056h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[058h] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[050h] bits [6:0]) + 1) × 8 Ts
HNDP	= Horizontal Non-Display Period	= $HNDP_1$ + $HNDP_2$= ((REG[052h] bits [5:0]) + 1) × 8 Ts

Note

The signals RED, GREEN and BLUE are analog signals from the embedded DAC and represent the color components which make up each pixel.

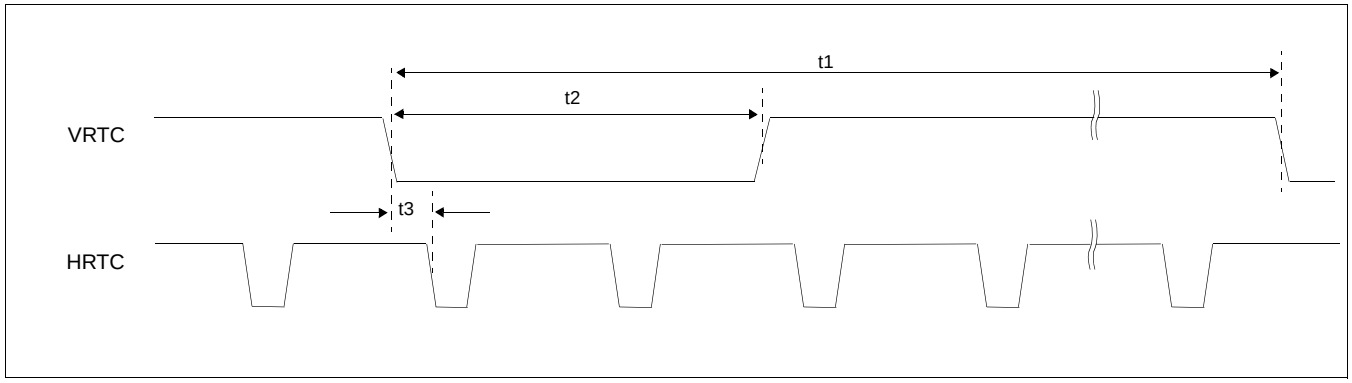

Figure 7-49: CRT A.C. Timing

Table 7-34: CRT A.C. Timing

Symbol	Parameter	Min. Setting	Typical	Max. Setting	Units
t1	VRTC cycle time	2	note 1	1152	lines
t2	VRTC pulse width low	1	note 2	8	lines
t3	VRTC falling edge to FPLINE falling edge phase difference	8	note 3	512	Ts

1. t1 = [((REG[057h] bits 1:0, REG[056h] bits 7:0) + 1) + ((REG[058h] bits 6:0) + 1)] lines
2. t2 = [((REG[05Ah] bits 2:0) + 1)] lines
3. t3 = [((REG[053h] bits 5:0) + 1) × 8] Ts

7.6 TV Timing

7.6.1 TV Output Timing

The overall NTSC and PAL video timing is shown in Figure 7-50: and Figure 7-51: respectively.

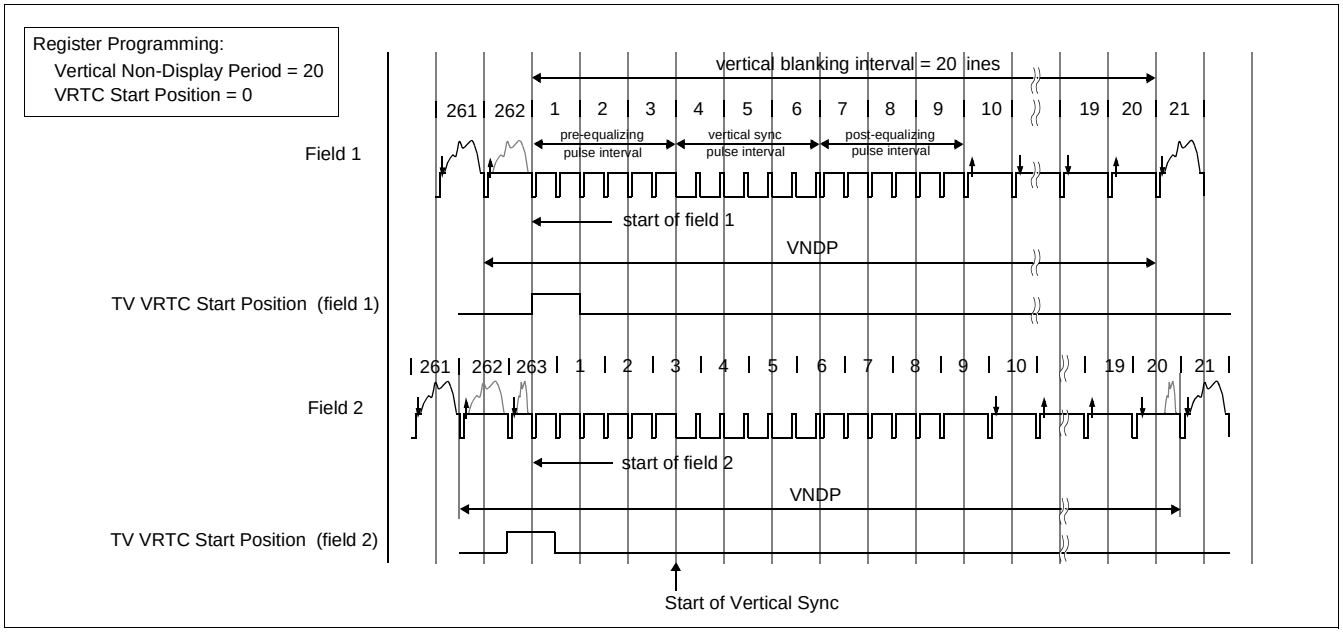

Figure 7-50: NTSC Video Timing

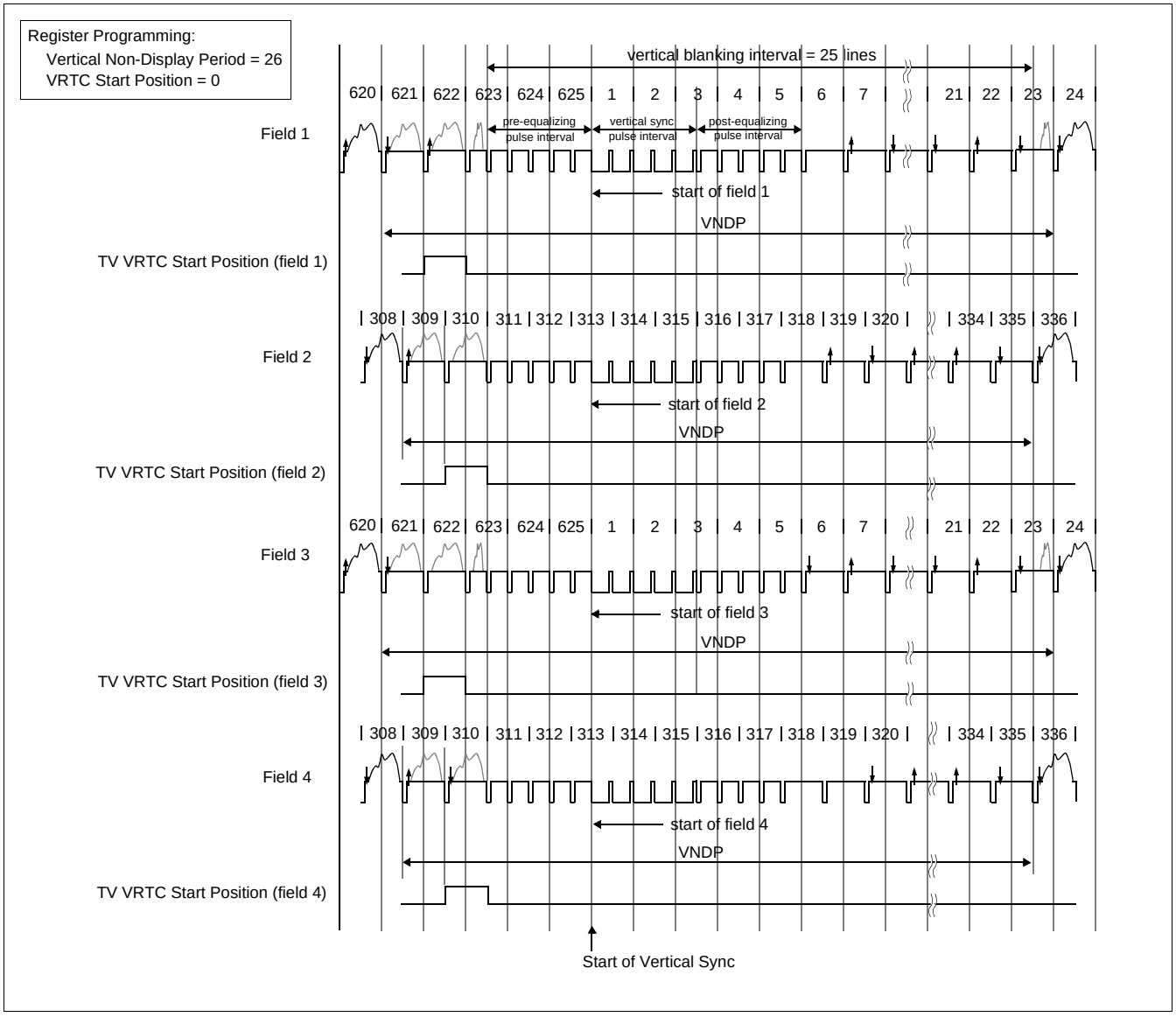

Figure 7-51: PAL Video Timing

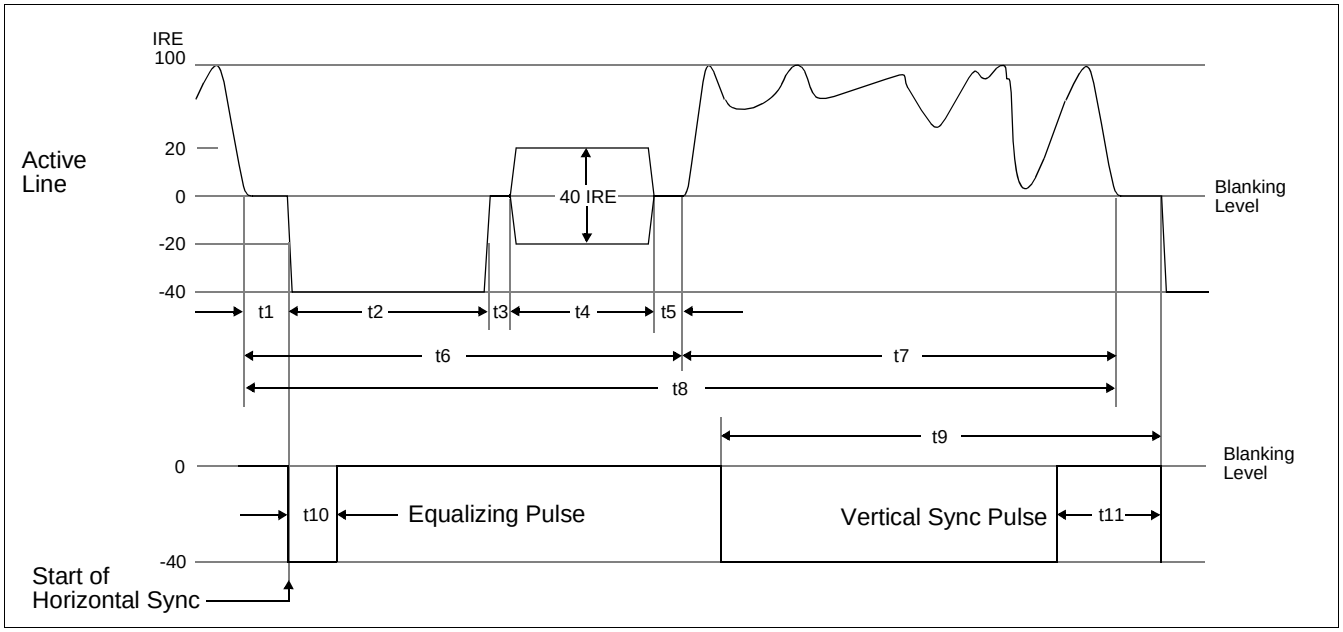

Figure 7-52: Horizontal Timing for NTSC/PAL

Table 7-35: Horizontal Timing for NTSC/PAL

Symbol	Parameter	NTSC	PAL	Units
T_{4SC}	(4x Subcarrier clock) period	69.841	56.387	ns
t1	Front Porch	note 1	note 1	T_{4SC}
t2	Horizontal Sync	67	83	T_{4SC}
t3	Breezeway	9	16	T_{4SC}
t4	Color Burst	39	44	T_{4SC}
t5	Color Back Porch	note 2	note 3	T_{4SC}
t6	Horizontal Blanking	note 4	note 5	T_{4SC}
t7	Active Video	note 6	note 6	T_{4SC}
t8	Line Period	910	1135	T_{4SC}
t9	Half Line Period	455	568 / 567	T_{4SC}
t10	Equalizing Pulse	33	41	T_{4SC}
t11	Vertical Serration	67	83	T_{4SC}

1. t1 = ((REG[053] bits[5:0]) + 1) x 8 - 7 (4 bpp, 8 bpp modes)
   = ((REG[053] bits[5:0]) + 1) x 8 - 5 (15/16 bpp modes)
2. $t5_{NTSC}$ = (((REG[052] bits[5:0]) x 8) + 6) - (((REG[053] bits[5:0]) + 1) x 8) - 108 (4 bpp, 8 bpp modes)
   = (((REG[052] bits[5:0]) x 8) + 6) - (((REG[053] bits[5:0]) + 1) x 8) - 110 (15/16 bpp modes)
3. $t5_{PAL}$ = (((REG[052] bits[5:0]) x 8) + 7) - (((REG[053] bits[5:0]) + 1) x 8) - 136 (4 bpp, 8 bpp modes)
   = (((REG[052] bits[5:0]) x 8) + 7) - (((REG[053] bits[5:0]) + 1) x 8) - 138 (15/16 bpp modes)
4. $t6_{NTSC}$ = ((REG[052] bits[5:0]) x 8) + 6
5. $t6_{PAL}$ = ((REG[052] bits[5:0]) x 8) + 7
6. t7 = ((REG[050] bits[6:0]) + 1) x 8

Important:

REG[050] and REG[052] must be programmed to satisfy the Line Period (t8).

For NTSC, (((REG[050] bits[6:0]) + 1) x 8) + (((REG[052] bits[5:0]) x 8) + 6) = 910.

For PAL, (((REG[050] bits[6:0]) + 1) x 8) + (((REG[052] bits[5:0]) x 8) + 7) = 1135.

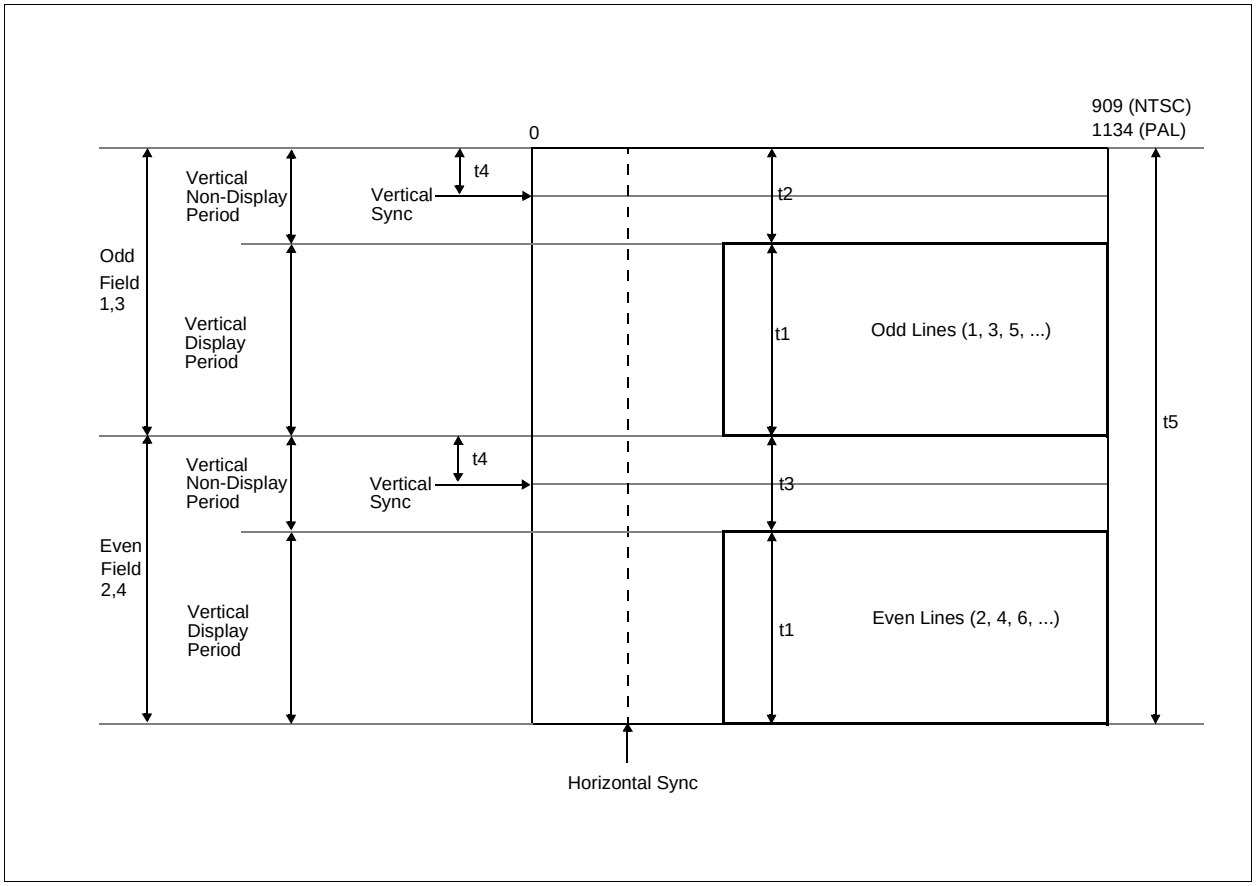

Figure 7-53: Vertical Timing for NTSC/PAL

Table 7-36: Vertical Timing for NTSC/PAL

Symbol	Parameter	NTSC	PAL	Units
T_{LINE}	Line Period	63.55556	63.99964	us
t1	Vertical Field Period	note 1	note 1	T_{LINE}
t2	Vertical Blanking (Fields 1, 3)	note 2	note 2	T_{LINE}
t3	Vertical Blanking (Fields 2, 4)	note 3	note 3	T_{LINE}
t4	Vertical Sync Position	note 4	note 5	T_{LINE}
t5	Frame Period	525	625	T_{LINE}

1. t1 = ({(REG[057] bits[1:0]), (REG[056] bits[7:0])} + 1) / 2
2. t2 = ((REG[058] bits[6:0]) + 1) for fields 1 & 3
3. t3 = ((REG[058] bits[6:0]) + 2) for fields 2 & 4
4. $t4_{NTSC}$ = ((REG[059] bits[6:0]) + 4) for field 1
   = ((REG[059] bits[6:0]) + 4.5) for field 2
5. $t4_{PAL}$ = ((REG[059] bits[6:0]) + 5) for field 1 and field 3
   = ((REG[059] bits[6:0]) + 4.5) for field 2 and field 4

Important

REG[056], REG[057], and REG[058] must be programmed to satisfy the Frame Period (t5).

For NTSC, ({(REG[057] bits[1:0]), (REG[056] bits[7:0])} + 1) + ((REG[058] bits[6:0]) + 1) x 2 + 1) = 525
For PAL, ({(REG[057] bits[1:0]), (REG[056] bits[7:0])} + 1) + ((REG[058] bits[6:0]) + 1) x 2 + 1) = 625.

7.7 MediaPlug Interface Timing

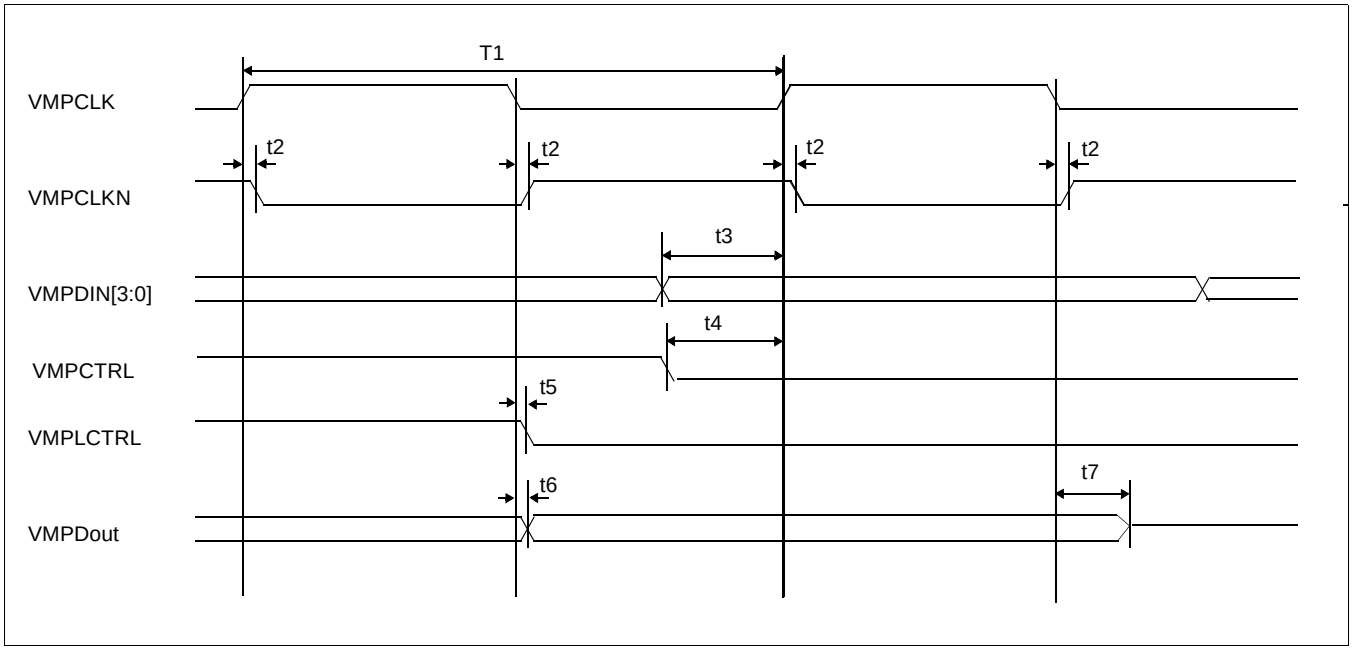

Figure 7-54: MediaPlug A.C. Timing

Note
The above timing diagram assumes no load.

Table 7-37: MediaPlug A.C. Timing

Symbol	Parameter	Min	Max	Units
T1	MediaPlug clock period	100		ns
t2	VMPCLKN delay from VMPCLK	0	3	ns
t3	Input data setup	6		ns
t4	VMPCTRL setup	6		
t5	Local control signal delay from VMPCLK falling edge		2	ns
t6	Output data delay from VMPCLK falling edge		1	ns
t7	Output data tristate delay from VMPCLK falling edge		14	ns

8 Registers

This section discusses how and where to access the S1D13506 registers. It also provides detailed information about the layout and usage of each register.

8.1 Initializing the S1D13506

Before programming the S1D13506 registers, the Register/Memory Select bit (REG[000h] bit 7) must be set.

8.1.1 Register/Memory Select Bit

At reset, the Register/Memory Select bit is set to 1. This means that only REG[000h] (read-only) and REG[001h] are accessible **until a write to REG[001h] sets bit 7 to 0 making all registers and memory accessible**. When debugging a new hardware design, this can sometimes give the appearance that the interface is not working, so it is important to remember to clear this bit before proceeding with debugging.

8.2 Register Mapping

The S1D13506 registers are memory-mapped. When the system decodes the input pins as CS# = 0 and M/R# = 0, the registers may be accessed. The register space is decoded by A20-A0.

When A20 = 1 the BitBLT data register ports are decoded allowing the system to access the display buffer through the 2D BitBLT engine using address lines A19-A0. When A20 = 0 and A12 = 0 the registers are decoded using A8-A0 as an index. When A20 = 0 and A12 = 1 the MediaPlug register ports are decoded using A11-A0.

The MediaPlug register ports are defined only when configuration input MD13 = 1 on reset. When MD13 = 0 on reset, A12 is always treated as 0 and the MediaPlug register space is not available - see Table 5-6:, “Summary of Power-On/Reset Options,” on page 31.

Table 8-1: “Register Mapping with CS# = 0 and M/R# = 0” shows the decoding for each register type.

Table 8-1: Register Mapping with CS# = 0 and M/R# = 0

Register Types (Range)	Address A20-A0 Decoding
BitBLT data registers (1M byte)	100000h to 1FFFFFh
MediaPlug registers (4K bytes)	1000h to 1FFFh
Main Registers (512 bytes)	0 to 1FFh

Note
The registers may be aliased within the allocated register space. If aliasing is undesirable, the register space must be fully decoded.

8.3 Register Descriptions

8.3.1 Basic Registers

Revision Code Register REG[000h]							RO
Product Code Bit 5	Product Code Bit 4	Product Code Bit 3	Product Code Bit 2	Product Code Bit 1	Product Code Bit 0	Revision Code Bit 1	Revision Code Bit 0

bits 7-2 Product Code Bits [5:0]
This is a read-only register that indicates the product code of the chip. The product code for S1D13506 is 000100b.

bits 1-0 Revision Code Bits [1:0]
This is a read-only register that indicates the revision code of the chip. The revision code is 01b.

Miscellaneous Register REG[001h]							RW
Register/ Memory Select	n/a	n/a	n/a	n/a	Reserved	Reserved	Reserved

bit 7 Register Memory Select
At reset, the Register/Memory Select bit is set to 1. This means that only REG[000h] (read-only) and REG[001h] are accessible **until a write to REG[001h] sets bit 7 to 0 making all registers and memory accessible**. When debugging a new hardware design, this can sometimes give the appearance that the interface is not working, so it is important to remember to clear this bit before proceeding with debugging.

bit 2 Reserved.
This bit must be set to 0.

bit 1 Reserved.
This bit must be set to 0.

bit 0 Reserved.
This bit must be set to 0.

8.3.2 General IO Pins Registers

General IO Pins Configuration Register REG[004h]							RW
Reserved	Reserved	Reserved	Reserved	GPIO3 Pin IO Config.	GPIO2 Pin IO Config.	GPIO1 Pin IO Config.	Reserved

bit 3 GPIO3 Pin IO Configuration
When this bit = 1, GPIO3 is configured as an output pin.
When this bit = 0 (default), GPIO3 is configured as an input pin.

Note
Note that MD[7:6] must be properly configured at the rising edge of RESET# to enable GPIO3, otherwise GPIO3 will be used as MA[9] for the DRAM and this bit will have no hardware effect. (See Table 8-2: “MA[11:9]/GPIO[1:3] Pin Functionality”).

bit 2 GPIO2 Pin IO Configuration
When this bit = 1, GPIO2 is configured as an output pin.
When this bit = 0 (default), GPIO2 is configured as an input pin.

Note
Note that MD[14] and MD[7:6] must be properly configured at the rising edge of RESET# to enable GPIO2, otherwise GPIO2 will be used as MA[11] for the DRAM or as the MediaPlug VMPEPWR output and this bit will have no hardware effect. (See Table 8-2: “MA[11:9]/GPIO[1:3] Pin Functionality”).

bit 1 GPIO1 Pin IO Configuration
When this bit = 1, GPIO1 is configured as an output pin.
When this bit = 0 (default), GPIO1 is configured as an input pin.

Note
Note that MD[7:6] must be properly configured at the rising edge of RESET# to enable GPIO1, otherwise GPIO1 will be used as MA[10] for the DRAM and this bit will have no hardware effect. (See Table 8-2: “MA[11:9]/GPIO[1:3] Pin Functionality”).

Table 8-2: MA[11:9]/GPIO[1:3] Pin Functionality

MD[14] on Reset	**MD[7:6] on Reset**	**Pin**		
		MA[9]/GPIO3	**MA[10]/GPIO1**	**MA[11]/GPIO2**
0	00	GPIO3	GPIO1	GPIO2
0	01	MA9	GPIO1	GPIO2
0	10	MA9	GPIO1	GPIO2
0	11	MA9	MA10	MA11
1	00	GPIO3	GPIO1	VMPEPWR
1	01	MA9	GPIO1	VMPEPWR
1	10	MA9	GPIO1	VMPEPWR
1	11	MA9	MA10	MA11

General IO Pins Control Register
REG[008h] RW

Reserved	Reserved	Reserved	Reserved	GPIO3 Pin IO Status	GPIO2 Pin IO Status	GPIO1 Pin IO Status	Reserved

bit 3 GPIO3 Pin IO Status
When GPIO3 is configured as an output, writing a 1 to this bit drives GPIO3 high and writing a 0 to this bit drives GPIO3 low.
When GPIO3 is configured as an input, a read from this bit returns the status of GPIO3.

Note
Note that MD[7:6] must be properly configured at the rising edge of RESET# to enable GPIO3, otherwise GPIO3 will be used as MA9 for the DRAM and this bit will have no hardware effect. (See Table 8-2: “MA[11:9]/GPIO[1:3] Pin Functionality”).

bit 2 GPIO2 Pin IO Status
When GPIO2 is configured as an output, writing a 1 to this bit drives GPIO2 high and writing a 0 to this bit drives GPIO2 low.
When GPIO2 is configured as an input, a read from this bit returns the status of GPIO2.

Note
Note that MD[14] and MD[7:6] must be properly configured at the rising edge of RESET# to enable GPIO2, otherwise GPIO2 will be used as MA11 for the DRAM or as the MediaPlug VMPEPWR output and this bit will have no hardware effect. (See Table 8-2: “MA[11:9]/GPIO[1:3] Pin Functionality”).

bit 1 GPIO1 Pin IO Status
When GPIO1 is configured as an output, writing a 1 to this bit drives GPIO1 high and writing a 0 to this bit drives GPIO1 low.
When GPIO1 is configured as an input, a read from this bit returns the status of GPIO1.

Note
Note that MD[7:6] must be properly configured at the rising edge of RESET# to enable GPIO1, otherwise GPIO1 will be used as MA10 for the DRAM and this bit will have no hardware effect. (See Table 8-2: “MA[11:9]/GPIO[1:3] Pin Functionality”).

8.3.3 MD Configuration Readback Registers

MD Configuration Status Register 0 REG[00Ch]							RO
MD[7] Config. Status	MD[6] Config. Status	MD[5] Config. Status	MD[4] Config. Status	MD[3] Config. Status	MD[2] Config. Status	MD[1] Config. Status	MD[0] Config. Status

MD Configuration Status Register 1 REG[00Dh]							RO
MD[15] Config. Status	MD[14] Config. Status	MD[13] Config. Status	MD[12] Config. Status	MD[11] Config. Status	MD[10] Config. Status	MD[9] Config. Status	MD[8] Config. Status

REG[00Ch] bits 7-0 MD[15:0] Configuration Status Bits [15:0]
REG[00Dh] bits 7-0 These read-only bits return the status of MD[15:0] at the rising edge of RESET#.

8.3.4 Clock Configuration Registers

Memory Clock Configuration Register REG[010h]							RW
n/a	n/a	n/a	MCLK Divide Select	n/a	n/a	n/a	MCLK Source Select

bit 4 MCLK Divide Select
When this bit = 1, the internal memory clock frequency is half of the MCLK source frequency.
When this bit = 0, the memory clock frequency is equal to the MCLK source frequency.

The MCLK frequency should always be set to the maximum frequency allowed by the DRAM. This provides maximum performance and minimizes overall system power consumption.

bit 0 MCLK Source Select
When this bit = 1, the source for the internal MCLK is derived from BUSCLK.
When this bit = 0, the source for MCLK is derived from CLKI.

Table 8-3: MCLK Source Select

MCLK Source Select	MCLK Source
0	CLKI
1	BUSCLK

Note
The MCLK Divide Select bit must be set to 1 before changing the MCLK Source Select bit.

Note
For further information on MCLK, refer to Section 20.2, “Clock Descriptions” on page 218.

LCD Pixel Clock Configuration Register
REG[014h] RW

n/a	n/a	LCD PCLK Divide Select Bit 1	LCD PCLK Divide Select Bit 0	n/a	n/a	LCD PCLK Source Select Bit 1	LCD PCLK Source Select Bit 0

bits 5-4 LCD PCLK Divide Select Bits [1:0]
These bits determine the divide used to generate the LCD pixel clock from the LCD pixel clock source.

Table 8-4: LCD PCLK Divide Selection

LCD PCLK Divide Select Bits	LCD PCLK Source to LCD PCLK Frequency Ratio
00	1:1
01	2:1
10	3:1
11	4:1

bits 1-0 LCD PCLK Source Select Bits [1:0]
These bits determine the source of the LCD pixel clock for the LCD display.

Table 8-5: LCD PCLK Source Selection

LCD PCLK Source Select Bits	LCD PCLK Source
00	CLKI
01	BUSCLK
10	CLKI2
11	MCLK (see note)

Note
MCLK may be a previously divided down version of CLKI, CLKI2 or BUSCLK.

CRT/TV Pixel Clock Configuration Register
REG[018h] RW

CRT/TV PCLK 2X Enable	n/a	CRT/TV PCLK Divide Select Bit 1	CRT/TV PCLK Divide Select Bit 0	n/a	n/a	CRT/TV PCLK Source Select Bit 1	CRT/TV PCLK Source Select Bit 0

bit 7 CRT/TV PCLK 2X Enable
This bit multiplies the CRT/TV pixel clock by 2.
This bit must be set to 1 when TV with flicker filter is enabled. See REG[1FCh] bits 2-0.

bits 5-4 CRT/TV PCLK Divide Select Bits[1:0]
These bits determine the divide used to generate the CRT/TV pixel clock from the CRT/TV pixel clock source.

Table 8-6: CRT/TV PCLK Divide Selection

CRT/TV PCLK Divide Select Bits	CRT/TV PCLK Source to CRT/TV PCLK Frequency Ratio
00	1:1
01	2:1
10	3:1
11	4:1

bits 1-0 CRT/TV PCLK Source Select Bits [1:0]
These bits determine the source of the CRT/TV pixel clock for the CRT/TV display.

Table 8-7: CRT/TV PCLK Source Selection

CRT/TV PCLK Source Select Bits	CRT/TV PCLK Source
00	CLKI
01	BUSCLK
10	CLKI2
11	MCLK (see note)

Note
MCLK may be a previously divided down version of CLKI, CLKI2 or BUSCLK.

MediaPlug Clock Configuration Register
REG[01Ch] RW

n/a	n/a	MediaPlug Clock Divide Select Bit 1	MediaPlug Clock Divide Select Bit 0	n/a	n/a	MediaPlug Clock Source Select Bit 1	MediaPlug Clock Source Select Bit 0

bits 5-4 MediaPlug Clock Divide Select Bits[1:0]
These bits determine the divide used to generate the MediaPlug Clock from the CRT/TV pixel clock source.

Table 8-8: MediaPlug Clock Divide Selection

MediaPlug Clock Divide Select Bits	MediaPlug Clock Source to CRT/TV Pixel Clock Frequency Ratio
00	1:1
01	2:1
10	3:1
11	4:1

bits 1-0 MediaPlug Clock Source Select Bits [1:0]
These bits determine the source of the MediaPlug Clock for the MediaPlug Interface. See Section 7.7, “MediaPlug Interface Timing” on page 115 for AC Timing.

Table 8-9: Video Clock Source Selection

MediaPlug Clock Source Select Bits	MediaPlug Clock Source
00	CLKI
01	BUSCLK
10	CLKI2
11	MCLK (see note)

Note
MCLK may be a previously divided down version of CLKI, CLKI2 or BUSCLK.

CPU To Memory Wait State Select Register
REG[01Eh] RW

n/a	n/a	n/a	n/a	n/a	n/a	CPU to Memory Wait State Select Bit 1	CPU to Memory Wait State Select Bit 0

bits 1-0 CPU to Memory Wait State Select Bits [1:0]
These bits are used to optimize the handshaking between the host interface and the memory controller. The bits should be set according to the relationship between BCLK and MCLK (memory clock).

Note
BCLK can be either BUSCLK or BUSCLK ÷ 2 depending on the setting of MD12 (see Table 5-6:, “Summary of Power-On/Reset Options,” on page 31).

Failure to meet the following conditions may lead to system failure which is recoverable only by RESET.

Table 8-10: Minimum Memory Timing Selection

Wait State Bits [1:0]	Condition
00	no restrictions
01	2 x period (MCLK) - 4ns > period(BCLK)
10	period(MCLK) - 4ns > period(BCLK)
11	Reserved

8.3.5 Memory Configuration Registers

Memory Configuration Register REG[020h]							RW
n/a	n/a	n/a	n/a	n/a	n/a	Memory Type Bit 1	Memory Type Bit 0

bits 1-0 Memory Type Bits [1:0]
These bits specify the memory type.

Table 8-11: Memory Type Selection

Memory Type Bits [1:0]	Memory Type
00	EDO-DRAM with 2-CAS#
01	FPM-DRAM with 2-CAS#
10	EDO-DRAM with 2-WE#
11	FPM-DRAM with 2-WE#

DRAM Refresh Rate Register REG[021h]							RW
Refresh Select Bit 1	Refresh Select Bit 0	n/a	n/a	n/a	DRAM Refresh Rate Bit 2	DRAM Refresh Rate Bit 1	DRAM Refresh Rate Bit 0

bits 7-6 Refresh Select Bits [1:0]
These bits specify the type of DRAM refresh used while in power save mode.

Table 8-12: Refresh Selection

Refresh Select Bits [1:0]	DRAM Refresh Type
00	CBR Refresh
01	Self-Refresh
1X	No Refresh

Note
These bits should not be changed while power save mode is enabled.

bits 2-0 DRAM Refresh Rate Select Bits [2:0]

These bits specify the divide used to generate the DRAM refresh clock rate, which is equal to $2^{(ValueOfTheseBits + 6)}$, from the MCLK source (either BUSCLK or CLKI as determined by REG[010h] bit 0).

Table 8-13: DRAM Refresh Rate Selection

DRAM Refresh Rate Bits [2:0]	MCLK Source Divide Amount	Refresh Rate for 40MHz MCLK Source	DRAM Refresh Time/256 cycles
000	64	625 kHz	0.4 ms
001	128	312 kHz	0.8 ms
010	256	156 kHz	1.6 ms
011	512	78 kHz	3.3 ms
100	1024	39 kHz	6.6 ms
101	2048	20 kHz	13.1 ms
110	4096	10 kHz	26.2 ms
111	8192	5 kHz	52.4 ms

DRAM Timing Control Register 0 REG[02Ah]							RW
DRAM Timing Control Register Bit 7	DRAM Timing Control Register Bit 6	DRAM Timing Control Register Bit 5	DRAM Timing Control Register Bit 4	DRAM Timing Control Register Bit 3	DRAM Timing Control Register Bit 2	DRAM Timing Control Register Bit 1	DRAM Timing Control Register Bit 0

DRAM Timing Control Register 1 REG[02Bh]							RW
n/a	n/a	n/a	n/a	n/a	n/a	DRAM Timing Control Register Bit 9	DRAM Timing Control Register Bit 8

REG[02Ah] bits 4-0 DRAM Timing Control Bits [9:0]
REG[02Bh] bits 1-0 The DRAM Timing Control registers must be set based on the type of DRAM, speed of DRAM, and MCLK frequency used. The following table provides the optimal values for each register.

Table 8-14: DRAM Timing Control Selection

DRAM Type	DRAM Speed (ns)	MCLK Frequency (MHz)	DRAM Timing Control Register 0	DRAM Timing Control Register 1
EDO	50	40	01h	01h
	50	33	12h	02h
	60		01h	01h
	50	30	12h	02h
	60		01h	01h
	70		00h	00h
	50	25	12h	02h
	60		12h	02h
	70		01h	01h
	80		00h	01h
	50	20	12h	02h
	60		12h	02h
	70		12h	02h
	80		01h	01h
FPM	50	25	12h	02h
	60		01h	01h
	50	20	12h	02h
	60		12h	02h
	70		11h	02h
	80		01h	01h

8.3.6 Panel Configuration Registers

Panel Type Register REG[030h]							RW
EL Panel Mode Enable	n/a	Panel Data Width Bit 1	Panel Data Width Bit 0	Panel Data Format Select	Color/Mono. Panel Select	Dual/Single Panel Select	TFT/ Passive LCD Panel Select

bit 7 EL Panel Mode Enable
When this bit = 1, the EL Panel support circuit is enabled.
When this bit = 0, there is no hardware effect.
This bit enables the S1D13506 built-in circuit for EL panels which require the Frame Rate Modulation (FRM) to remain static for one frame after every 262143 frames (approximately 1 hour at 60Hz refresh). When this bit is enabled, the need for external circuitry to perform the above function is eliminated.

bits 5-4 Panel Data Width Bits [1:0]
These bits select passive LCD/TFT/D-TFD panel data width size.

Table 8-15: Panel Data Width Selection

Panel Data Width Bits [1:0]	Passive LCD Panel Data Width Size	TFT/D-TFD Panel Data Width Size
00	4-bit	9-bit
01	8-bit	12-bit
10	16-bit	18-bit (64K color)
11	Reserved	Reserved

bit 3 Panel Data Format Select
When this bit = 1, 8-bit single color passive LCD panel data format 2 is selected. For AC timing see Section 7.5.5, “Single Color 8-Bit Panel Timing (Format 2)” on page 85.
When this bit = 0, 8-bit single color passive LCD panel data format 1 is selected. For AC timing see Section 7.5.4, “Single Color 8-Bit Panel Timing (Format 1)” on page 82.

bit 2 Color/Mono Panel Select
When this bit = 1, color LCD panel is selected.
When this bit = 0, monochrome LCD panel is selected.

bit 1 Dual/Single Panel Select
When this bit = 1, dual LCD panel is selected.
When this bit = 0, single LCD panel is selected.

bit 0 TFT/Passive LCD Panel Select
When this bit = 1, TFT/D-TFD panel is selected.
When this bit = 0, passive LCD panel is selected.

MOD Rate Register REG[031h]							RW
n/a	n/a	MOD Rate Bit 5	MOD Rate Bit 4	MOD Rate Bit 3	MOD Rate Bit 2	MOD Rate Bit 1	MOD Rate Bit 0

bits 5-0 MOD Rate Bits [5:0]
For a non-zero value these bits specify the number of FPLINE between toggles of the MOD output signal (DRDY).
When these bits are all 0's the MOD output signal toggles every FPFRAME. These bits are for passive LCD panels only.

LCD Horizontal Display Width Register REG[032h]							RW
n/a	LCD Horizontal Display Width Bit 6	LCD Horizontal Display Width Bit 5	LCD Horizontal Display Width Bit 4	LCD Horizontal Display Width Bit 3	LCD Horizontal Display Width Bit 2	LCD Horizontal Display Width Bit 1	LCD Horizontal Display Width Bit 0

bits 6-0 LCD Horizontal Display Width Bits [6:0]
These bits specify the LCD panel horizontal display width, in 8 pixel resolution.

Horizontal display width in number of pixels = ((ContentsOfThisRegister)+ 1) × 8

The Horizontal Display Width has certain limitations on the values that may be used for each type of LCD panel. Use of values that do not meet the limitations listed in the following table will result in undefined behavior.

Table 8-16: Horizontal Display Width (Pixels)

Panel Type	Horizontal Display Width (Pixels)
Passive Single	must be divisible by 16
Passive Dual	must be divisible by 32
TFT	must be divisible by 8

Note
This register must be programmed such that REG[032h] ≥ 3 (32 pixels).

LCD Horizontal Non-Display Period Register
REG[034h] RW

n/a	n/a	n/a	LCD Horizontal Non-Display Period Bit 4	LCD Horizontal Non-Display Period Bit 3	LCD Horizontal Non-Display Period Bit 2	LCD Horizontal Non-Display Period Bit 1	LCD Horizontal Non-Display Period Bit 0

bits 4-0 LCD Horizontal Non-Display Period Bits [4:0]
These bits specify the LCD panel horizontal non-display period width in 8 pixel resolution.

Horiz. non-display period width in number of pixels = ((ContentsOfThisRegister) + 1) × 8

Note
This register must be programmed such that REG[034h] ≥ 3 (32 pixels).

Note
For TFT/D-TFD only:
REG[034h] + 1 ≥ (REG[035h] + 1) + (REG[036h] bits 3-0 + 1)

TFT FPLINE Start Position Register
REG[035h] RW

n/a	n/a	n/a	TFT FPLINE Start Position Bit 4	TFT FPLINE Start Position Bit 3	TFT FPLINE Start Position Bit 2	TFT FPLINE Start Position Bit 1	TFT FPLINE Start Position Bit 0

bits 4-0 TFT FPLINE Start Position Bits [4:0]
For TFT/D-TFD panel only, these bits specify the delay, in 8 pixel resolution, from the start of the horizontal non-display period to the leading edge of the FPLINE pulse.

For 4/8 bpp color depth:
FPLINE start position in number of pixels = [(ContentsOfThisRegister) x 8 + 4]

For 15/16 bpp color depth:
FPLINE start position in number of pixels = [(ContentsOfThisRegister) x 8 + 6]

Note
For TFT/D-TFD only:
REG[034h] + 1 ≥ (REG[035h] + 1) + (REG[036h] bits 3-0 + 1)

TFT FPLINE Pulse Width Register							
REG[036h]							RW
LCD FPLINE Polarity Select	n/a	n/a	n/a	TFT FPLINE Pulse Width Bit 3	TFT FPLINE Pulse Width Bit 2	TFT FPLINE Pulse Width Bit 1	TFT FPLINE Pulse Width Bit 0

bit 7 LCD FPLINE Polarity Select
This bit selects the polarity of FPLINE for all LCD panels.
When this bit = 1, the FPLINE pulse is active high for TFT/D-TFD and active low for passive LCD.
When this bit = 0, the FPLINE pulse is active low for TFT/D-TFD and active high for passive LCD.

Table 8-17: LCD FPLINE Polarity Selection

LCD FPLINE Polarity Select	Passive LCD FPLINE Polarity	TFT FPLINE Polarity
0	active high	active low
1	active low	active high

bits 3-0 TFT FPLINE Pulse Width Bits [3:0]
For TFT/D-TFD panel only, these bits specify the pulse width of the FPLINE output signal in 8 pixel resolution.

FPLINE pulse width in number of pixels = ((ContentsOfThisRegister) + 1) × 8

The maximum FPLINE pulse width is 128 pixels.

Note
For TFT/D-TFD only:
REG[034h] + 1 ≥ (REG[035h] + 1) + (REG[036h] bits 3-0 + 1)

LCD Vertical Display Height Register 0							
REG[038h]							RW
LCD Vertical Display Height Bit 7	LCD Vertical Display Height Bit 6	LCD Vertical Display Height Bit 5	LCD Vertical Display Height Bit 4	LCD Vertical Display Height Bit 3	LCD Vertical Display Height Bit 2	LCD Vertical Display Height Bit 1	LCD Vertical Display Height Bit 0

LCD Vertical Display Height Register 1							
REG[039h]							RW
n/a	n/a	n/a	n/a	n/a	n/a	LCD Vertical Display Height Bit 9	LCD Vertical Display Height Bit 8

REG[038h] bits 7-0 LCD Vertical Display Height Bits [9:0]

REG[039h] bits 1-0 These bits specify the LCD panel vertical display height, in 1 line resolution.

Vertical display height in number of lines = (ContentsOfThisRegister) + 1

LCD Vertical Non-Display Period Register
REG[03Ah] RW

LCD Vertical Non-Display Period Status (RO)	n/a	LCD Vertical Non-Display Period Bit 5	LCD Vertical Non-Display Period Bit 4	LCD Vertical Non-Display Period Bit 3	LCD Vertical Non-Display Period Bit 2	LCD Vertical Non-Display Period Bit 1	LCD Vertical Non-Display Period Bit 0

bit 7 LCD Vertical Non-Display Period Status
This is a read-only status bit.
When a read from this bit = 1, a LCD panel vertical non-display period is occurring.
When a read from this bit = 0, the LCD panel output is in a vertical display period.

bits 5-0 LCD Vertical Non-Display Period Bits [5:0]
These bits specify the LCD panel vertical non-display period height in 1 line resolution.

Vertical non-display period height in number of lines = (ContentsOfThisRegister) + 1

Note
For TFT/D-TFD only:
(REG[03Ah] bits 5-0 + 1) ≥ (REG[03Bh] + 1) + (REG[03Ch] bits 2-0 + 1)

TFT FPFRAME Start Position Register
REG[03Bh] RW

n/a	n/a	TFT FPFRAME Start Position Bit 5	TFT FPFRAME Start Position Bit 4	TFT FPFRAME Start Position Bit 3	TFT FPFRAME Start Position Bit 2	TFT FPFRAME Start Position Bit 1	TFT FPFRAME Start Position Bit 0

bits 5-0 TFT FPFRAME Start Position Bits [5:0]
For TFT/D-TFD panel only, these bits specify the delay in lines from the start of the vertical non-display period to the leading edge of the FPFRAME pulse.

FPFRAME start position in number of lines = (ContentsOfThisRegister) + 1

Note
For TFT/D-TFD only:
(REG[03Ah] bits 5-0 + 1) ≥ (REG[03Bh] + 1) + (REG[03Ch] bits 2-0 + 1)

TFT FPFRAME Pulse Width Register REG[03Ch]							RW
LCD FPFRAME Polarity Select	n/a	n/a	n/a	n/a	TFT FPFRAME Pulse Width Bit 2	TFT FPFRAME Pulse Width Bit 1	TFT FPFRAME Pulse Width Bit 0

bit 7 LCD FPFRAME Polarity Select

This bit selects the polarity of FPFRAME for all LCD panels.

When this bit = 1, the FPFRAME pulse is active high for TFT/D-TFD and active low for passive LCD.

When this bit = 0, the FPFRAME pulse is active low for TFT/D-TFD and active high for passive LCD.

Table 8-18: LCD FPFRAME Polarity Selection

LCD FPFRAME Polarity Select	Passive LCD FPFRAME Polarity	TFT FPFRAME Polarity
0	active high	active low
1	active low	active high

bits 2-0 TFT FPFRAME Pulse Width Bits [2:0]

For TFT/D-TFD panel only, these bits specify the pulse width of the FPFRAME output signal in number of lines.

FPFRAME pulse width in number of lines = (ContentsOfThisRegister) + 1

Note

For TFT/D-TFD only:

(REG[03Ah] bits 5-0 + 1) ≥ (REG[03Bh] + 1) + (REG[03Ch] bits 2-0 + 1)

8.3.7 LCD Display Mode Registers

LCD Display Mode Register REG[040h]							RW
LCD Display Blank	n/a	n/a	SwivelView™ Enable Bit 1	n/a	LCD Bit-per-pixel Select Bit 2	LCD Bit-per-pixel Select Bit 1	LCD Bit-per-pixel Select Bit 0

bit 7 LCD Display Blank

When this bit = 1, the LCD display pipeline is disabled and all LCD data outputs are forced to zero (i.e., the screen is blanked).

When this bit = 0, the LCD display pipeline is enabled.

Note

If a dual panel is used, the Dual Panel Buffer (REG[041h] bit 0) must be disabled (set to 1) before blanking the LCD display.

bit 4 SwivelView™ Enable Bit 1

When this bit = 1, the LCD display image is rotated 180° clockwise. Please refer to Section 15, “SwivelView™” on page 194 for application and limitations.

When this bit = 0, there is no hardware effect.

This bit in conjunction with SwivelView™ Enable Bit 0 achieves the following hardware rotations.

Table 8-19: Setting SwivelView Modes

SwivelView Enable Bits	**SwivelView™ Modes**			
	Normal	**SwivelView 90°**	**SwivelView 180°**	**SwivelView 270°**
SwivelView Enable Bit 0 (REG[1FCh] bit 6)	0	1	0	1
SwivelView Enable Bit 1 (REG[040h] bit 4)	0	0	1	1

bits 2-0 LCD Bit-per-pixel Select Bits [2:0]

These bits select the color depth (bit-per-pixel) for the displayed data.

Note

15/16 bpp color depths bypass the LUT. Passive panels are supported up to 32K/64K colors (4096 colors if dithering disabled, see REG[041h] bit 1). TFT/D-TFD panels are supported up to 32K/64K colors.

Table 8-20: LCD Bit-per-pixel Selection

Bit-per-pixel Select Bits [1:0]	**Color Depth (bpp)**
000	Reserved
001	Reserved
010	4 bpp
011	8 bpp
100	15 bpp
101	16 bpp
110-111	Reserved

LCD Miscellaneous Register REG[041h]							RW
n/a	n/a	n/a	n/a	n/a	n/a	Dithering Disable	Dual Panel Buffer Disable

bit 1 Dithering Disable

When this bit = 1, dithering on the passive LCD panel for 15/16 bpp mode is disabled allowing a maximum of 4096 colors (2^{12}) or 16 gray shades.
When this bit = 0, dithering on the passive LCD panel for 15/16 bpp mode is enabled allowing a maximum of 64K colors (2^{16}) or 64 gray shades.

Note
This bit has no effect in 4/8 bpp modes where dithering is not supported.

All passive STN color panels are controlled using 3 bits for each pixel (RGB) for a total of 8 possible colors. LCD controllers use a combination of Frame Rate Modulation (FRM) and dithering to achieve more than 8 colors per pixel. FRM can achieve 16 shades of color for each RGB component resulting in a total of 4096 possible colors (16x16x16). Dithering uses a 4 pixel square formation and applies a set of 4 hard-coded patterns for each of the 16 shades of color. This expands the original 16 shades of color from the FRM logic to 64 shades per RGB component which results in 256K colors per pixel (64x64x64).

For the S1D13506, 16 bpp is arranged as 5-6-5 RGB. In this mode, when dithering is enabled, the LUT is bypassed and the original 16-bit data is used as a pointer into the 64 shades per color in the following manner.

(5-6-5 RGB) 32 possible Red, 64 possible Green, 32 possible Blue

This combination of FRM and dithering results in 256K colors/pixel, however, the 16 bpp limitation of the S1D13506 limits this to 64K colors/pixel.

bit 0 Dual Panel Buffer Disable

This bit is used to disable the Dual Panel Buffer.
When this bit = 1, the Dual Panel Buffer is disabled.
When this bit = 0, the Dual Panel Buffer is enabled.
When a single panel is selected, the Dual Panel Buffer is automatically disabled and this bit has no effect.

The Dual Panel Buffer is needed to fully support dual panels. Disabling the Dual Panel Buffer will improve performance, reduce power consumption, and allow higher resolution/ color display modes than would otherwise be possible; however, disabling the Dual Panel Buffer will reduce image contrast and overall display quality. This mode is not normally used except in special circumstances such as simultaneous display on a CRT/TV and dual panel LCD. For details on Frame Rate Calculation, see Section 17.

LCD Display Start Address Register 0 REG[042h]							RW
LCD Display Start Address Bit 7	LCD Display Start Address Bit 6	LCD Display Start Address Bit 5	LCD Display Start Address Bit 4	LCD Display Start Address Bit 3	LCD Display Start Address Bit 2	LCD Display Start Address Bit 1	LCD Display Start Address Bit 0

LCD Display Start Address Register 1 REG[043h]							RW
LCD Display Start Address Bit 15	LCD Display Start Address Bit 14	LCD Display Start Address Bit 13	LCD Display Start Address Bit 12	LCD Display Start Address Bit 11	LCD Display Start Address Bit 10	LCD Display Start Address Bit 9	LCD Display Start Address Bit 8

LCD Display Start Address Register 2 REG[044h]							RW
n/a	n/a	n/a	n/a	LCD Display Start Address Bit 19	LCD Display Start Address Bit 18	LCD Display Start Address Bit 17	LCD Display Start Address Bit 16

REG[042h] bits 7-0 LCD Display Start Address Bits [19:0]

REG[043h] bits 7-0 This register forms the 20-bit address for the starting word of the LCD image in the display buffer.

REG[044h] bits 3-0 **Note that this is a word address.** An entry of 00000h into these registers represents the first word of display memory, an entry of 00001h represents the second word of the display memory, and so on.

LCD Memory Address Offset Register 0 REG[046h]							RW
LCD Memory Address Offset Bit 7	LCD Memory Address Offset Bit 6	LCD Memory Address Offset Bit 5	LCD Memory Address Offset Bit 4	LCD Memory Address Offset Bit 3	LCD Memory Address Offset Bit 2	LCD Memory Address Offset Bit 1	LCD Memory Address Offset Bit 0

LCD Memory Address Offset Register 1 REG[047h]							RW
n/a	n/a	n/a	n/a	n/a	LCD Memory Address Offset Bit 10	LCD Memory Address Offset Bit 9	LCD Memory Address Offset Bit 8

REG[046h] bits 7-0 LCD Memory Address Offset Bits [10:0]

REG[047h] bits 2-0 These bits are the LCD display's 11-bit address offset from the starting word of line "n" to the starting word of line "n + 1".

A virtual image can be formed by setting this register to a value greater than the width of the display. The displayed image is a window into the larger virtual image.

LCD Pixel Panning Register REG[048h]							RW
n/a	n/a	n/a	n/a	Reserved	Reserved	LCD Pixel Panning Bit 1	LCD Pixel Panning Bit 0

bits 3-2 Reserved.
Must be set to 0.

bits 1-0 LCD Pixel Panning Bits [1:0]
This register is used to control the horizontal pixel panning of the LCD display. The display can be panned to the left by programming its respective Pixel Panning Bits to a non-zero value. This value represents the number of pixels panned. The maximum pan value is dependent on the display mode as shown in the table below.

Table 8-21: LCD Pixel Panning Selection

Color Depth (bpp)	Screen 2 Pixel Panning Bits Used
4 bpp	Bits [1:0]
8 bpp	Bit 0
15/16 bpp	---

Smooth horizontal panning can be achieved by a combination of this register and the LCD Display Start Address register.

LCD Display FIFO High Threshold Control Register REG[04Ah]							RW
n/a	n/a	LCD Display FIFO High Threshold Bit 5	LCD Display FIFO High Threshold Bit 4	LCD Display FIFO High Threshold Bit 3	LCD Display FIFO High Threshold Bit 2	LCD Display FIFO High Threshold Bit 1	LCD Display FIFO High Threshold Bit 0

bits 5-0 LCD Display FIFO High Threshold Bits [5:0]
These bits are used to optimize the display memory request arbitration. When this register is set to 00h, the threshold is automatically set in hardware. However, programming may be required if screen corruption is present (see Section 18.2, “Example Frame Rates” on page 209).

Note
This register does not need to be used in single display modes and may only be required in some display modes where two displays are active (see Section 16.2, “Bandwidth Limitation” on page 204).

LCD Display FIFO Low Threshold Control Register REG[04Bh]							RW
n/a	n/a	LCD Display FIFO Low Threshold Bit 5	LCD Display FIFO Low Threshold Bit 4	LCD Display FIFO Low Threshold Bit 3	LCD Display FIFO Low Threshold Bit 2	LCD Display FIFO Low Threshold Bit 1	LCD Display FIFO Low Threshold Bit 0

bits 5-0 LCD Display FIFO Low Threshold Bits [5:0]
When this register is set to 00h, the threshold is automatically set in hardware. If it becomes necessary to adjust REG[04Ah] from its default value, then the following formula must be maintained:

REG[04Bh] > REG[04Ah] and REG[04Bh] ≤ 3Ch

8.3.8 CRT/TV Configuration Registers

CRT/TV Horizontal Display Width Register REG[050h]							RW
n/a	CRT/TV Horizontal Display Width Bit 6	CRT/TV Horizontal Display Width Bit 5	CRT/TV Horizontal Display Width Bit 4	CRT/TV Horizontal Display Width Bit 3	CRT/TV Horizontal Display Width Bit 2	CRT/TV Horizontal Display Width Bit 1	CRT/TV Horizontal Display Width Bit 0

bits 6-0 CRT/TV Horizontal Display Width Bits [6:0]
These bits specify the CRT/TV horizontal display width, in 8 pixel resolution.

Horizontal display width in number of pixels = ((ContentsOfThisRegister)+ 1) × 8

CRT/TV Horizontal Non-Display Period Register REG[052h]							RW
n/a	n/a	CRT/TV Horizontal Non-Display Period Bit 5	CRT/TV Horizontal Non-Display Period Bit 4	CRT/TV Horizontal Non-Display Period Bit 3	CRT/TV Horizontal Non-Display Period Bit 2	CRT/TV Horizontal Non-Display Period Bit 1	CRT/TV Horizontal Non-Display Period Bit 0

bits 5-0 CRT/TV Horizontal Non-Display Period Bits [5:0]
These bits specify the CRT/TV horizontal non-display period width in 8 pixel resolution.

Horizontal non-display period width in number of pixels =
((ContentsOfThisRegister) + 1) × 8 for CRT mode
(ContentsOfThisRegister) × 8 + 6 for TV mode with NTSC output
(ContentsOfThisRegister) × 8 + 7 for TV mode with PAL output

Note
For CRT mode, the recommended minimum value which should be programmed into this register is 3 (32 pixels).

Note
REG[052h] + 1 ≥ (REG[053h] + 1) + (REG[054h] bits 3-0 + 1)

CRT/TV HRTC Start Position Register
REG[053h] RW

n/a	n/a	CRT/TV HRTC Start Position Bit 5	CRT/TV HRTC Start Position Bit 4	CRT/TV HRTC Start Position Bit 3	CRT/TV HRTC Start Position Bit 2	CRT/TV HRTC Start Position Bit 1	CRT/TV HRTC Start Position Bit 0

bits 5-0 CRT/TV HRTC Start Position Bits [5:0]
For CRT/TV, these bits specify the delay, in 8 pixel resolution, from the start of the horizontal non-display period to the leading edge of the HRTC pulse.

The following equations can be used to determine the HRTC start position in number of pixels for each display type:

HRTC start position in number of pixels=:
[(ContentsOfThisRegister) x 8 + 3] for CRT with 4/8 bpp color depth
[(ContentsOfThisRegister) x 8 + 5] for CRT in 15/16 bpp color depth
[((ContentsOfThisRegister) + 1) x 8 - 7] for TV-NTSC in 4/8 bpp color depth
[((ContentsOfThisRegister) + 1) x 8 - 5] for TV-NTSC in 15/16 bpp color depth
[((ContentsOfThisRegister) + 1) x 8 - 7] for TV-PAL in 4/8 bpp color depth
[((ContentsOfThisRegister) + 1) x 8 - 5] for TV-PAL in 15/16 bpp color depth

Note
REG[052h] + 1 ≥ (REG[053h] + 1) + (REG[054h] bits 3-0 + 1)

CRT HRTC Pulse Width Register
REG[054h] RW

CRT HRTC Polarity Select	n/a	n/a	n/a	CRT HRTC Pulse Width Bit 3	CRT HRTC Pulse Width Bit 2	CRT HRTC Pulse Width Bit 1	CRT HRTC Pulse Width Bit 0

bit 7 CRT HRTC Polarity Select
This bit selects the polarity of HRTC for CRTs.
When this bit = 1, the HRTC pulse is active high.
When this bit = 0, the HRTC pulse is active low.

Note
For NTSC/PAL modes, this bit must be set to 0b.

bits 3-0 CRT HRTC Pulse Width Bits [3:0]
These bits specify the pulse width of the CRT HRTC output signal in 8 pixel resolution.

HRTC pulse width in number of pixels = ((ContentsOfThisRegister) + 1) × 8

Note
For NTSC/PAL modes, these bits must be set to 0000b.

Note
REG[052h] + 1 ≥ (REG[053h] + 1) + (REG[054h] bits 3-0 + 1)

CRT/TV Vertical Display Height Register 0
REG[056h] RW

CRT/TV Vertical Display Height Bit 7	CRT/TV Vertical Display Height Bit 6	CRT/TV Vertical Display Height Bit 5	CRT/TV Vertical Display Height Bit 4	CRT/TV Vertical Display Height Bit 3	CRT/TV Vertical Display Height Bit 2	CRT/TV Vertical Display Height Bit 1	CRT/TV Vertical Display Height Bit 0

CRT/TV Vertical Display Height Register 1
REG[057h] RW

n/a	n/a	n/a	n/a	n/a	n/a	CRT/TV Vertical Display Height Bit 9	CRT/TV Vertical Display Height Bit 8

REG[056h] bits 7-0 CRT/TV Vertical Display Height Bits [9:0]

REG[057h] bits 1-0 These bits specify the CRT/TV vertical display height, in 1 line resolution.

Vertical display height in number of lines = (ContentsOfThisRegister) + 1

CRT/TV Vertical Non-Display Period Register
REG[058h] RW

CRT/TV Vertical Non-Display Period Status (RO)	CRT/TV Vertical Non-Display Period Bit 6	CRT/TV Vertical Non-Display Period Bit 5	CRT/TV Vertical Non-Display Period Bit 4	CRT/TV Vertical Non-Display Period Bit 3	CRT/TV Vertical Non-Display Period Bit 2	CRT/TV Vertical Non-Display Period Bit 1	CRT/TV Vertical Non-Display Period Bit 0

bit 7 CRT/TV Vertical Non-Display Period Status
This is a read-only status bit.
When a read from this bit = 1, a CRT/TV vertical non-display period is occurring.
When a read from this bit = 0, the CRT/TV output is in a vertical display period.

bits 6-0 CRT/TV Vertical Non-Display Period Bits [6:0]
These bits specify the CRT/TV vertical non-display period height in 1 line resolution.

Vertical non-display period height in number of lines = (ContentsOfThisRegister) + 1

Note
(REG[058h] bits 5-0 + 1) ≥ (REG[059h] + 1) + (REG[05Ah] bits 2-0 + 1)

CRT/TV VRTC Start Position Register REG[059h]							RW
n/a	CRT/TV VRTC Start Position Bit 6	CRT/TV VRTC Start Position Bit 5	CRT/TV VRTC Start Position Bit 4	CRT/TV VRTC Start Position Bit 3	CRT/TV VRTC Start Position Bit 2	CRT/TV VRTC Start Position Bit 1	CRT/TV VRTC Start Position Bit 0

bits 6-0 CRT/TV VRTC Start Position Bits [6:0]

For CRT/TV, these bits specify the delay in lines from the start of the vertical non-display period to the leading edge of the VRTC pulse.

VRTC start position in number of lines = (ContentsOfThisRegister) + 1

Note

(REG[058h] bits 5-0 + 1) ≥ (REG[059h] + 1) + (REG[05Ah] bits 2-0 + 1)

CRT/TV VRTC Pulse Width Register REG[05Ah]							RW
CRT VRTC Polarity Select	n/a	n/a	n/a	n/a	CRT VRTC Pulse Width Bit 2	CRT VRTC Pulse Width Bit 1	CRT VRTC Pulse Width Bit 0

bit 7 CRT VRTC Polarity Select

This bit selects the polarity of VRTC for CRT.
When this bit = 1, the VRTC pulse is active high.
When this bit = 0, the VRTC pulse is active low.

Note

For PAL/NTSC, this bit must be set to 0b.

bits 2-0 CRT VRTC Pulse Width Bits [2:0]

These bits specify the pulse width of the CRT VRTC output signal in number of lines.

VRTC pulse width in number of lines = (ContentsOfThisRegister) + 1

Note

For NTSC/PAL modes, these bits should be set to 000b.

Note

(REG[058h] bits 5-0 + 1) ≥ (REG[059h] + 1) + (REG[05Ah] bits 2-0 + 1)

CRT/TV Output Control Register REG[05Bh]							RW
n/a	n/a	TV Chrominance Filter Enable	TV Luminance Filter Enable	DAC Output Level Select	n/a	TV S-Video/ Composite Output Select	TV PAL/NTSC Output Select

bit 5 TV Chrominance Filter Enable
When this bit = 1, the TV chrominance filter is enabled.
When this bit = 0, there is no hardware effect.
The chrominance filter adjusts the color of the TV by limiting the bandwidth of the chrominance signal (reducing cross-luminance distortion). This reduces the “ragged edges” seen at boundaries between sharp color transitions. This filter is most useful for composite video output.

bit 4 TV Luminance Filter Enable
When this bit = 1, the TV luminance filter is enabled.
When this bit = 0, there is no hardware effect.
The luminance filter adjusts the brightness of the TV by limiting the bandwidth of the luminance signal (reducing cross-chrominance distortion). This reduces the “rainbow-like” colors at boundaries between sharp luminance transitions. This filter is most useful for composite video output.

bit 3 DAC Output Level Select
This bit should be set based on the conditions in the following table. When this bit is set to 1 it allows IREF to be reduced. For an example implementation of the required external CRT/TV circuitry, see Figure 5-2: “External Circuitry for CRT/TV Interface,” on page 36.

Table 8-22: DAC Output Level Selection

LCD	CRT	TV	REG[05Bh] bit 3	IREF (mA)
Supported	Not Supported	Not Supported	x	x
x	Supported	Not Supported	1	4.6
x	Supported	Supported	0	9.2

x = don’t care

bit 1 TV S-Video/Composite Output Select
When this bit = 1, S-Video TV signal output is selected.
When this bit = 0, Composite TV signal output is selected.

bit 0 TV PAL/NTSC Output Select
When this bit = 1, PAL format TV signal output is selected.
When this bit = 0, NTSC format TV signal output is selected.
This bit must be set to 0 when CRT mode is enabled.

8.3.9 CRT/TV Display Mode Registers

CRT/TV Display Mode Register REG[060h]							RW
CRT/TV Display Blank	n/a	n/a	n/a	n/a	CRT/TV Bit-per-pixel Select Bit 2	CRT/TV Bit-per-pixel Select Bit 1	CRT/TV Bit-per-pixel Select Bit 0

bit 7 CRT/TV Display Blank
When this bit = 1 the CRT/TV display pipeline is disabled and all CRT/TV data outputs are forced to zero (i.e., the screen is blanked).
When this bit = 0 the CRT/TV display pipeline is enabled.

bits 2-0 CRT/TV Bit-per-pixel Select Bits [2:0]
These bits select the bit-per-pixel for the displayed data.

Note
15/16 bpp color depths bypass the LUT.

Table 8-23: CRT/TV Bit-per-pixel Selection

Bit-per-pixel Select Bits [2:0]	Color Depth (bpp)
000	Reserved
001	Reserved
010	4 bpp
011	8 bpp
100	15 bpp
101	16 bpp
110-111	Reserved

CRT/TV Display Start Address Register 0
REG[062h] RW

CRT/TV Display Start Address Bit 7	CRT/TV Display Start Address Bit 6	CRT/TV Display Start Address Bit 5	CRT/TV Display Start Address Bit 4	CRT/TV Display Start Address Bit 3	CRT/TV Display Start Address Bit 2	CRT/TV Display Start Address Bit 1	CRT/TV Display Start Address Bit 0

CRT/TV Display Start Address Register 1
REG[063h] RW

CRT/TV Display Start Address Bit 15	CRT/TV Display Start Address Bit 14	CRT/TV Display Start Address Bit 13	CRT/TV Display Start Address Bit 12	CRT/TV Display Start Address Bit 11	CRT/TV Display Start Address Bit 10	CRT/TV Display Start Address Bit 9	CRT/TV Display Start Address Bit 8

CRT/TV Display Start Address Register 2
REG[064h] RW

n/a	n/a	n/a	n/a	CRT/TV Display Start Address Bit 19	CRT/TV Display Start Address Bit 18	CRT/TV Display Start Address Bit 17	CRT/TV Display Start Address Bit 16

REG[062h] bits 7-0 CRT/TV Start Address Bits [19:0]
REG[063h] bits 7-0 This register forms the 20-bit address for the starting word of the CRT/TV image in the display buffer. **Note that this is a word address.** An entry of 00000h into these registers
REG[064h] bits 3-0 represents the first word of display memory, an entry of 00001h represents the second word of the display memory, and so on.

CRT/TV Memory Address Offset Register 0
REG[066h] RW

CRT/TV Memory Address Offset Bit 7	CRT/TV Memory Address Offset Bit 6	CRT/TV Memory Address Offset Bit 5	CRT/TV Memory Address Offset Bit 4	CRT/TV Memory Address Offset Bit 3	CRT/TV Memory Address Offset Bit 2	CRT/TV Memory Address Offset Bit 1	CRT/TV Memory Address Offset Bit 0

CRT/TV Memory Address Offset Register 1
REG[067h] RW

n/a	n/a	n/a	n/a	n/a	CRT/TV Memory Address Offset Bit 10	CRT/TV Memory Address Offset Bit 9	CRT/TV Memory Address Offset Bit 8

REG[066h] bits 7-0 CRT/TV Memory Address Offset Bits [10:0]
REG[067h] bits 2-0 These bits are the CRT/TV display's 11-bit address offset from the starting word of line "n" to the starting word of line "n + 1". A virtual image can be formed by setting this register to a value greater than the width of the display. The displayed image is a window into the larger virtual image.

CRT/TV Pixel Panning Register REG[068h]							RW
n/a	n/a	n/a	n/a	Reserved	Reserved	CRT/TV Pixel Panning Bit 1	CRT/TV Pixel Panning Bit 0

bits 3-2 Reserved.
Must be set to 0.

bits 1-0 CRT/TV Pixel Panning Bits [1:0]
This register is used to control the horizontal pixel panning of the CRT/TV display. The display can be panned to the left by programming its respective Pixel Panning Bits to a non-zero value. This value represents the number of pixels panned. The maximum pan value is dependent on the display mode as shown in the table below.

Table 8-24: CRT/TV Pixel Panning Selection

Color Depth (bpp)	Screen 2 Pixel Panning Bits Used
4 bpp	Bits [1:0]
8 bpp	Bit 0
15/16 bpp	---

Smooth horizontal panning can be achieved by a combination of this register and the CRT/TV Display Start Address register.

CRT/TV Display FIFO High Threshold Control Register REG[06Ah]							RW
n/a	n/a	CRT/TV Display FIFO High Threshold Bit 5	CRT/TV Display FIFO High Threshold Bit 4	CRT/TV Display FIFO High Threshold Bit 3	CRT/TV Display FIFO High Threshold Bit 2	CRT/TV Display FIFO High Threshold Bit 1	CRT/TV Display FIFO High Threshold Bit 0

bits 5-0 CRT/TV Display FIFO High Threshold Bits [5:0]
These bits are used to optimize the display memory request arbitration. When this register is set to 00h, the threshold is automatically set in hardware. However, programming may be required if screen corruption is present (see Section 18.2, “Example Frame Rates” on page 209).

Note
This register does not need to be used in single display modes and may only be required in some display modes where two displays are active (see Section 16.2, “Bandwidth Limitation” on page 204).

CRT/TV Display FIFO Low Threshold Control Register REG[06Bh]							RW
n/a	n/a	CRT/TV Display FIFO Low Threshold Bit 5	CRT/TV Display FIFO Low Threshold Bit 4	CRT/TV Display FIFO Low Threshold Bit 3	CRT/TV Display FIFO Low Threshold Bit 2	CRT/TV Display FIFO Low Threshold Bit 1	CRT/TV Display FIFO Low Threshold Bit 0

bits 5-0 CRT/TV Display FIFO Low Threshold Bits [5:0]
When this register is set to 00h, the threshold is automatically set in hardware. If it becomes necessary to adjust REG[04Ah] from its default value, then the following formula must be maintained:

REG[04Bh] > REG[04Ah] and REG[04Bh] ≤ 3Ch

8.3.10 LCD Ink/Cursor Registers

LCD Ink/Cursor Control Register REG[070h]							RW
n/a	n/a	n/a	n/a	n/a	n/a	LCD Ink/Cursor Mode Bit 1	LCD Ink/Cursor Mode Bit 0

bits 1-0 LCD Ink/Cursor Control Bits [1:0]
These bits enable the LCD Ink/Cursor circuitry.

Table 8-25: LCD Ink/Cursor Selection

LCD Ink/Cursor Bits [1:0]	Mode
00	Inactive
01	Cursor
10	Ink
11	Reserved

Note
While in Ink mode, the Cursor X & Y Position registers must be set to 00h.

LCD Ink/Cursor Start Address Register REG[071h]							RW
LCD Ink/Cursor Start Address Bit 7	LCD Ink/Cursor Start Address Bit 6	LCD Ink/Cursor Start Address Bit 5	LCD Ink/Cursor Start Address Bit 4	LCD Ink/Cursor Start Address Bit 3	LCD Ink/Cursor Start Address Bit 2	LCD Ink/Cursor Start Address Bit 1	LCD Ink/Cursor Start Address Bit 0

bits 7-0 LCD Ink/Cursor Start Address Bits [7:0]
Encoded bits defining the start address for the LCD Ink/Cursor. For Cursor modes, a start address of 0 should be valid for most applications. For Ink or special Cursor modes, the start address should be set at an address location that does not conflict with the display memory of Dual Panel Buffer, which always takes the top M memory locations in bytes, where
M = (Panel Height x Panel Width / 16) x c, c = 1 for monochrome, 4 for color panel.

Table 8-26: LCD Ink/Cursor Start Address Encoding

LCD Ink/Cursor Start Address Bits [7:0]	Start Address
0	Memory Size - 1024
n = 255...1	Memory Size - n x 8192

Note
The effect of this register takes place at the next LCD vertical non-display period.

Note
See Section 10, “Display Buffer” on page 175 for display buffer organization.

LCD Cursor X Position Register 0 REG[072h]							RW
LCD Cursor X Position Bit 7	LCD Cursor X Position Bit 6	LCD Cursor X Position Bit 5	LCD Cursor X Position Bit 4	LCD Cursor X Position Bit 3	LCD Cursor X Position Bit 2	LCD Cursor X Position Bit 1	LCD Cursor X Position Bit 0

LCD Cursor X Position Register 1 REG[073h]							RW
LCD Cursor X Sign	n/a	n/a	n/a	n/a	n/a	LCD Cursor X Position Bit 9	LCD Cursor X Position Bit 8

REG[073h] bit 7 LCD Cursor X Sign
When this bit = 1, it defines the LCD Cursor X Position register to be a negative number. The negative number shall not exceed 63 decimal.
When this bit = 0, it defines the LCD Cursor X Position register to be a positive number.

REG[072h] bits 7-0 LCD Cursor X Position Bits [9:0]
REG[073h] bits 1-0 A 10-bit register that defines the horizontal position of the LCD Cursor’s top left hand corner in pixel units. This register is only valid when Cursor has been selected in the LCD Ink/Cursor select registers.

LCD Cursor Y Position Register 0
REG[074h] RW

LCD Cursor Y Position Bit 7	LCD Cursor Y Position Bit 6	LCD Cursor Y Position Bit 5	LCD Cursor Y Position Bit 4	LCD Cursor Y Position Bit 3	LCD Cursor Y Position Bit 2	LCD Cursor Y Position Bit 1	LCD Cursor Y Position Bit 0

LCD Cursor Y Position Register 1
REG[075h] RW

LCD Cursor Y Sign	n/a	n/a	n/a	n/a	n/a	LCD Cursor Y Position Bit 9	LCD Cursor Y Position Bit 8

REG[075h] bit 7 LCD Cursor Y Sign
When this bit = 1, it defines the LCD Cursor Y Position register to be a negative number. The negative number shall not exceed 63 decimal.
When this bit = 0, it defines the LCD Cursor Y Position register to be a positive number.

REG[074h] bits 7-0 LCD Cursor Y Position Bits [9:0]
REG[075h] bits 1-0 A 10-bit register that defines the vertical position of the LCD Cursor's top left hand corner in pixel units. This register is only valid when Cursor has been selected in the LCD Ink/Cursor select registers.

Note
The effect of REG[072h] through REG[074h] takes place only after REG[075h] is written and at the next LCD vertical non-display period.The effect of REG[075h] takes place at the next LCD vertical non-display period.

LCD Ink/Cursor Blue Color 0 Register
REG[076h] RW

n/a	n/a	n/a	LCD Ink/Cursor Blue Color 0 Bit 4	LCD Ink/Cursor Blue Color 0 Bit 3	LCD Ink/Cursor Blue Color 0 Bit 2	LCD Ink/Cursor Blue Color 0 Bit 1	LCD Ink/Cursor Blue Color 0 Bit 0

bits 4-0 LCD Ink/Cursor Blue Color 0 Bits[4:0]
These bits define the blue LCD Ink/Cursor color 0.

LCD Ink/Cursor Green Color 0 Register
REG[077h] RW

n/a	n/a	LCD Ink/Cursor Green Color 0 Bit 5	LCD Ink/Cursor Green Color 0 Bit 4	LCD Ink/Cursor Green Color 0 Bit 3	LCD Ink/Cursor Green Color 0 Bit 2	LCD Ink/Cursor Green Color 0 Bit 1	LCD Ink/Cursor Green Color 0 Bit 0

bits 5-0 LCD Ink/Cursor Green Color 0 Bits[5:0]
These bits define the green LCD ink/Cursor color 0.

LCD Ink/Cursor Red Color 0 Register
REG[078h] RW

n/a	n/a	n/a	LCD Ink/Cursor Red Color 0 Bit 4	LCD Ink/Cursor Red Color 0 Bit 3	LCD Ink/Cursor Red Color 0 Bit 2	LCD Ink/Cursor Red Color 0 Bit 1	LCD Ink/Cursor Red Color 0 Bit 0

bits 4-0 LCD Ink/Cursor Red Color 0 Bits[4:0]
These bits define the red LCD Ink/Cursor color 0.

LCD Ink/Cursor Blue Color 1 Register
REG[07Ah] RW

n/a	n/a	n/a	LCD Ink/Cursor Blue Color 1 Bit 4	LCD Ink/Cursor Blue Color 1 Bit 3	LCD Ink/Cursor Blue Color 1 Bit 2	LCD Ink/Cursor Blue Color 1 Bit 1	LCD Ink/Cursor Blue Color 1 Bit 0

bits 4-0 LCD Ink/Cursor Blue Color 1 Bits[4:0]
These bits define the blue LCD Ink/Cursor color 1.

LCD Ink/Cursor Green Color 1 Register
REG[07Bh] RW

n/a	n/a	LCD Ink/Cursor Green Color 1 Bit 5	LCD Ink/Cursor Green Color 1 Bit 4	LCD Ink/Cursor Green Color 1 Bit 3	LCD Ink/Cursor Green Color 1 Bit 2	LCD Ink/Cursor Green Color 1 Bit 1	LCD Ink/Cursor Green Color 1 Bit 0

bits 5-0 LCD Ink/Cursor Green Color 1 Bits[5:0]
These bits define the green LCD Ink/Cursor color 1.

LCD Ink/Cursor Red Color 1 Register
REG[07Ch] RW

n/a	n/a	n/a	LCD Ink/Cursor Red Color 1 Bit 4	LCD Ink/Cursor Red Color 1 Bit 3	LCD Ink/Cursor Red Color 1 Bit 2	LCD Ink/Cursor Red Color 1 Bit 1	LCD Ink/Cursor Red Color 1 Bit 0

bits 4-0 LCD Ink/Cursor Red Color 1 Bits[4:0]
These bits define the red LCD Ink/Cursor color 1.

LCD Ink/Cursor FIFO High Threshold Register REG[07Eh]							RW
n/a	n/a	n/a	n/a	LCD Ink/Cursor FIFO High Threshold Bit 3	LCD Ink/Cursor FIFO High Threshold Bit 2	LCD Ink/Cursor FIFO High Threshold Bit 1	LCD Ink/Cursor FIFO High Threshold Bit 0

bits 5-0 LCD Ink/Cursor FIFO High Threshold Bits [3:0]
These bits are used to optimize the display memory request arbitration for the Hardware Cursor/Ink Layer. When this register is set to 00h, the threshold is automatically set in hardware.

8.3.11 CRT/TV Ink/Cursor Registers

CRT/TV Ink/Cursor Control Register REG[080h]							RW
n/a	n/a	n/a	n/a	n/a	n/a	CRT/TV Ink/Cursor Mode Bit 1	CRT/TV Ink/Cursor Mode Bit 0

bits 1-0 CRT/TV Ink/Cursor Control Bits [1:0]
These bits enable the CRT/TV Ink/Cursor circuitry.

Table 8-27: CRT/TV Ink/Cursor Selection

CRT/TV Ink/Cursor Bits [1:0]	Mode
00	Inactive
01	Cursor
10	Ink
11	Reserved

Note
During Ink mode, the Cursor X & Y Position registers must be programmed to zero.

CRT/TV Ink/Cursor Start Address Register							
REG[081h]							RW
CRT/TV Ink/Cursor Start Address Bit 7	CRT/TV Ink/Cursor Start Address Bit 6	CRT/TV Ink/Cursor Start Address Bit 5	CRT/TV Ink/Cursor Start Address Bit 4	CRT/TV Ink/Cursor Start Address Bit 3	CRT/TV Ink/Cursor Start Address Bit 2	CRT/TV Ink/Cursor Start Address Bit 1	CRT/TV Ink/Cursor Start Address Bit 0

bits 7-0 CRT/TV Ink/Cursor Start Address Bits [7:0]

Encoded bits defining the start address for the CRT/TV Ink/Cursor. For Cursor modes, a start address of 0 should be valid for most applications. For Ink or special Cursor modes, the start address should be set at an address location that does not conflict with the display memory of Dual Panel Buffer, which always takes the top M memory locations in bytes, where

M = (Panel Height x Panel Width / 16) x c, c = 1 for monochrome, 4 for color panel.

Table 8-28: CRT/TV Ink/Cursor Start Address Encoding

CRT/TV Ink/Cursor Start Address Bits [7:0]	Start Address
0	Memory Size - 1024
n = 255...1	Memory Size - n x 8192

Note

The effect of this register takes place at the next CRT/TV vertical non-display period.

Note

See Section 10, “Display Buffer” on page 175 for display buffer organization.

CRT/TV Cursor X Position Register 0							
REG[082h]							RW
CRT/TV Cursor X Position Bit 7	CRT/TV Cursor X Position Bit 6	CRT/TV Cursor X Position Bit 5	CRT/TV Cursor X Position Bit 4	CRT/TV Cursor X Position Bit 3	CRT/TV Cursor X Position Bit 2	CRT/TV Cursor X Position Bit 1	CRT/TV Cursor X Position Bit 0

CRT/TV Cursor X Position Register 1							
REG[083h]							RW
CRT/TV Cursor X Sign	n/a	n/a	n/a	n/a	n/a	CRT/TV Cursor X Position Bit 9	CRT/TV Cursor X Position Bit 8

REG[083h] bit 7 CRT/TV Cursor X Sign

When this bit = 1, it defines the CRT/TV Cursor X Position register to be a negative number. The negative number shall not exceed 63 decimal.

When this bit = 0, it defines the CRT/TV Cursor X Position register to be a positive number.

REG[082h] bits 7-0 CRT/TV Cursor X Position Bits [9:0]

REG[083h] bits 1-0 A 10-bit register that defines the horizontal position of the CRT/TV Cursor’s top left hand corner in pixel units. This register is only valid when Cursor has been selected in the CRT/TV Ink/Cursor select registers.

CRT/TV Cursor Y Position Register 0
REG[084h] RW

CRT/TV Cursor Y Position Bit 7	CRT/TV Cursor Y Position Bit 6	CRT/TV Cursor Y Position Bit 5	CRT/TV Cursor Y Position Bit 4	CRT/TV Cursor Y Position Bit 3	CRT/TV Cursor Y Position Bit 2	CRT/TV Cursor Y Position Bit 1	CRT/TV Cursor Y Position Bit 0

CRT/TV Cursor Y Position Register 1
REG[085h] RW

CRT/TV Cursor Y Sign	n/a	n/a	n/a	n/a	n/a	CRT/TV Cursor Y Position Bit 9	CRT/TV Cursor Y Position Bit 8

REG[084h] bit 7 CRT/TV Cursor YSign
When this bit = 1, it defines the CRT/TV Cursor Y Position register as a negative number. The negative number shall not exceed 63 decimal.
When this bit = 0, it defines the CRT/TV Cursor Y Position register as a positive number.

REG[084h] bits 7-0 CRT/TV Cursor Y Position Bits [9:0]
REG[085h] bits 1-0 A 10-bit register that defines the vertical position of the CRT/TV Cursor's top left hand corner in pixel units. This register is only valid when Cursor has been selected in the CRT/TV Ink/Cursor select registers.

Note
The effect of REG[082h] through REG[084h] takes place only after REG[085h]is written to and at the next CRT/TV vertical non-display period.The effect of REG[085h] takes place at the next CRT/TV vertical non-display period.

CRT/TV Ink/Cursor Blue Color 0 Register
REG[086h] RW

n/a	n/a	n/a	CRT/TV Ink/Cursor Blue Color 0 Bit 4	CRT/TV Ink/Cursor Blue Color 0 Bit 3	CRT/TV Ink/Cursor Blue Color 0 Bit 2	CRT/TV Ink/Cursor Blue Color 0 Bit 1	CRT/TV Ink/Cursor Blue Color 0 Bit 0

bits 4-0 CRT/TV Ink/Cursor Blue Color 0 Bits[4:0]
These bits define the blue CRT/TV Ink/Cursor color 0.

CRT/TV Ink/Cursor Green Color 0 Register
REG[087h] RW

n/a	n/a	CRT/TV Ink/Cursor Green Color 0 Bit 5	CRT/TV Ink/Cursor Green Color 0 Bit 4	CRT/TV Ink/Cursor Green Color 0 Bit 3	CRT/TV Ink/Cursor Green Color 0 Bit 2	CRT/TV Ink/Cursor Green Color 0 Bit 1	CRT/TV Ink/Cursor Green Color 0 Bit 0

bits 5-0 CRT/TV Ink/Cursor Green Color 0 Bits[5:0]
These bits define the green CRT/TV Ink/Cursor color 0.

CRT/TV Ink/Cursor Red Color 0 Register
REG[088h] RW

n/a	n/a	n/a	CRT/TV Ink/Cursor Red Color 0 Bit 4	CRT/TV Ink/Cursor Red Color 0 Bit 3	CRT/TV Ink/Cursor Red Color 0 Bit 2	CRT/TV Ink/Cursor Red Color 0 Bit 1	CRT/TV Ink/Cursor Red Color 0 Bit 0

bits 4-0 CRT/TV Ink/Cursor Red Color 0 Bits[4:0]
These bits define the red CRT/TV Ink/Cursor color 0.

CRT/TV Ink/Cursor Blue Color 1 Register
REG[08Ah] RW

n/a	n/a	n/a	CRT/TV Ink/Cursor Blue Color 1 Bit 4	CRT/TV Ink/Cursor Blue Color 1 Bit 3	CRT/TV Ink/Cursor Blue Color 1 Bit 2	CRT/TV Ink/Cursor Blue Color 1 Bit 1	CRT/TV Ink/Cursor Blue Color 1 Bit 0

bits 4-0 CRT/TV Ink/Cursor Blue Color 1 Bits[4:0]
These bits define the blue CRT/TV Ink/Cursor color 1.

CRT/TV Ink/Cursor Green Color 1 Register
REG[08Bh] RW

n/a	n/a	CRT/TV Ink/Cursor Green Color 1 Bit 5	CRT/TV Ink/Cursor Green Color 1 Bit 4	CRT/TV Ink/Cursor Green Color 1 Bit 3	CRT/TV Ink/Cursor Green Color 1 Bit 2	CRT/TV Ink/Cursor Green Color 1 Bit 1	CRT/TV Ink/Cursor Green Color 1 Bit 0

bits 5-0 CRT/TV Ink/Cursor Green Color 1 Bits[5:0]
These bits define the green CRT/TV Ink/Cursor color 1.

CRT/TV Ink/Cursor Red Color 1 Register
REG[08Ch] RW

n/a	n/a	n/a	CRT/TV Ink/Cursor Red Color 1 Bit 4	CRT/TV Ink/Cursor Red Color 1 Bit 3	CRT/TV Ink/Cursor Red Color 1 Bit 2	CRT/TV Ink/Cursor Red Color 1 Bit 1	CRT/TV Ink/Cursor Red Color 1 Bit 0

bits 4-0 CRT/TV Ink/Cursor Red Color 1 Bits[4:0]
These bits define the red CRT/TV Ink/Cursor color 1.

CRT/TV Ink/Cursor FIFO High Threshold Register REG[08Eh]							RW
n/a	n/a	n/a	n/a	CRT/TV Ink/Cursor FIFO High Threshold Bit 3	CRT/TV Ink/Cursor FIFO High Threshold Bit 2	CRT/TV Ink/Cursor FIFO High Threshold Bit 1	CRT/TV Ink/Cursor FIFO High Threshold Bit 0

bits 5-0 CRT/TV Ink/Cursor FIFO High Threshold Bits [5:0]
These bits are used to optimize the display memory request arbitration for the Hardware Cursor/Ink Layer. When this register is set to 00h, the threshold is automatically set in hardware.

8.3.12 BitBLT Configuration Registers

BitBLT Control Register 0 REG[100h]							RW
BitBLT Active Status	BitBLT FIFO Not Empty Status (RO)	BitBLT FIFO Half Full Status (RO)	BitBLT FIFO Full Status (RO)	n/a	n/a	BitBLT Destination Linear Select	BitBLT Source Linear Select

bits 7 BitBLT Active Status
This register bit has two data paths, one for write, the other for read.

Write Data Path
When software writes a one to this bit, it will initiate the 2D operation.

Read Data Path
The read back of this register indicates the status of the 2D engine.
When a read from this bit = 1, the 2D engine is busy.
When a read from this bit = 0, the 2D engine is idle and is ready for the next operation.

Table 8-29: BitBLT Active Status

BitBLT Active Status		**State**
Write	**Read**	
0	0	Idle
0	1	Reserved
1	0	Initiating operation
1	1	Operation in progress

bit 6 BitBLT FIFO Not-Empty Status
This is a read-only status bit.
When this bit = 1, the BitBLT FiFO has at least one data.
When this bit = 0, the BitBLT FIFO is empty.
To reduce system memory read latency, software can monitor this bit prior to a BitBLT read burst operation.

The following table shows the number of data available in BitBLT FIFO under different status conditions.

Table 8-30: BitBLT FIFO Data Available

BitBLT FIFO Full Status (REG[100h] Bit 4)	BitBLT FIFO Half Full Status (REG[100h] Bit 5)	BitBLT FIFO Not Empty Status (REG[100h] Bit 6)	Number of Data available in BitBLT FIFO
0	0	0	0
0	0	1	1 to 6
0	1	1	7 to 14
1	1	1	15 to 16

bit 5 BitBLT FIFO Half Full Status
This is a read-only status bit.
Software can use this bit to optimize BitBLT write burst operations.
When this bit = 1, the BitBLT FIFO is half full or greater than half full.
When this bit = 0, the BitBLT FIFO is less than half full.

bit 4 BitBLT FIFO Full Status
This is a read-only status bit.
Software can use this bit to optimize BitBLT write burst operations.
When this bit = 1, the BitBLT FIFO is full.
When this bit = 0, the BitBLT FIFO is not full.

bit 1 BitBLT Destination Linear Select
When this bit = 1, the Destination BitBLT is stored as a contiguous linear block of memory.
When this bit = 0, the Destination BitBLT is stored as a rectangular region of memory.
The BitBLT Memory Address Offset (REG[10Ch], REG[10Dh]) determines the address offset from the start of one line to the next line.

bit 0 BitBLT Source Linear Select
When this bit = 1, the Source BitBLT is stored as a contiguous linear block of memory.
When this bit = 0, the Source BitBLT is stored as a rectangular region of memory.
The BitBLT Memory Address Offset (REG[10Ch], REG[10Dh]) determines the address offset from the start of one line to the next line.

BitBLT Control Register 1 REG[101h]							RW
n/a	n/a	n/a	Reserved	n/a	n/a	n/a	BitBLT Color Format Select

bit 4 Reserved.
Must be set to 0.

bit 0 BitBLT Color Format Select
This bit selects the color format that the 2D operation is applied to.
When this bit = 0, 8 bpp (256 color) format is selected.
When this bit = 1, 16 bpp (64K color) format is selected.

BitBLT ROP Code/Color Expansion Register REG[102h]							RW
n/a	n/a	n/a	n/a	BitBLT ROP Code Bit 3	BitBLT ROP Code Bit 2	BitBLT ROP Code Bit 1	BitBLT ROP Code Bit 0

bits 3-0 BitBLT Raster Operation Code/Color Expansion Bits [3:0]
ROP Code for Write BitBLT and Move BitBLT. Bits 2-0 also specify the start bit position for Color Expansion.

Table 8-31: BitBLT ROP Code/Color Expansion Function Selection

BitBLT ROP Code Bits [3:0]	Boolean Function for Write BitBLT and Move BitBLT	Boolean Function for Pattern Fill	Start Bit Position for Color Expansion
0000	0 (Blackness)	0 (Blackness)	bit 0
0001	~S . ~D or ~(S + D)	~P . ~D or ~(P + D)	bit 1
0010	~S . D	~P . D	bit 2
0011	~S	~P	bit 3
0100	S . ~D	P . ~D	bit 4
0101	~D	~D	bit 5
0110	S ^ D	P ^ D	bit 6
0111	~S + ~D or ~(S . D)	~P + ~D or ~(P . D)	bit 7
1000	S . D	P . D	bit 0
1001	~(S ^ D)	~(P ^ D)	bit 1
1010	D	D	bit 2
1011	~S + D	~P + D	bit 3
1100	S	P	bit 4
1101	S + ~D	P + ~D	bit 5
1110	S + D	P + D	bit 6
1111	1 (Whiteness)	1 (Whiteness)	bit 7

Note
S = Source, D = Destination, P = Pattern.

BitBLT Operation Register REG[103h]							RW
n/a	n/a	n/a	n/a	BitBLT Operation Bit 3	BitBLT Operation Bit 2	BitBLT Operation Bit 1	BitBLT Operation Bit 0

bits 3-0 BitBLT Operation Bits [3:0]

Specifies the 2D Operation to be carried out based on the following table:

Table 8-32: BitBLT Operation Selection

BitBLT Operation Bits [3:0]	BitBLT Operation
0000	Write BitBLT with ROP.
0001	Read BitBLT.
0010	Move BitBLT in positive direction with ROP.
0011	Move BitBLT in negative direction with ROP.
0100	Transparent Write BitBLT.
0101	Transparent Move BitBLT in positive direction.
0110	Pattern Fill with ROP.
0111	Pattern Fill with transparency.
1000	Color Expansion.
1001	Color Expansion with transparency.
1010	Move BitBLT with Color Expansion.
1011	Move BitBLT with Color Expansion and transparency.
1100	Solid Fill.
Other combinations	Reserved

Note

The BitBLT operations Pattern Fill with ROP and Pattern Fill with transparency require a BitBLT width ≥ 2. The BitBLT width is set in REG[110h], REG[111h].

BitBLT Source Start Address Register 0 REG[104h]							RW
BitBLT Source Start Address Bit 7	BitBLT Source Start Address Bit 6	BitBLT Source Start Address Bit 5	BitBLT Source Start Address Bit 4	BitBLT Source Start Address Bit 3	BitBLT Source Start Address Bit 2	BitBLT Source Start Address Bit 1	BitBLT Source Start Address Bit 0

BitBLT Source Start Address Register 1 REG[105h]							RW
BitBLT Source Start Address Bit 15	BitBLT Source Start Address Bit 14	BitBLT Source Start Address Bit 13	BitBLT Source Start Address Bit 12	BitBLT Source Start Address Bit 11	BitBLT Source Start Address Bit 10	BitBLT Source Start Address Bit 9	BitBLT Source Start Address Bit 8

BitBLT Source Start Address Register 2 REG[106h]							RW
n/a	n/a	n/a	BitBLT Source Start Address Bit 20	BitBLT Source Start Address Bit 19	BitBLT Source Start Bit 18	BitBLT Source Start Address Bit 17	BitBLT Source Start Address Bit 16

REG[104h] bits 7-0 BitBLT Source Start Address Bits [20:0]
REG[105h] bits 7-0 A 21-bit register that specifies the source start address for the BitBLT operation.
REG[106h] bits 4-0 If data is sourced from the CPU, then bit 0 is used for byte alignment within a 16-bit word and the other address bits are ignored. In pattern fill operation, the BitBLT Source Start Address is defined by the following equation:
Value programmed to the Source Start Address Register =
Pattern Base Address + Pattern Line Offset + Pixel Offset.

The following table shows how Source Start Address Register is defined for 8 and 16 bpp color depths.

Table 8-33: BitBLT Source Start Address Selection

Color Format	Pattern Base Address[20:0]	Pattern Line Offset[2:0]	Pixel Offset[3:0]
8 bpp	BitBLT Source Start Address[20:6], 6'b0	BitBLT Source Start Address[5:3]	1'b0, BitBLT Source Start Address[2:0]
16 bpp	BitBLT Source Start Address[20:7], 7'b0	BitBLT Source Start Address[6:4]	BitBLT Source Start Address[3:0]

BitBLT Destination Start Address Register 0							
REG[108h]							RW
BitBLT Destination Start Address Bit 7	BitBLT Destination Start Address Bit 6	BitBLT Destination Start Address Bit 5	BitBLT Destination Start Address Bit 4	BitBLT Destination Start Address Bit 3	BitBLT Destination Start Address Bit 2	BitBLT Destination Start Address Bit 1	BitBLT Destination Start Address Bit 0

BitBLT Destination Start Address Register 1							
REG[109h]							RW
BitBLT Destination Start Address Bit 15	BitBLT Destination Start Address Bit 14	BitBLT Destination Start Address Bit 13	BitBLT Destination Start Address Bit 12	BitBLT Destination Start Address Bit 11	BitBLT Destination Start Address Bit 10	BitBLT Destination Start Address Bit 9	BitBLT Destination Start Address Bit 8

BitBLT Destination Start Address Register 2							
REG[10Ah]							RW
n/a	n/a	n/a	BitBLT Destination Start Address Bit 20	BitBLT Destination Start Address Bit 19	BitBLT Destination Start Address Bit 18	BitBLT Destination Start Address Bit 17	BitBLT Destination Start Address Bit 16

REG[108h] bits 7-0 BitBLT Destination Start Address Bits [20:0]
REG[109h] bits 7-0 A 21-bit register that specifies the destination start address for the BitBLT operation.
REG[10Ah] bits 4-0

BitBLT Memory Address Offset Register 0							
REG[10Ch]							RW
BitBLT Memory Address Offset Bit 7	BitBLT Memory Address Offset Bit 6	BitBLT Memory Address Offset Bit 5	BitBLT Memory Address Offset Bit 4	BitBLT Memory Address Offset Bit 3	BitBLT Memory Address Offset Bit 2	BitBLT Memory Address Offset Bit 1	BitBLT Memory Address Offset Bit 0

BitBLT Memory Address Offset Register 1							
REG[10Dh]							RW
n/a	n/a	n/a	n/a	n/a	BitBLT Memory Address Offset Bit 10	BitBLT Memory Address Offset Bit 9	BitBLT Memory Address Offset Bit 8

REG[10Ch] bits 7-0 BitBLT Memory Address Offset Bits [10:0]
REG[10Dh] bits 2-0 These bits are the display's 11-bit address offset from the starting word of line "n" to the starting word of line "n + 1". They are used only for address calculation when the BitBLT is configured as a rectangular region of memory. They are not used for the displays.

BitBLT Width Register 0
REG[110h] RW

BitBLT Width Bit 7	BitBLT Width Bit 6	BitBLT Width Bit 5	BitBLT Width Bit 4	BitBLT Width Bit 3	BitBLT Width Bit 2	BitBLT Width Bit 1	BitBLT Width Bit 0

BitBLT Width Register 1
REG[111h] RW

n/a	n/a	n/a	n/a	n/a	n/a	BitBLT Width Bit 9	BitBLT Width Bit 8

REG[110h] bits 7-0 BitBLT Width Bits [9:0]
REG[111h] bits 1-0 A 10-bit register that specifies the BitBLT width in pixels -1.

Note
The BitBLT operations Pattern Fill with ROP and Pattern Fill with transparency require a BitBLT width ≥ 2.

BitBLT Height Register 0
REG[112h] RW

BitBLT Height Bit 7	BitBLT Height Bit 6	BitBLT Height Bit 5	BitBLT Height Bit 4	BitBLT Height Bit 3	BitBLT Height Bit 2	BitBLT Height Bit 1	BitBLT Height Bit 0

BitBLT Height Register 1
REG[113h] RW

n/a	n/a	n/a	n/a	n/a	n/a	BitBLT Height Bit 9	BitBLT Height Bit 8

REG[112h] bits 7-0 BitBLT Height Bits [9:0]
REG[113h] bits 1-0 A 10-bit register that specifies the BitBLT height in lines -1.

BitBLT Background Color Register 0
REG[114h] RW

BitBLT Background Color Bit 7	BitBLT Background Color Bit 6	BitBLT Background Color Bit 5	BitBLT Background Color Bit 4	BitBLT Background Color Bit 3	BitBLT Background Color Bit 2	BitBLT Background Color Bit 1	BitBLT Background Color Bit 0

BitBLT Background Color Register 1
REG[115h] RW

BitBLT Background Color Bit 15	BitBLT Background Color Bit 14	BitBLT Background Color Bit 13	BitBLT Background Color Bit 12	BitBLT Background Color Bit 11	BitBLT Background Color Bit 10	BitBLT Background Color Bit 9	BitBLT Background Color Bit 8

REG[114h] bits 7-0 BitBLT Background Color Bits [15:0]
REG[115h] bits 15-8 A 16-bit register that specifies the BitBLT background color for Color Expansion or key color for Transparent BitBLT. For 16 bpp mode (REG[101h] bit 0 = 1), all 16 bits are used.

For 8 bpp mode (REG[101h] bit 0 = 0), only bits 7-0 are used.

BitBLT Foreground Color Register 0
REG[118h] RW

BitBLT Foreground Color Bit 7	BitBLT Foreground Color Bit 6	BitBLT Foreground Color Bit 5	BitBLT Foreground Color Bit 4	BitBLT Foreground Color Bit 3	BitBLT Foreground Color Bit 2	BitBLT Foreground Color Bit 1	BitBLT Foreground Color Bit 0

BitBLT Foreground Color Register 1
REG[119h] RW

BitBLT Foreground Color Bit 15	BitBLT Foreground Color Bit 14	BitBLT Foreground Color Bit 13	BitBLT Foreground Color Bit 12	BitBLT Foreground Color Bit 11	BitBLT Foreground Color Bit 10	BitBLT Foreground Color Bit 9	BitBLT Foreground Color Bit 8

REG[118h] bits 7-0 BitBLT Foreground Color Bits [15:0]
REG[119h] bits 7-0 A 16-bit register that specifies the BitBLT foreground color for Color Expansion or Solid Fill. For 16 bpp mode (REG[101h] bit 0 = 1), all 16 bits are used. For 8 bpp mode (REG[101h] bit 0 = 0), only bits 7-0 are used.

8.3.13 Look-Up Table Registers

Note
Accessing the LCD Look-Up Table (LUT) requires an active LCD PCLK and accessing the CRT/TV LUT requires an active CRT/TV PCLK. Additionally, access to the LUT registers is not permitted during power save mode. For further information on the clocks, see Section 20, “Clocks” on page 217.

Look-Up Table Mode Register REG[1E0h]							RW
n/a	n/a	n/a	n/a	n/a	n/a	LUT Mode Bit 1	LUT Mode Bit 0

bits 1-0 Look-Up Table Mode Bits [1:0]
These bits determine which of the Look-Up Tables (LCD and CRT/TV) are accessible by REG[1E2h] and REG[1E4h].

Table 8-34: LUT Mode Selection

LUT Mode Bits [1:0]	Read	Write
00	LCD LUT	LCD and CRT/TV LUT’s
01	LCD LUT	LCD LUT
10	CRT/TV LUT	CRT/TV LUT
11	Reserved	Reserved

Look-Up Table Address Register REG[1E2h]							RW
LUT Address Bit 7	LUT Address Bit 6	LUT Address Bit 5	LUT Address Bit 4	LUT Address Bit 3	LUT Address Bit 2	LUT Address Bit 1	LUT Address Bit 0

bits 7-0 LUT Address Bits [7:0]
These 8 bits control a pointer into the Look-Up Tables (LUT). The S1D13506 has three 256-position, 4-bit wide LUTs, one for each of red, green, and blue – refer to Section 12, “Look-Up Table Architecture” on page 179 for details.

This register selects which LUT entry is read/write accessible through the LUT Data Register (REG[1E4h]). Writing the LUT Address Register automatically sets the pointer to the Red LUT. Accesses to the LUT Data Register automatically increment the pointer.

For example, writing a value 03h into the LUT Address Register sets the pointer to R[3]. A subsequent access to the LUT Data Register accesses R[3] and moves the pointer onto G[3]. Subsequent accesses to the LUT Data Register move the pointer onto B[3], R[4], G[4], B[4], R[5], etc.

Note
The RGB data is inserted into the LUT after the Blue data is written, i.e. all three colors must be written before the LUT is updated.

Look-Up Table Data Register REG[1E4h]							RW
LUT Data Bit 3	LUT Data Bit 2	LUT Data Bit 1	LUT Data Bit 0	n/a	n/a	n/a	n/a

bits 7-4 LUT Data Bits [3:0]

This register is used to read/write the RGB Look-Up Tables. This register accesses the entry at the pointer controlled by the Look-Up Table Address Register (REG[1E2h]). Accesses to the Look-Up Table Data Register automatically increment the pointer.

Note

The RGB data is inserted into the LUT after the Blue data is written, i.e. all three colors must be written before the LUT is updated.

8.3.14 Power Save Configuration Registers

Power Save Configuration Register REG[1F0h]							RW
n/a	n/a	n/a	Reserved	n/a	n/a	n/a	Power Save Mode Enable

bit 4 Reserved.
This bit must be set to 0.bit 0Power Save Mode Enable
When this bit = 1, the software initiated power save mode is enabled.
When this bit = 0, the software initiated power save mode is disabled.

Power Save Status Register REG[1F1h]							RO
n/a	n/a	n/a	n/a	n/a	n/a	LCD Power Save Status	Memory Controller Power Save Status

bit 1 LCD Power Save Status
This bit indicates the power save state of the LCD panel.
When this bit = 1, the panel is powered down.
When this bit = 0, the panel is powered up, or in transition of powering up or down.

Note
When this bit reads a 1, the system may safely shut down the LCD pixel clock source.

bit 0 Memory Controller Power Save Status
This bit indicates the power save state of the memory controller.
When this bit = 1, the memory controller is powered down and is either in self refresh or no refresh mode.
When this bit = 0, the memory controller is powered up and is either in CBR refresh or normal mode.

Note
When this bit reads a 1, the system may safely shut down the memory clock source.

8.3.15 Miscellaneous Registers

CPU-to-Memory Access Watchdog Timer Register REG[1F4h]							RW
n/a	n/a	Mem. Access Watchdog Timer bit 5	Mem. Access Watchdog Timer bit 4	Mem. Access Watchdog Timer bit 3	Mem. Access Watchdog Timer bit 2	Mem. Access Watchdog Timer bit 1	Mem. Access Watchdog Timer bit 0

bits 5-0 CPU-to-Memory Access Watchdog Timer

A non-zero value in this register enables the watchdog timer for CPU-to-memory access. When enabled, any CPU-to-memory access cycle will be completed successfully within a time determined by the following equation:

$$\text{Maximum CPU-to-memory access cycle time} = (8n + 7) \times T_{bclk} + 13 \times T_{mclk}$$

where:

n = A non-zero value in this register

T_{bclk} = Bus clock period, or Bus clock period x 2 (if MD12 = 1, see Table 5-6: on page 31)

T_{mclk} = Memory clock period

This function is required by some busses which time-out if the cycle duration exceeds a certain time period. This function is **not intended to arbitrarily shorten the CPU-to-memory access cycle time** in order gain higher CPU bandwidth. Doing so may significantly reduce the available display refresh bandwidth which may cause display corruption. This register does not affect CPU-to-register access or BitBLT access.

8.3.16 Common Display Mode Register

Display Mode Register REG[1FCh]							RW
n/a	SwivelView™ Enable Bit 0	n/a	n/a	n/a	Display Mode Select Bit 2	Display Mode Select Bit 1	Display Mode Select Bit 0

bit 6 SwivelView™ Enable Bit 0

When this bit = 1, the LCD and CRT display image is rotated 90° clockwise. Please refer to Section 15, "SwivelView™" on page 194 for application and limitations.

When this bit = 0, there is no hardware effect.

This bit in conjunction with SwivelView™ Enable Bit 1 achieves the following hardware rotations.

Table 8-35: Setting SwivelView Modes

SwivelView Enable Bits	**SwivelView™ Modes**			
	Normal	**SwivelView 90°**	**SwivelView 180°**	**SwivelView 270°**
SwivelView Enable Bit 0 (REG[1FCh] bit 6)	0	1	0	1
SwivelView Enable Bit 1 (REG[040h] bit 4)	0	0	1	1

bits 2-0 Display Mode Select Bits [2:0]

These bits select the display model according to the following table. The LCD display mode is enabled/disabled using bit 0. Programming this bit from a 0 to a 1 starts the power-on sequence. Programming this bit from a 1 to a 0 starts the power-off sequence.

Table 8-36: Display Mode Selection

Display Mode Select Bits [2:0]	**Display Mode Enabled**
000	no display
001	LCD only
010	CRT only
011	EISD (CRT and LCD)
100	TV with flicker filter off
101	EISD (TV with flicker filter off and LCD)
110	TV with flicker filter on
111	EISD (TV with flicker filter on and LCD)

Note

REG[018h] bit 7 must be set to 1 when the flicker filter is enabled.

Note

The **Flicker Filter** reduces the "flickering" effect seen on interlaced displays by averaging adjacent lines on the TV display. This "flickering" is caused by sharp vertical image transitions that occur over one line (1 vertical pixel). For example, one pixel high lines, edges of window boxes, etc. Flickering occurs because these high resolution lines are effectively displayed at half the refresh frequency due to interlacing.

8.3.17 MediaPlug Register Descriptions

The S1D13506 has built-in support for Winnov's MediaPlug connection designed for video cameras. The following registers are used to control the connection and accept data from the camera. The MediaPlug registers decode A11-A0 and require A20 = 0 and A12 = 1. The MediaPlug registers are 16-bit wide. Byte access to the MediaPlug registers is not allowed. For further information, see Section 17, "MediaPlug Interface" on page 205.

Note

The MediaPlug control registers must not be accessed while Power Save Mode is enabled (REG[1F0h] bit 0 = 1).

MediaPlug LCMD Register REG[1000h]							RW
LCMD Bit 7	LCMD Bit 6	LCMD Bit 5	LCMD Bit 4	LCMD Bit 3	LCMD Bit 2	LCMD Bit 1	LCMD Bit 0
LCMD Bit 15	LCMD Bit 14	LCMD Bit 13	LCMD Bit 12	LCMD Bit 11	LCMD Bit 10	LCMD Bit 9	LCMD Bit 8

REG[1000h] bits 15-0 MediaPlug LCMD Bits [15:0]

A 16-bit register for setting and detecting various modes of operation of the MediaPlug Local Slave. This register is handled differently for reads and writes. The following table shows the MediaPlug description of the LCMD Register. See bit descriptions for details.

Table 8-37: MediaPlug LCMD Read/Write Descriptions

Data	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Write	TO[2:0]		Xxxxxxxxxx										IC	MC	P	W
Read	TO[2:0]		00b		Rev[3:0]				Rstat[2:0]			0b	IC	MC	P	W

bits 15-14 Timeout Option (MediaPlug Parameter TO)

These bits select the timeout delay in MediaPlug clock cycles:

Table 8-38: Timeout Option Delay

Timeout Option Bits[15:14]	**Timeout (MediaPlug clock cycles)**
00	1023 (default)
01	64
10	128
11	64

bits 13-12
A read from these bits will always return 00b.
A write to these bits has no hardware effect.

bits 11-8
MediaPlug IC Revision (MediaPlug Parameter Rev)
The revision for this MediaPlug IC is “0011b”.
A write to these bits has no hardware effect.

bit 7
Cable Detected Status (MediaPlug Parameter Rstat)
The cable detected status as determined by the MPD(1) pin.
When this bit = 0, a MediaPlug cable is connected.
When this bit = 1, a MediaPlug cable is not detected.
A write to this bit has no hardware effect.

bit 6
A read from this bit will always return 0b.
A write to this bit has no hardware effect.

bit 5
Remote Powered Status (MediaPlug Parameter Rstat)
The remote powered status as determined by the RCTRL pin.
When this bit = 0, the remote is not powered.
When this bit = 1, the remote is powered and connected.
A write to this bit has no hardware effect.

Table 8-39: Cable Detect and Remote Powered Status

Cable Detected Status [bit 7]	Remote Powered Status [bit 5]	Status
0	0	cable connected but remote not powered
0	1	cable connected and remote powered
1	x	cable not connected

bit 4
A read from this bit will always return 0b.
A write to this bit has no hardware effect.

bit 3
MediaPlug Interface Clock Enable (MediaPlug Parameter IC)
When this bit = 0, the MediaPlug interface clock is enabled (default).
When this bit = 1, the MediaPlug interface clock is disabled.

bit 2
MediaPlug Clock (MediaPlug Parameter MC)
When this bit = 0, the MediaPlug cable clock is disabled (default).
When this bit = 1, the MediaPlug cable clock is enabled.

bit 1
Power Enable to Remote (MediaPlug Parameter P)
When this bit = 0, power to remote is off (default).
When this bit =1, power to remote is on.

bit 0
Watchdog Disable (MediaPlug Parameter W)
When this bit = 0, the MediaPlug watchdog is enabled (default).
When this bit = 1, the MediaPlug watchdog is disabled.

MediaPlug Reserved LCMD Register REG[1002h] RW							
LCMD Bit 23	LCMD Bit 22	LCMD Bit 21	LCMD Bit 20	LCMD Bit 19	LCMD Bit 18	LCMD Bit 17	LCMD Bit 16
LCMD Bit 31	LCMD Bit 30	LCMD Bit 29	LCMD Bit 28	LCMD Bit 27	LCMD Bit 26	LCMD Bit 25	LCMD Bit 24

REG[1002h] bits 15-0 MediaPlug Reserved LCMD Bits [15:0]
This register is not implemented and is reserved for future expansion of the LCMD register. A write to this register has no hardware effect. A read from this register always return 0000h.

MediaPlug CMD Register REG[1004h] RW							
CMD Bit 7	CMD Bit 6	CMD Bit 5	CMD Bit 4	CMD Bit 3	CMD Bit 2	CMD Bit 1	CMD Bit 0
CMD Bit 15	CMD Bit 14	CMD Bit 13	CMD Bit 12	CMD Bit 11	CMD Bit 10	CMD Bit 9	CMD Bit 8

REG[1002h] bits 15-0 MediaPlug CMD Bits [15:0]
A 16-bit register for setting the MediaPlug commands. This register is handled differently for reads and writes. The following table shows the MediaPlug description of the CMD Register. See bit descriptions for details.

Table 8-40: MediaPlug CMD Read/Write Descriptions

Data	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Write	I[12:0]													C[2:0]		
Read	D	T	I[10:0]											C[2:0]		

bit 15 Dirty Bit (MediaPlug Parameter D)
This bit is set by the hardware when the command register is written.
It is cleared by hardware by the following conditions:
1. Remote-Reset (After this command has been acknowledged by remote.
2. End_Stream (After this command has been acknowledged by remote.
3. Write to DATA register if the CCC field is Write_Reg.
4. Read to DATA register if the CCC field is Read_Reg.
It is also set when the Remote Machine loses power or the cable is disconnected.

bit 14 Timeout Bit (MediaPlug Parameter T)
It is set when Watchdog is enabled and MediaPlug read or write cycle takes longer than 64, 128, 1024 cycles of MediaPlug clock depending on LCMD register settings.
It is also set when the remote is not powered.
It is cleared at the beginning of every command write by the host.

bits 13-3 Index Field (MediaPlug Parameter I)
This field is the address presented by the remote to the remote function. MediaPlug transmits the entire 16-bits of the first word of the command Register as written, but I12 (D15) and I11 (D14) are hidden from readback by the dirty bit and Watchdog error bit.

bit 2-0 Command Field (MediaPlug Parameter C)
Selects the command as follows:

Table 8-41: MediaPlug Commands

Command Field [bits 2:0]	Command
000	Remote-Reset: Hardware reset of remote.
001	Stream-End: Indicates end of data streaming operation.
010	Write-Register: Write remote register INDEX[5:0] with DATA.
011	Read-Register: Read remote register INDEX[5:0] to DATA.
100	Write_Stream: Begin streaming data to the remote.
101	NOP: The command is sent across the MediaPlug. There is no other effect.
110	NOP: The command is sent across the MediaPlug. There is no other effect.
111	Read-Stream: Begin streaming data from the remote.

MediaPlug Reserved CMD Register
REG[1006h] RW

CMD Bit 23	CMD Bit 22	CMD Bit 21	CMD Bit 20	CMD Bit 19	CMD Bit 18	CMD Bit 17	CMD Bit 16
CMD Bit 31	CMD Bit 30	CMD Bit 29	CMD Bit 28	CMD Bit 27	CMD Bit 26	CMD Bit 25	CMD Bit 24

REG[1006h] bits 15-0 MediaPlug Reserved CMD Bits [15:0]
This register is not implemented and is reserved for future expansion of the CMD register. A write to this register has no hardware effect. A read from this register always return 0000h.

MediaPlug Data Register
REG[1008h] to REG[1FFEh], even address RW

Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
Data Bit 15	Data Bit 14	Data Bit 13	Data Bit 12	Data Bit 11	Data Bit 10	Data Bit 9	Data Bit 8

Data Register bits 15-0 MediaPlug Data Bits [15:0]
A 16-bit register used for read/write and streaming read/write of MediaPlug data. This register is loosely decoded from 1008h to 1FFEh so that the port may be accessed using DWORD block transfer instructions.

8.3.18 BitBLT Data Registers Descriptions

The BitBLT data registers decode A19-A0 and require A20 = 1. The BitBLT data registers are 16-bit wide. Byte access to the BitBLT data registers is not allowed.

BitBLT Data Register 0 A20-A0 = 100000h-1FFFFEh, even address							RW
Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
Data Bit 15	Data Bit 14	Data Bit 13	Data Bit 12	Data Bit 11	Data Bit 10	Data Bit 9	Data Bit 8

Data Register bits 15-0 BitBLT Data Bits [15:0]
A 16-bit register that specifies the BitBLT data. This register is loosely decoded from 100000h to 1FFFFEh.

9 2D BitBLT Engine

The S1D13506 has a built-in 2D BitBLT engine which increases the performance of Bit Block Transfers (BitBLT). This section will discuss the BitBLT engine design and functionality.

9.1 Functional Description

The 2D BitBLT engine is designed using a 16-bit architecture. It implements a 16-bit data bus and supports both 8 and 16 bit-per-pixel color depths.

The BitBLT engine supports rectangular and linear addressing modes for source and destination in a positive direction for all BitBLT operations except the move BitBLT which also supports in negative direction.

The BitBLT operations support byte alignment of all types. The BitBLT engine has a dedicated BitBLT IO access space allowing it to support multi-tasking applications. This allows the BitBLT engine to support simultaneous BitBLT and CPU read/write operations.

9.2 BitBLT Operations

Note
For details on the operation of the BitBLT registers, see Section 8.3.12, “BitBLT Configuration Registers” on page 154.

Write BitBLT

The Write BitBLT provides 16, two operand, ROP functions.

Move BitBLT

The Move BitBLT provides 16, two operand, ROP functions and is supported in both a positive and negative direction.

Read BitBLT

The Read BitBLT supports bit block transfers from the display buffer to the host. No ROP function is applied.

Solid Fill

The Solid Fill BitBLT fills a specified BitBLT area with a solid color as defined in the Foreground Color Register. In 8 bpp mode, only the low byte of the Foreground Color is used for solid fill.

Pattern Fill

The Pattern Fill BitBLT fills a specified BitBLT area with an 8 pixel by 8 line pattern in full color defined in off-screen display buffer. The pattern data has to be stored in a contiguous address (i.e. for 8 and 16 bpp, the pattern data will occupy 64 and 128 bytes respectively starting from the base address).

Any pixel within the 8x8 pattern can be used to start the fill area. The least significant bits of the source address start register are used to specify the starting pixel.

The 2D engine can detects the end of each line and continues from the beginning of the next line. When the last line of pattern is encountered, the first line of the pattern will be drawn on the following line.

Supports two full 16-bit operand ROP functions.

Note
The BitBLT operation Pattern Fill with ROP requires a BitBLT width ≥ 2. The BitBLT width is set in REG[110h], REG[111h].

Transparent Pattern Fill

The Transparent Pattern Fill fills a specified BitBLT area with an 8 pixel by 8 line pattern in full color defined in off-screen display buffer. The pattern data has to be stored in a contiguous address (i.e. for 8 and 16 bpp, the pattern data will occupy 64 and 128 bytes respectively starting from the base address).

When the pattern color is equal to the key color, which is defined in Background Color Register, the destination area is not updated. In 8 bpp mode, only the low byte of the key color is used for comparison.

For this BitBLT no raster operation is applied.

Note
The BitBLT operation Pattern Fill with transparency requires a BitBLT width ≥ 2. The BitBLT width is set in REG[110h], REG[111h].

Transparent Write BitBLT

The Transparent Write BitBLT supports bit block transfers from the host to display buffer.

When the source color is equal to key color, which is defined in Background Color Register, the destination area is not updated. In 8 bpp mode, only the low byte of the key color is used for comparison.

For this BitBLT no raster operation is applied.

Transparent Move BitBLT

The Transparent Move BitBLT supports bit block transfers from display buffer to display buffer in positive direction only.

When the source color is equal to key color, which is defined in Background Color Register, the destination area is not updated. In 8 bpp mode, only the low byte of key color is used for comparison.

For this BitBLT no raster operation is applied.

Color Expansion

The Color Expansion BitBLT expands the host's monochrome data to 8 or 16 bpp color format.

A 1 expands to the color defined in the Foreground Color Register. In 8 bpp mode, only the low byte of the Foreground Color Register is used.

A 0 expands to the color defined in the Background Color Register. In 8 bpp mode, only the low byte of the Background Color Register is used. If background transparency is enabled, then the destination color will remain untouched.

The host will be continuously feeding a 16-bit data package. When the end of the line is reached, any unused bits will be discarded. The data for the next line will be taken from the next data package. The low byte write data will be used first for the operation. Each bit is serially expanded to the destination data starting from MSB (Bit 7) to LSB (Bit 0).

This BitBLT supports any bit alignment, but supports in a positive direction only.

Move BitBLT with Color Expansion

The Move BitBLT with Color Expansion expands off-screen source's monochrome data to 8 or 16 bpp color format.

A 1 expands to the color defined in the Foreground Color Register.

A 0 expands to the color defined in the Background Color Register. If background transparency is enabled, then the destination color will remain untouched.

In 8 bpp mode, only the low byte of the Foreground Color Register and Background Color Register are used for color expansion. The low byte write data will be used first for the operation. Each bit is serially expanded to the destination data starting from MSB (Bit 7) to LSB (Bit 0).

This BitBLT supports byte alignment only and supports in a positive direction only.

10 Display Buffer

The system addresses the display buffer through the CS#, M/R#, and AB[20:0] input pins. When CS# = 0 and M/R# = 1, the display buffer is addressed by bits AB[20:0]. See the table below:

Table 10-1: S1D13506 Addressing

CS#	M/R#	Access
0	0	Register access - see Section 8.2, “Register Mapping” on page 116. • REG[000h] is addressed when AB[12:0] = 0 • REG[001h] is addressed when AB[12:0] = 1 • REG[n] is addressed when AB[12:0] = n
0	1	Memory access: the 2M byte display buffer is addressed by AB[20:0]
1	X	S1D13506 not selected

The display buffer address space is always 2M bytes. However, the physical display buffer may be either 512K bytes or 2M bytes – see Section 5.3, “Summary of Configuration Options” on page 31.

A 512K byte display buffer is replicated in the 2M byte address space – see Figure 10-1: “Display Buffer Addressing,” on page 175.

The display buffer can contain an image buffer, one or more Ink Layer/Hardware Cursor buffers, and a Dual Panel Buffer.

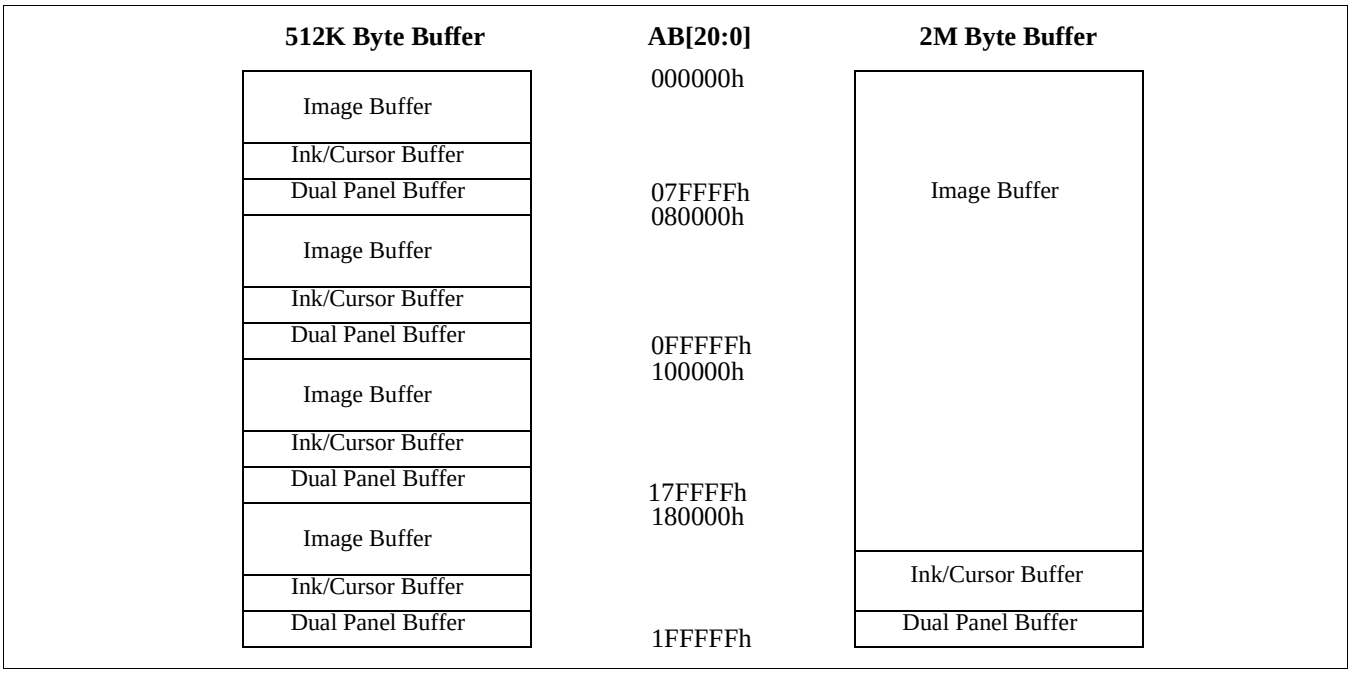

Figure 10-1: Display Buffer Addressing

10.1 Image Buffer

The image buffer contains the formatted display mode data – see Section 11.1, “Display Mode Data Format” on page 177.

The displayed image(s) may occupy only a portion of this space; the remaining area may be used for multiple images – possibly for animation or general storage. Section 11, “Display Configuration” on page 177 for the relationship between the image buffer and the displayed image.

10.2 Ink Layer/Hardware Cursor Buffers

The Ink Layer/Hardware Cursor buffers contain formatted image data for the Ink Layer and Hardware Cursor.

There may be several Ink Layer/Hardware Cursor images stored in the display buffer but only one may be active at any given time.

For details see Section 14, “Ink Layer/Hardware Cursor Architecture” on page 190.

10.3 Dual Panel Buffer

In dual panel mode a buffer is required and allocated by hardware. With this Dual Panel Buffer enabled, the top of the display buffer is allocated to the Dual Panel Buffer. The size of the Dual Panel Buffer is a function of the panel resolution and whether the panel is color or monochrome:

Dual Panel Buffer Size (in bytes) = (panel width x panel height) x factor / 16

where factor: = 4 for color panel
= 1 for monochrome panel

Note
Calculating the size of the Dual Panel Buffer is required to avoid overwriting the Hardware Cursor/Ink Layer buffer.

Example 1: *For a 640x480 8 bpp color panel the Dual Panel Buffer size is 75K bytes. In a 512K byte display buffer, the Dual Panel Buffer resides from 6D400h to 7FFFFh. In a 2M byte display buffer, the Dual Panel Buffer resides from 1ED400h to 1FFFFFh.*

11 Display Configuration

11.1 Display Mode Data Format

The following diagrams show the display mode data formats for a little endian system:

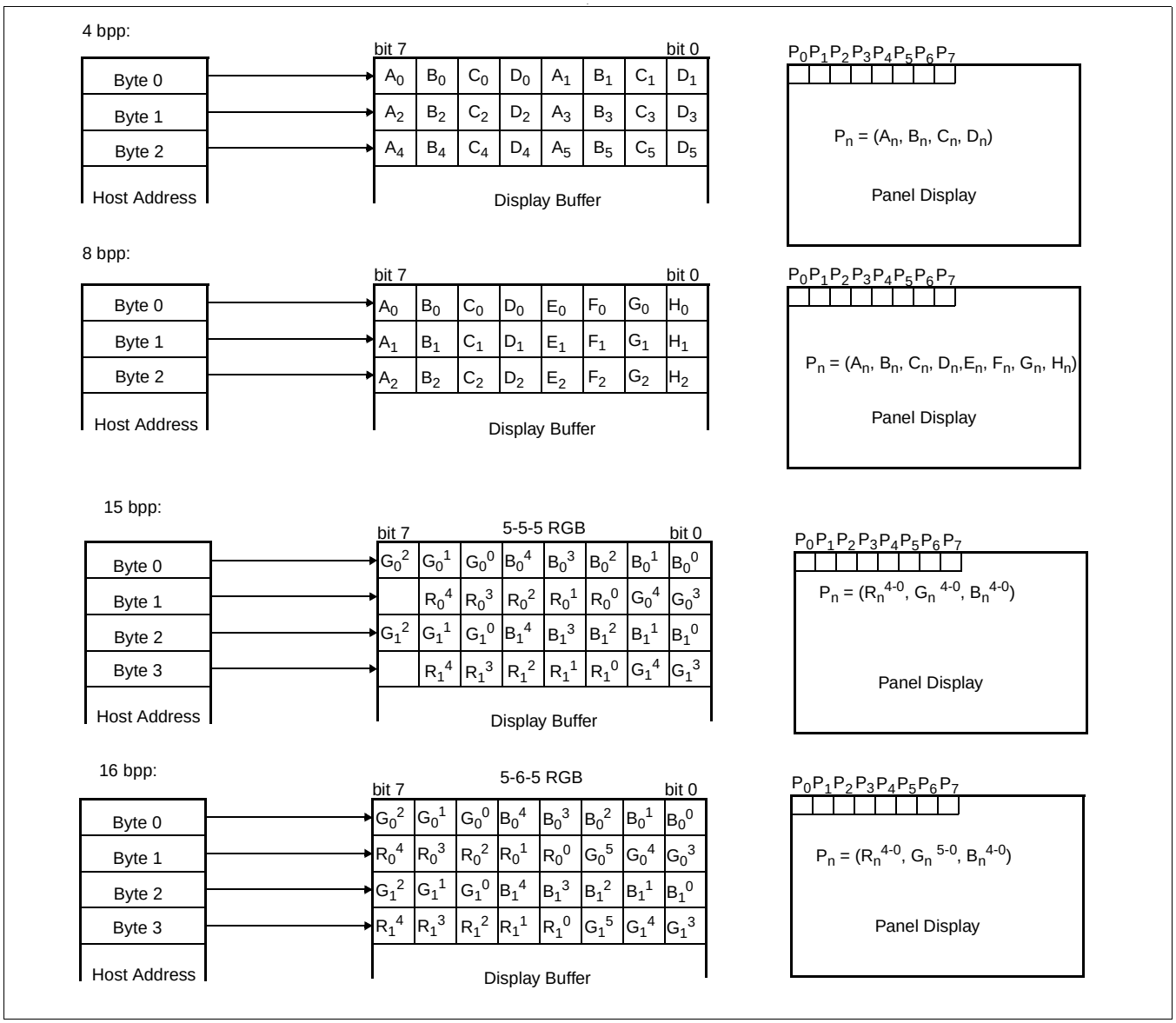

Figure 11-1: 4/8/15/16 Bit-per-pixel Format Memory Organization

Note

1. The Host-to-Display mapping shown here is for a little endian system.
2. For 15/16 bit-per-pixel formats, R_n, G_n, B_n represent the red, green, and blue color components.

11.2 Image Manipulation

The figure below shows how the screen image is stored in the image buffer and positioned on the LCD display. The screen image on the CRT/TV is manipulated similarly. When EISD is enabled (see Section 16, “EPSON Independent Simultaneous Display (EISD)” on page 203), the images on the LCD and on the CRT/TV are independent of each other.

- For LCD: REG[047h], REG[046h] defines the width of the virtual image.
  For CRT/TV: REG[067h], REG[066h] defines the width of the virtual image.
- For LCD: REG[044h], REG[043h], REG[042h] defines the starting word of the displayed image.
  For CRT/TV: REG[064h], REG[063h], REG[062h] defines the starting word of the displayed image.
- For LCD: REG[048h] defines the starting pixel within the starting word.
  For CRT/TV: REG[068h] defines the starting pixel within the starting word.
- For LCD: REG[032h] defines the width of the LCD display.
  For CRT/TV: REG[050h] defines the width of the CRT/TV display.
- For LCD: REG[039h], REG[038h] defines the height of the LCD display.
  For CRT/TV: REG[057h], REG[056h] defines the height of the CRT/TV display.

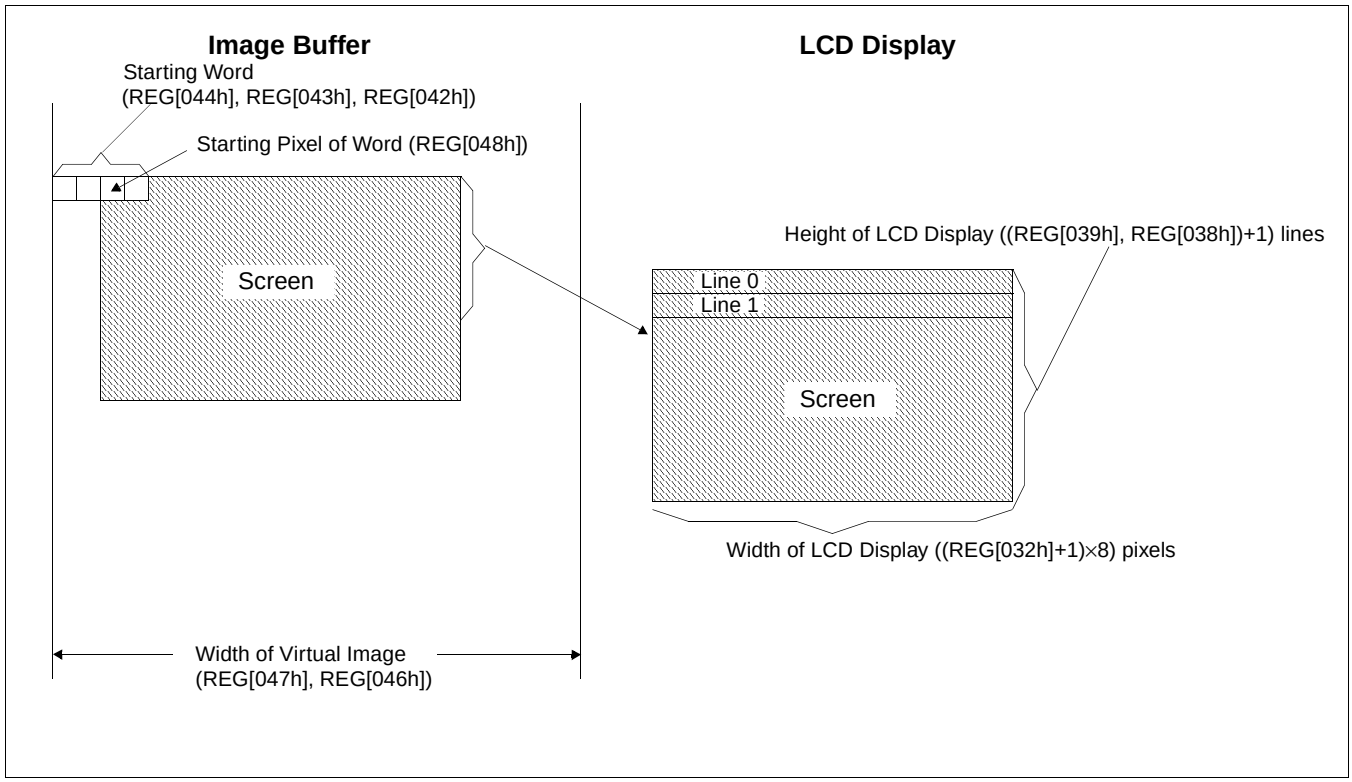

Figure 11-2: Image Manipulation

12 Look-Up Table Architecture

The following depictions are intended to show the display data output path only.

12.1 Monochrome Modes

The green LUT is used for all monochrome modes.

4 Bit-Per-Pixel Monochrome Mode

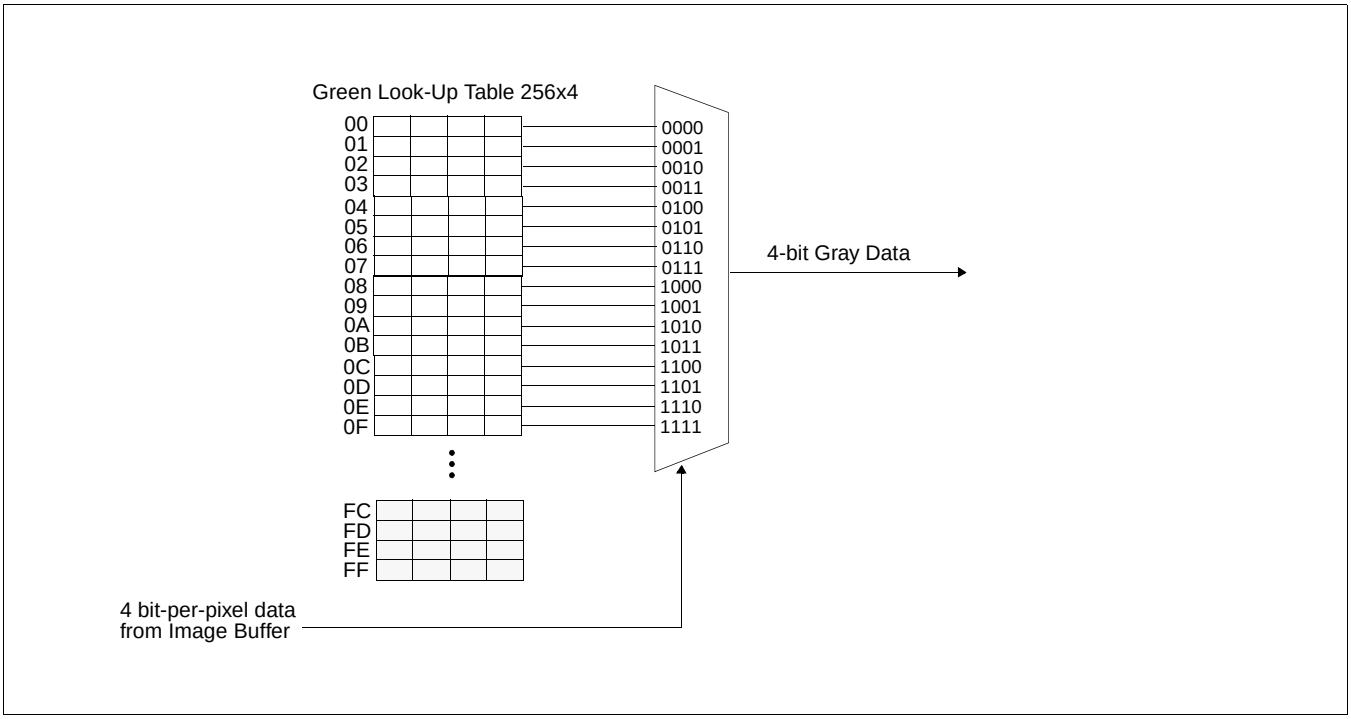

Figure 12-1: 4 Bit-Per-Pixel Monochrome Mode Data Output Path

12.2 Color Modes

4 Bit-Per-Pixel Color

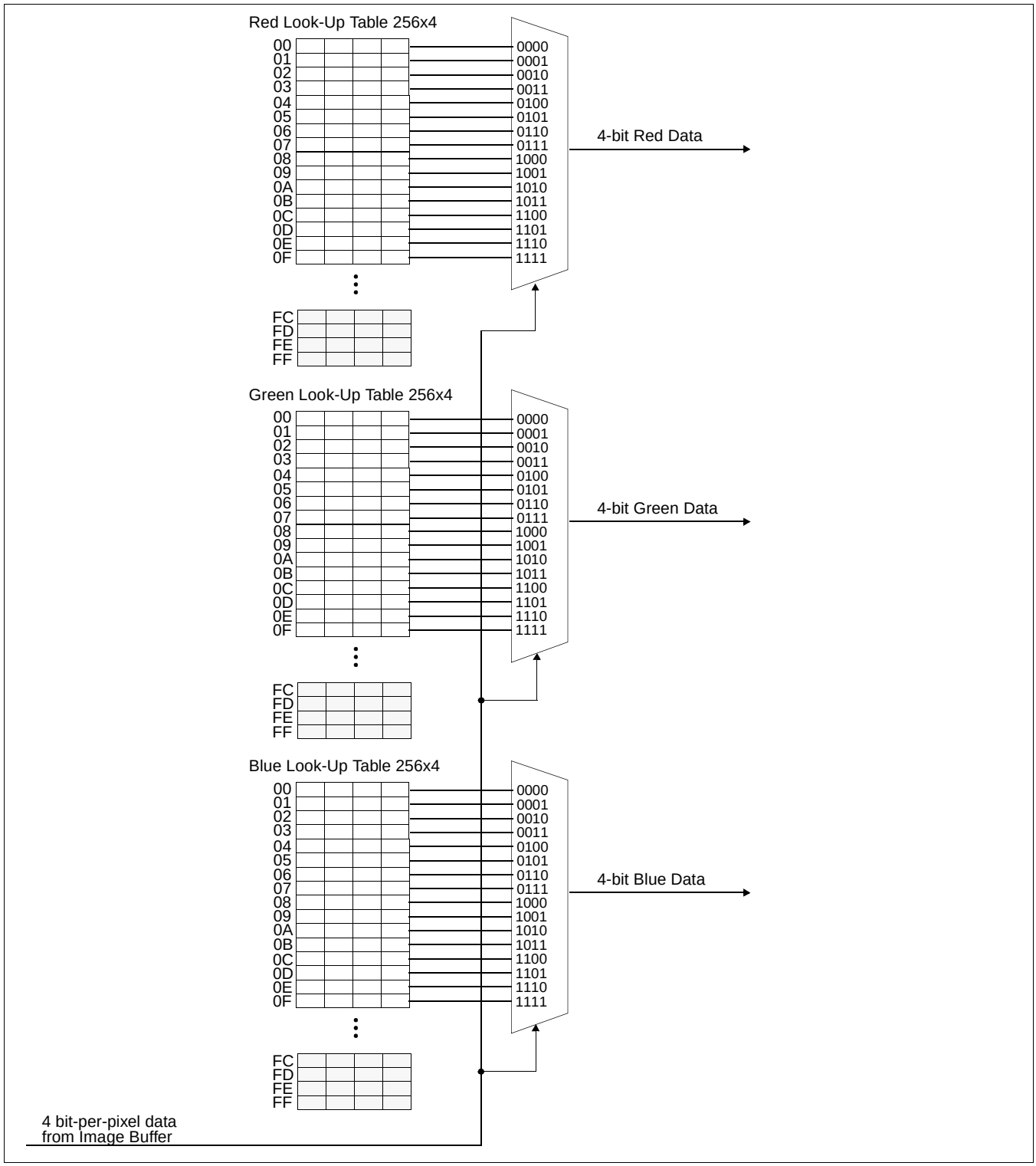

Figure 12-2: 4 Bit-Per-Pixel Color Mode Data Output Path

8 Bit-Per-Pixel Color

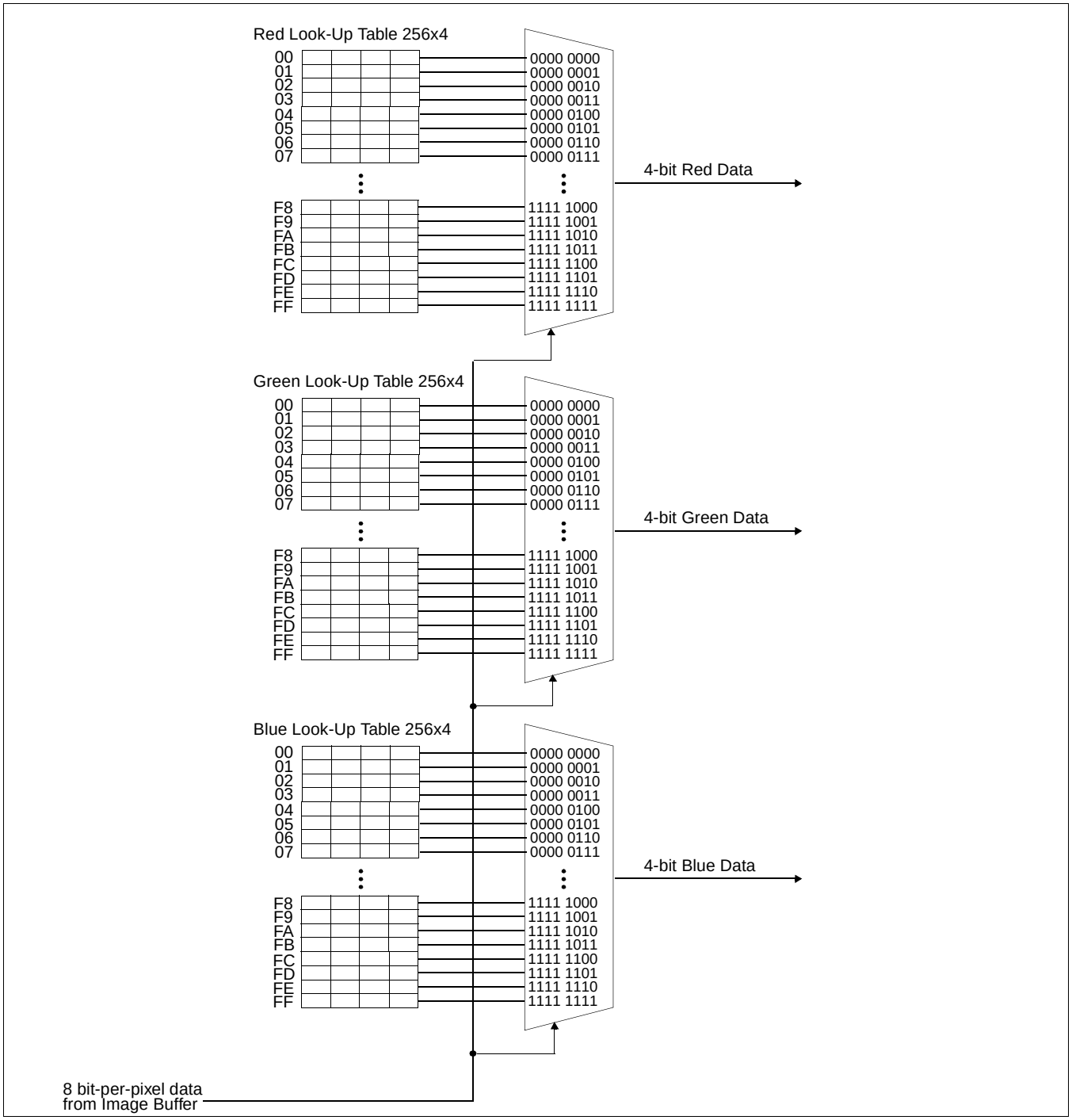

Figure 12-3: 8 Bit-Per-Pixel Color Mode Data Output Path

15/16 Bit-Per-Pixel Color Modes

The LUT is bypassed and the color data is directly mapped for these color depths– See "Display Configuration" on page 177.

13 TV Considerations

13.1 NTSC/PAL Operation

NTSC or PAL video is supported in either composite or S-video format. Filters may be enabled to reduce the distortion associated with displaying high resolution computer images on an interlaced TV display. The image can be vertically and horizontally positioned on the TV. Additionally, a dedicated Hardware Cursor (independent from the LCD display) is supported.

13.2 Clock Source

The required clock frequencies for NTSC/PAL are given in the following table:

Table 13-1: Required Clock Frequencies for NTSC/PAL

TV Format	Required Clock Frequency
NTSC	14.318180 MHz (3.579545 MHz subcarrier)
PAL	17.734475 MHz (4.43361875 MHz subcarrier)

13.3 Filters

When displaying computer images on a TV, several image distortions are likely to arise:

- cross-luminance distortion.
- cross-chrominance distortion.
- flickering.

These distortions are caused by the high-resolution nature of computer images which typically contain sharp color transitions, and sharp luminance transitions (e.g., high contrast one pixel wide lines and fonts, window edges, etc.). Three filters are available to reduce these distortions.

13.3.1 Chrominance Filter (REG[05Bh] bit 5)

The chrominance filter adjusts the color of the TV by limiting the bandwidth of the chrominance signal (reducing cross-luminance distortion). This reduces the “ragged edges” seen at boundaries between sharp color transitions. This filter is controlled using REG[05Bh] bit 5 and is most useful for composite video output.

13.3.2 Luminance Filter (REG[05Bh] bit 4)

The luminance filter adjusts the brightness of the TV by limiting the bandwidth of the luminance signal (reducing cross-chrominance distortion). This reduces the “rainbow-like” colors at boundaries between sharp luminance transitions. This filter is controlled using REG[05Bh] bit 4 and is most useful for composite video output.

13.3.3 Anti-flicker Filter (REG[1FCh] bits [2:1])

The “flickering” effect seen on interlaced displays is caused by sharp vertical image transitions that occur over one line (1 vertical pixel). For example, one pixel high lines, edges of window boxes, etc. Flickering occurs because these high resolution lines are effectively displayed at half the refresh frequency due to interlacing. The anti-flicker filter averages adjacent lines on the TV display to reduce flickering. This filter is controlled using the Display Mode register (REG[1FCh] bits [2:1]).

13.4 TV Output Levels

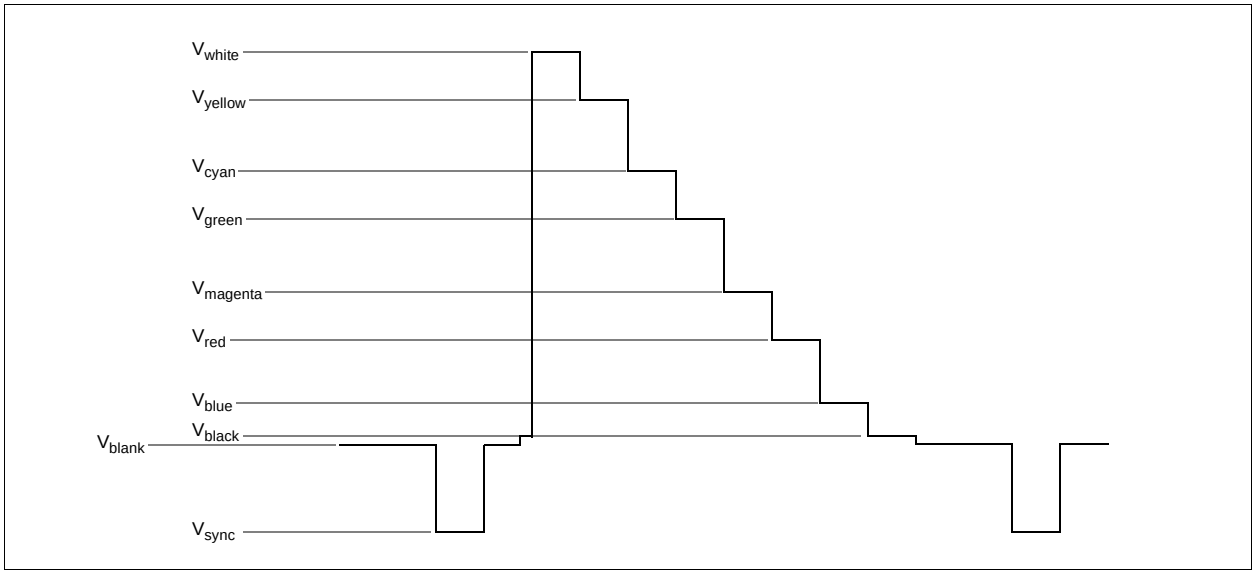

Figure 13-1: NTSC/PAL SVideo-Y (Luminance) Output Levels

Table 13-2: NTSC/PAL SVideo-Y (Luminance) Output Levels

Symbol	Parameter	RGB	NTSC / PAL (mv)	NTSC / PAL (IRE)
V_{white}	White	1F 3F 1F	996	99.5
V_{yellow}	Yellow	1F 3F 00	923	89
V_{cyan}	Cyan	00 3F 1F	798	72
V_{green}	Green	00 3F 00	725	62
$V_{magenta}$	Magenta	1F 00 1F	608	45
V_{red}	Red	1F 00 00	536	35
V_{blue}	Blue	00 00 1F	410	17
V_{black}	Black	00 00 00	338	7.3
$V_{blanking}$	Blanking	N.A.	284	0
V_{sync}	Sync Tip	N.A.	0	-40

Note

RGB values assume a 16 bpp color depth with 5-6-5 pixel packing.

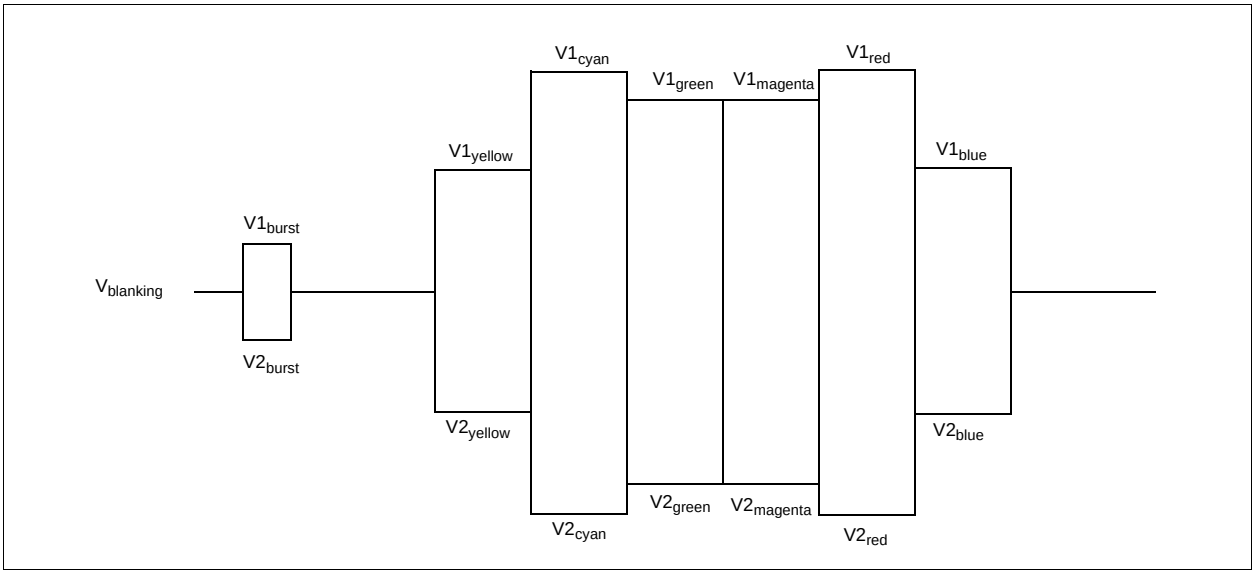

Figure 13-2: NTSC/PAL SVideo-C (Chrominance) Output Levels

Table 13-3: NTSC/PAL SVideo-C (Chrominance) Output Levels

Symbol	Parameter	RGB	NTSC / PAL (mv)	NTSC / PAL (IRE)
$V1_{burst}$	Burst positive peak	N.A.	552 / 541	
$V1_{yellow}$	Yellow positive peak	1F 3F 00	700	
$V1_{cyan}$	Cyan positive peak	00 3F 1F	815	
$V1_{green}$	Green positive peak	00 3F 00	751	
$V1_{magenta}$	Magenta positive peak	1F 00 1F	751	
$V1_{red}$	Red positive peak	1F 00 00	815	
$V1_{blue}$	Blue positive peak	00 00 1F	700	
$V_{blanking}$	Blanking	N.A.	410	
$V2_{burst}$	Burst negative peak	N.A.	268 / 279	
$V2_{yellow}$	Yellow negative peak	1F 3F 00	121	
$V2_{cyan}$	Cyan negative peak	00 3F 1F	5	
$V2_{green}$	Green negative peak	00 3F 00	70	
$V2_{magenta}$	Magenta negative peak	1F 00 1F	70	
$V2_{red}$	Red negative peak	1F 00 00	5	
$V2_{blue}$	Blue negative peak	00 00 1F	121	

Note

RGB values assume a 16 bpp color depth with 5-6-5 pixel packing.

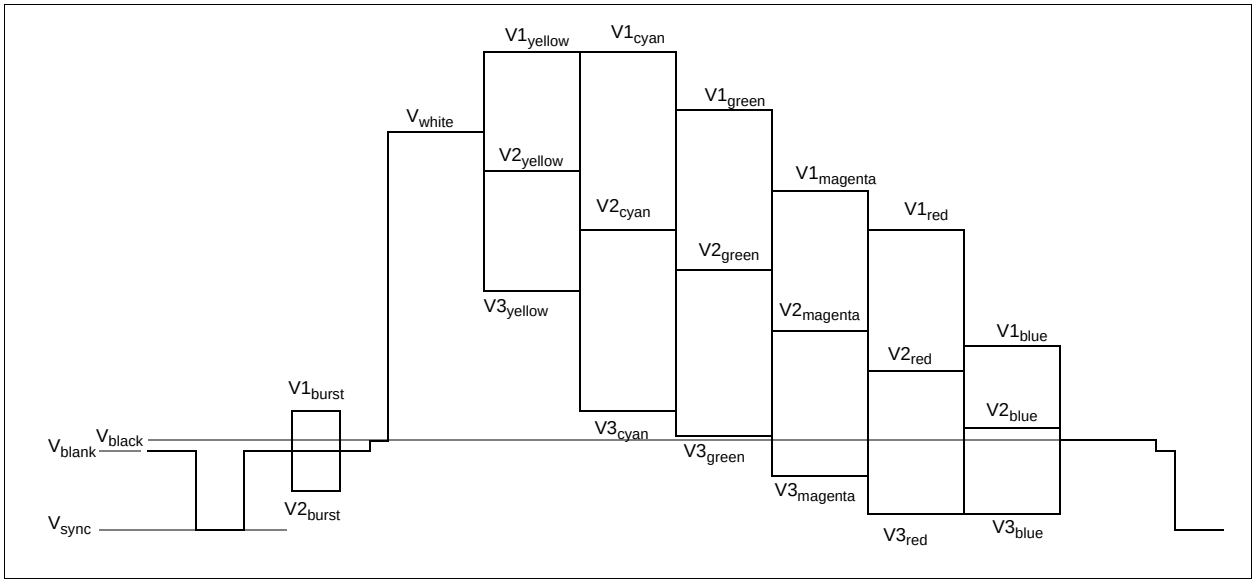

Figure 13-3: NTSC/PAL Composite Output Levels

Table 13-4: NTSC/PAL Composite Output Levels

Symbol	Parameter	RGB	NTSC / PAL (mv)	NTSC / PAL (IRE)
$V1_{yellow}$	Yellow chrominance positive peak	1F 3F 00	1211	130
$V1_{cyan}$	Cyan chrominance positive peak	00 3F 1F	1202	128
$V1_{green}$	Green chrominance positive peak	00 3F 00	1065	109
$V1_{magenta}$	Magenta chrominance positive peak	1F 00 1F	948	93
$V1_{red}$	Red chrominance positive peak	1F 00 00	939	92
$V1_{blue}$	Blue chrominance positive peak	00 00 1F	699	58
V_{white}	White luminance level	1F 3F 1F	995	99
$V2_{yellow}$	Yellow luminance level	1F 3F 00	923	89
$V2_{cyan}$	Cyan luminance level	00 3F 1F	797	72
$V2_{green}$	Green luminance level	00 3F 00	725	62
$V2_{magenta}$	Magenta luminance level	1F 00 1F	608	45
$V2_{red}$	Red luminance level	1F 00 00	535	35
$V2_{blue}$	Blue luminance level	00 00 1F	411	18
V_{black}	Black luminance level	00 00 00	338	7.3
$V3_{yellow}$	Yellow chrominance negative peak	1F 3F 00	634	49
$V3_{cyan}$	Cyan chrominance negative peak	00 3F 1F	392	15
$V3_{green}$	Green chrominance negative peak	00 3F 00	384	14
$V3_{magenta}$	Magenta chrominance negative peak	1F 00 1F	267	-2.6
$V3_{red}$	Red chrominance negative peak	1F 00 00	130	-22
$V3_{blue}$	Blue chrominance negative peak	00 00 1F	122	-23
V_{blank}	Blank Level	N.A.	284	0
$V1_{burst}$	Burst positive peak	N.A.	426 / 415	20 / 18
$V2_{burst}$	Burst negative peak	N.A.	142 / 153	-20 / -19
V_{sync}	Sync Tip	N.A.	0	-40

Note

RGB values assume a 16 bpp color depth with 5-6-5 pixel packing.

13.5 TV Image Display and Positioning

This section describes how to setup and position an image to be displayed on a TV. Figure 13-4: “NTSC/PAL Image Positioning,” on page 188 shows an image positioned on the TV display with the related programmable parameters. The TV display area is shaded.

The size of the display image determines the register values for the Horizontal Display Period, Horizontal Non-Display Period, Vertical Display Period, and Vertical Non-Display Period. The maximum and minimum values for these registers are given in Table 13-5: “Minimum and Maximum Values for NTSC/PAL”. The line period and frame period determined by these registers must also satisfy the following equations:

NTSC:

(((REG[050] bits[6:0]) + 1) x 8) + (((REG[052] bits[5:0]) x 8) + 6) = 910

({(REG[057] bits[1:0]), (REG[056] bits[7:0])}+1) + ((REG[058] bits[6:0])+1)x2+1) = 525

PAL:

(((REG[050] bits[6:0]) + 1) x 8) + (((REG[052] bits[5:0]) x 8) + 7) = 1135

({(REG[057] bits[1:0]), (REG[056] bits[7:0])}+1) + ((REG[058] bits[6:0])+1)x2+1) = 625

The HRTC Start Position and VRTC Start Position registers position the image horizontally and vertically. The maximum and minimum register values for these registers are given in Table 13-5: “Minimum and Maximum Values for NTSC/PAL”. Increasing the HRTC Start Position will move the image left, while increasing the VRTC Start Position will move the image up.

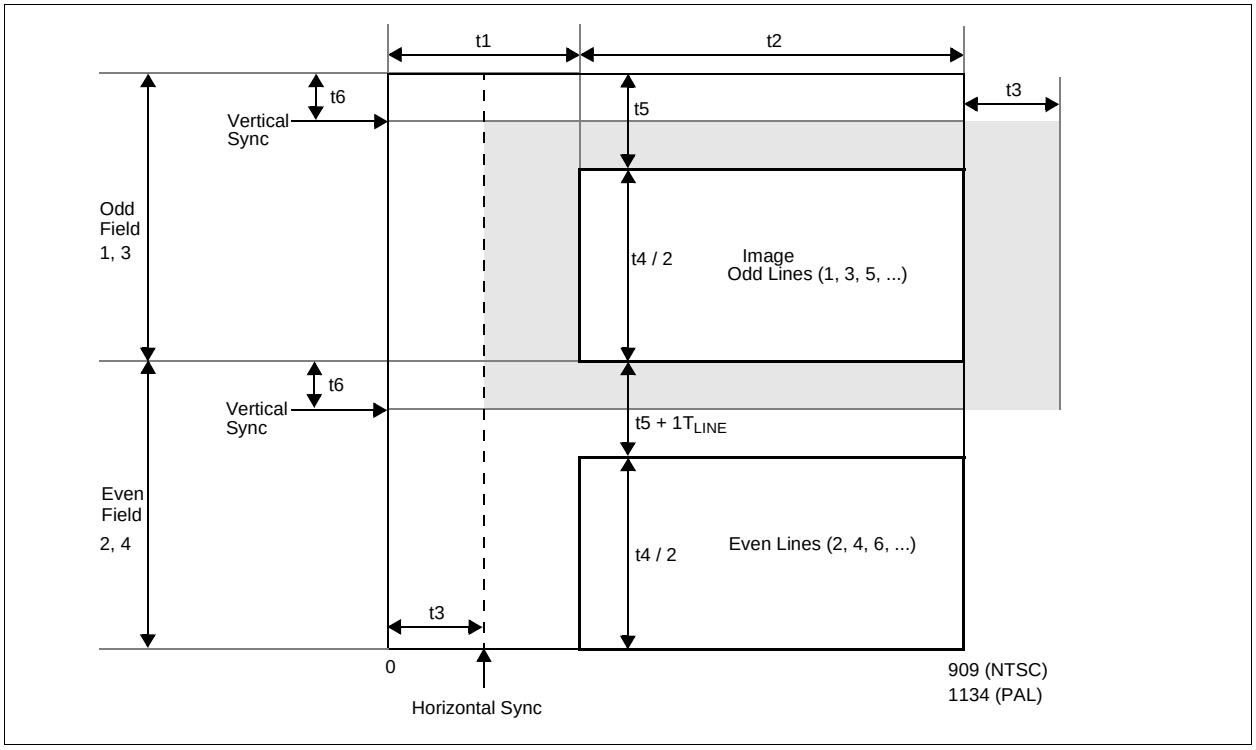

Figure 13-4: NTSC/PAL Image Positioning

The maximum Horizontal and Vertical Display Widths shown in Table 13-5: “Minimum and Maximum Values for NTSC/PAL” include display areas that are normally hidden by the edges of the TV. The visible display dimensions are shown in Figure 13-5: “Typical Total Display and Visible Display Dimensions for NTSC and PAL,” on page 189 as a guideline. The actual visible display area for a particular TV may differ slightly from those dimensions given. Table 13-6: “Register Values for Example NTSC/PAL Images” lists register values for some example images.

Table 13-5: Minimum and Maximum Values for NTSC/PAL

Symbol	Parameter	Register(s)	NTSC		PAL		Units
			min	max	min	max	
t1	TV Horizontal Non-Display Period	52	158	510	215	511	T_{4SC}
t2	TV Horizontal Display Width	50	400	752	624	920	T_{4SC}
t3	TV HRTC Start Position	53	25	t2 - 158	25	t2 - 215	T_{4SC}
t4	TV Vertical Display Height	57, 56	396	484	496	572	T_{LINE}
t5	TV Vertical Non-Display Period	58	20	64	26	64	T_{LINE}
t6	TV VRTC Start Position	59	0	t5 - 20	0	t5 - 26	T_{LINE}

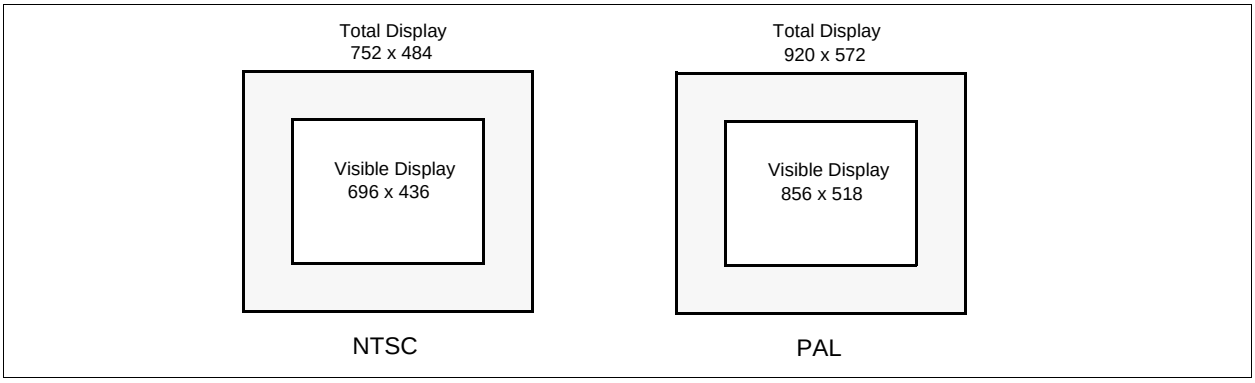

Figure 13-5: Typical Total Display and Visible Display Dimensions for NTSC and PAL

Note

For most implementations, the visible display does not equal the total display. The total display dimensions and the visible display dimensions must be determined for each specific implementation.

Table 13-6: Register Values for Example NTSC/PAL Images

Parameter	Register	NTSC			PAL			
		752x484	696x436	640x480	920x572	856x518	800x572	640x480
TV Horizontal Display Width	50	5Dh	56h	4Fh	72h	6Ah	63h	4Fh
TV Horizontal Non-Display Period	52	13h	1Ah	21h	1Ah	22h	29h	3Dh
TV HRTC Start Position	53	02h	04h	08h	02h	05h	09h	13h
TV Vertical Display Height	57	01h	01h	01h	02h	02h	02h	01h
	56	E3h	B3h	DFh	3Bh	05h	3Bh	DFh
TV Vertical Non-Display Period	58	13h	2Bh	15h	19h	34h	19h	47h
TV VRTC Start Position	59	00h	0Ch	01h	00h	0Dh	00h	16h

13.6 TV Cursor Operation

See Section 14, “Ink Layer/Hardware Cursor Architecture” on page 190.

14 Ink Layer/Hardware Cursor Architecture

14.1 Ink Layer/Hardware Cursor Buffers

The Ink Layer/Hardware Cursor buffers contain formatted image data for the Ink Layer or Hardware Cursor. There may be several Ink Layer/Hardware Cursor images stored in the display buffer but only one may be active at any given time. The active Ink Layer/Hardware Cursor buffer is selected by the Ink/Cursor Start Address register (REG[071h] for LCD, REG[081h] for CRT/TV). This register defines the start address for the active Ink/Cursor buffer. The Ink/Cursor buffer must be positioned where it does not conflict with the image buffer and Dual Panel Buffer. The start address for the Ink/Cursor buffer is programmed as shown in the following table.

Table 14-1: Ink/Cursor Start Address Encoding

Ink/Cursor Start Address Bits [7:0]	Start Address (Bytes)	Comments
0	Display Buffer Size - 1024	This default value is suitable for a cursor when there is no Dual Panel Buffer.
n = 255...1	Display Buffer Size - (n × 8192)	These positions can be used to: • position an Ink buffer at the top of the display buffer; • position an Ink buffer between the image and Dual Panel Buffers; • position a Cursor buffer between the image and Dual Panel Buffers; • select from a multiple of Cursor buffers.

The Ink/Cursor image is stored contiguously. The address offset from the starting word of line *n* to the starting word of line *n+1* is calculated as follows:

LCD Ink Address Offset (words) = REG[032h] + 1
CRT/TV Ink Address Offset (words) = REG[050h] + 1
LCD or CRT/TV Cursor Address Offset (words) = 8

14.2 Ink/Cursor Data Format

The Ink/Cursor image is always 2 bit-per-pixel. The following diagram shows the Ink/Cursor data format for a little endian system.

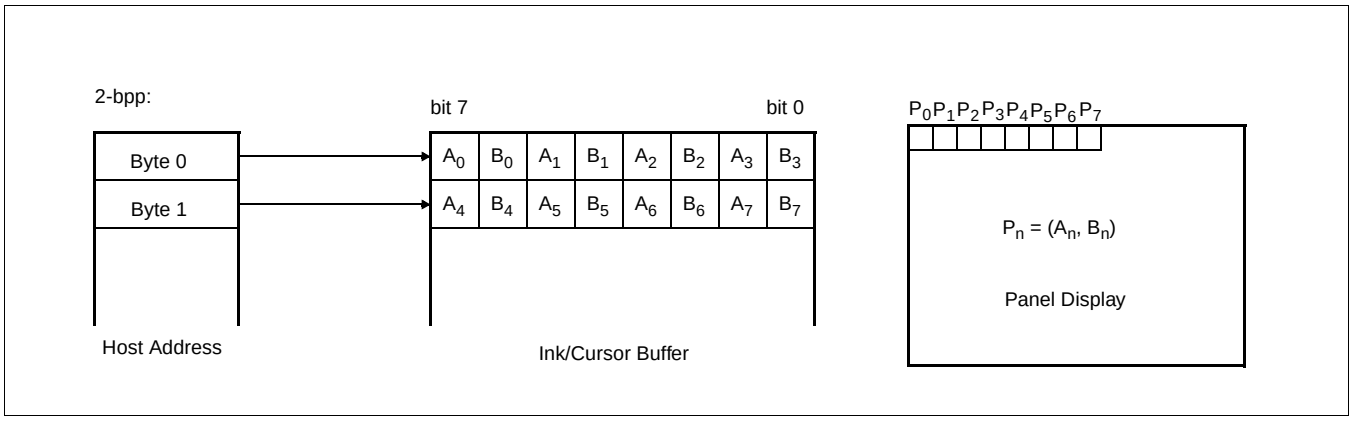

Figure 14-1: Ink/Cursor Data Format

The image data for pixel n, (A_n,B_n), selects the color for pixel n as follows.

Table 14-2: Ink/Cursor Color Select

(A_n,B_n)	Color	Comments
00	Color 0	Ink/Cursor Color 0 Register, (REG[078h], REG[077h], REG[076h] for LCD, REG[088h], REG[087h], REG[086h] for CRT/TV)
01	Color 1	Ink/Cursor Color 1 Register, (REG[07Ah], REG[07Bh],REG[07Ah] for LCD, REG[08Ah], REG[08Bh], REG[08Ah] for CRT/TV)
10	Background	Ink/Cursor is transparent – show background
11	Inverted Background	Ink/Cursor is transparent – show inverted background

14.3 Ink/Cursor Image Manipulation

14.3.1 Ink Image

The Ink image should always start at the top left pixel, i.e. Cursor X Position and Cursor Y Position registers should always be set to zero. The width and height of the ink image are automatically calculated to completely cover the display.

14.3.2 Cursor Image

The Cursor image size is always 64 x 64 pixels. The Cursor X Position and Cursor Y Position registers specify the position of the top left pixel. The following diagram shows how to position an unclipped cursor.

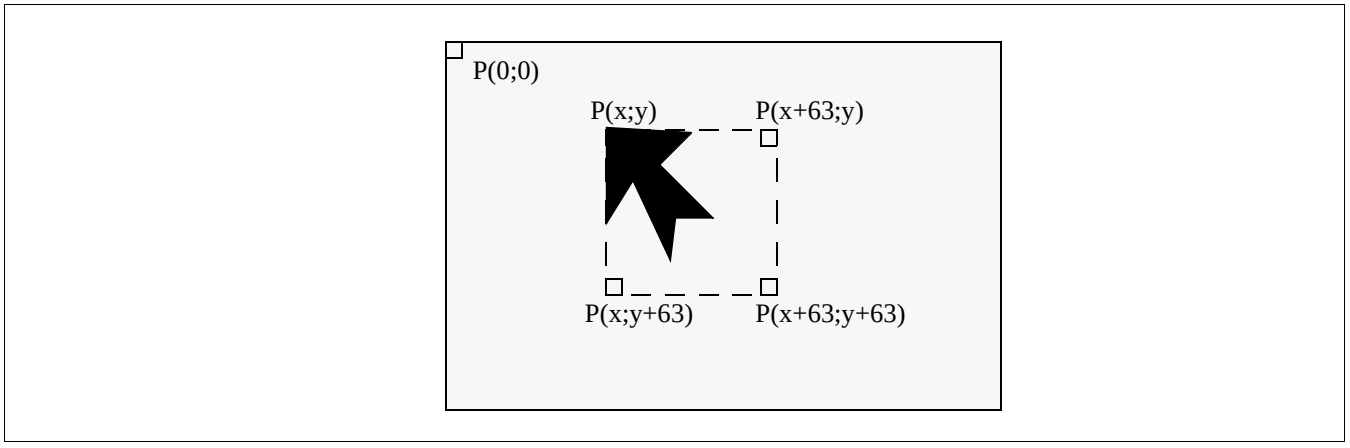

Figure 14-2: Unclipped Cursor Positioning

where

For LCD:
x = (REG[073h] bits [1:0], REG[072h]) **and** REG[073h] bit 7 = 0
y = (REG[075h] bits [1:0], REG[074h]) **and** REG[075h] bit 7 = 0

For CRT/TV:
x = (REG[083h] bits [1:0], REG[082h]) **and** REG[083h] bit 7 = 0
y = (REG[085h] bits [1:0], REG[084h]) **and** REG[085h] bit 7 = 0

The following diagram shows how to position a cursor that is clipped at the top and left sides of the display.

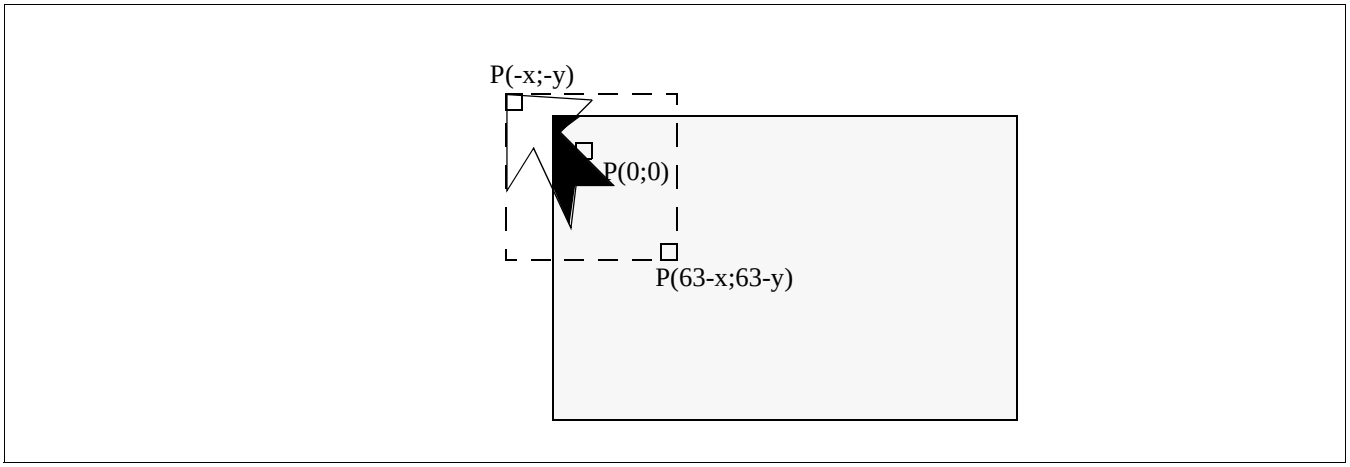

Figure 14-3: Clipped Cursor Positioning

where

For LCD:
x = (REG[073h] bits [1:0], REG[072h]) <= 63 **and** REG[073h] bit 7 = 1
y = (REG[075h] bits [1:0], REG[074h]) <= 63 **and** REG[075h] bit 7 = 1

For CRT/TV:
x = (REG[083h] bits [1:0], REG[082h]) <= 63 **and** REG[083h] bit 7 = 1
y = (REG[085h] bits [1:0], REG[084h]) <= 63 **and** REG[085h] bit 7 = 1

15 SwivelView™

15.1 Concept

Most computer displays are refreshed in landscape – from left to right and top to bottom. Computer images are stored in the same manner. SwivelView™ is designed to rotate the displayed image on an LCD by 90°, 180°, or 270° in a clockwise direction. 90° rotation is also available on CRT.

The rotation is done in hardware and is transparent to the user for all display buffer reads and writes. By processing the rotation in hardware, SwivelView™ offers a performance advantage over software rotation of the displayed image.

15.2 90° SwivelView™

90° SwivelView™ uses a 1024 × 1024 pixel virtual window. The following figures show how the display buffer memory map changes in 90° SwivelView™. The display is refreshed in the following sense: C–A–D–B. The application image is written to the S1D13506 in the following sense: A–B–C–D. The S1D13506 rotates and stores the application image in the following sense: C–A–D–B, the same sense as display refresh.

The user can read/write to the display buffer naturally, without the need to rotate the image first in software. The registers that control the panning and scrolling of the panel window are designed for a landscape window. However, it is still possible to pan and scroll the portrait window in 90° SwivelView™, but the user must program these registers somewhat differently (See Section 15.2.1, “Register Programming” on page 195).

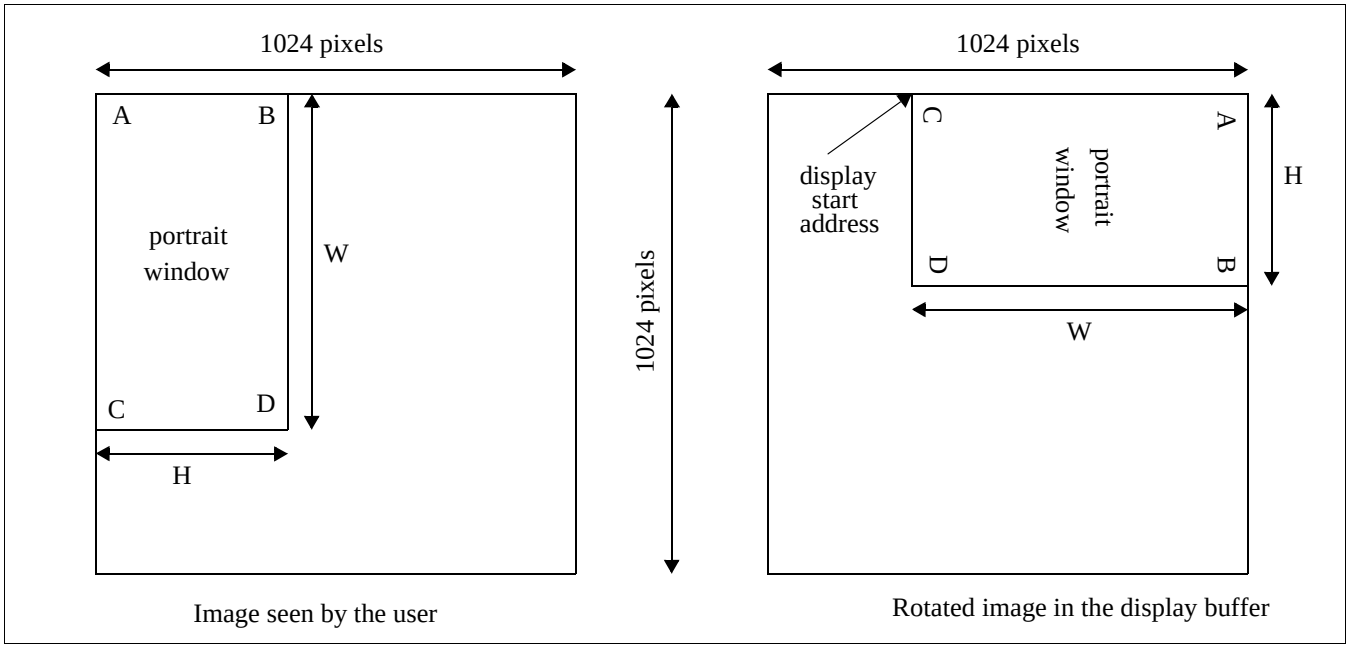

Figure 15-1: Relationship Between Screen Image and 90° Rotated Image in the Display Buffer

Note

W is the width of the LCD panel/CRT in number of pixels, (or the height of the portrait window in number of lines).
H is the height of the LCD panel/CRT in number of lines, (or the width of the portrait window in number of pixels).

Note

The image must be written with a 1024 pixel offset between adjacent lines (1024 bytes for 8 bpp mode or 2048 bytes for 15/16 bpp mode) and the display start address must be calculated (see below).

15.2.1 Register Programming

Enabling 90° Rotation on CPU Read/Write to Display Buffer

Set SwivelView™ Enable bit 0 to 1. All CPU accesses to the display buffer are translated to provide 90° clockwise rotation of the display image. SwivelView™ Enable bit 1 should be set to 0.

Memory Address Offset

The LCD/CRT Memory Address Offset register (REG[046h], REG[047h] for LCD, or REG[066h], REG[0667h] for CRT) must be set for a 1024 pixel offset:

LCD/CRT Memory Address Offset (words)

= 1024	for 15/16 bpp mode
= 512	for 8 bpp mode

Display Start Address

As seen in Figure 15-1: “Relationship Between Screen Image and 90° Rotated Image in the Display Buffer,” on page 195, the Display Start Address is determined by the location of the image corner “C”, and it is generally non-zero. The LCD/CRT Display Start Address register (REG[042h], REG[043h], REG[044h] for LCD, or REG[062h], REG[063h], REG[064h] for CRT) must be set accordingly.

LCD/CRT Display Start Address (words)

= (1024 - W)	for 15/16 bpp mode
= (1024 - W) / 2	for 8 bpp mode

where W is the width of the panel in number of pixels.

Horizontal Panning

Horizontal panning is achieved by changing the LCD/CRT Display Start Address register:

- Increase/decrease LCD/CRT Display Start Address register by 1024 (15/16 bpp mode) or 512 (8 bpp mode) pans the display window to the right/left by 1 pixel.

The amount the display window can be panned to the right is limited to 1024 pixels and limited by the amount of physical memory installed.

Vertical Scrolling

Vertical scrolling is achieved by changing the LCD/CRT Display Start Address register and/or the LCD/CRT Pixel Panning register:

- Increment/decrement LCD/CRT Display Start Address register in 8 bpp mode scrolls the display window up/down by 2 lines.
- Increment/decrement LCD/CRT Display Start Address register in 15/16 bpp mode scrolls the display window up/down by 1 line.
- Increment/decrement LCD/CRT Pixel Panning register in 8 bpp mode scrolls the display window up/down by 1 line.

15.2.2 Physical Memory Requirement

Because the user must now deal with a 1024×1024 virtual display, the amount of image buffer required for a particular display mode has increased. The minimum amount of image buffer required is:

Minimum Required Image Buffer (bytes)
= (1024 × H) × 2 for 15/16 bpp mode
= (1024 × H) for 8 bpp mode

where H is the height of the panel in number of lines.

This minimum amount is required to display a 90° SwivelView™ image without panning; scrolling, however, is permissible. The degree an image can be panned depends on the amount of physical memory installed and how much of that is used by the Dual Panel Buffer, Ink Layer, or Hardware Cursor. An image cannot be panned outside the 1024×1024 virtual display. Often it cannot be panned within the entire virtual display because part of the virtual display memory may be taken up by the Dual Panel Buffer, Ink Layer, Hardware Cursor, or even the CRT/TV display buffer.

The Dual Panel Buffer is used for dual panel mode. Its memory requirement is:

Dual Panel Buffer (bytes)
=(W × H) / 4 for color mode
=(W × H) / 16 for monochrome mode

where W is the width of the panel in number of pixels, and H is the height of the panel in number of lines.

The Dual Panel Buffer is always located at the end of the physical memory.

The Hardware Cursor or Ink Layer also takes up memory. If this memory is > 1KB, it must be located at an 8KB boundary, otherwise it may be located at the last 1KB area. The Hardware Cursor or Ink Layer must not overlap the image buffer or the Dual Panel Buffer.

The following table summarizes the DRAM size requirement for 90° SwivelView™ for different panel sizes and display modes. Note that DRAM size for the S1D13506 is limited to either 512K byte or 2M byte. The calculation is based on the minimum required image buffer size and the Dual Panel Buffer size. The Hardware Cursor/Ink Layer may or may not fit within this minimum DRAM configuration – this is noted in the table. The hardware cursor requires only 1KB of memory and so may resides at the last 1KB area if there is no Dual Panel Buffer, otherwise it must reside at an 8KB boundary. The 2-bit ink layer requires (W × H) / 4 bytes of memory; it must reside at an 8KB boundary. The table shows only one possible Hardware Cursor/Ink Layer location – at the highest possible location without interfering with the Dual Panel Buffer. It is also assumed that CRT/TV is not used.

Table 15-1: Minimum DRAM Size Required for SwivelView™

Panel Size	Panel Type		Display Mode	Min. Image Buffer Size	Dual Panel Buffer Size	Minimum DRAM Size	Ink/Cursor Buffer Size	Ink/Cursor Location
320 × 240	Single	Color	8 bpp	240KB	0KB	512KB	18.75KB/1KB	488KB/511KB
			15/16 bpp	480KB				
		Mono	8 bpp	240KB				
			15/16 bpp	480KB				
640 × 480	Single	Color	8 bpp	480KB	0KB		75KB/1KB	--/511KB
			15/16 bpp	960KB		2MB		1968KB/2047KB
		Mono	8 bpp	480KB		512KB		--/511KB
			15/16 bpp	960KB		2MB		1968KB/2047KB
	Dual	Color	8 bpp	480KB	75KB			1896KB/1968KB
			15/16 bpp	960KB				
		Mono	8 bpp	480KB	18.75KB	512KB		--/488KB
			15/16 bpp	960KB		2MB		1952KB/2024KB
800 × 600	Single	Color	8 bpp	600KB	0KB		117.19KB/1KB	1928KB/2047KB
			15/16 bpp	1.2MB				
		Mono	8 bpp	600KB				
			15/16 bpp	1.2MB				
	Dual	Color	8 bpp	600KB	117.19KB			1808KB/1928KB
			15/16 bpp	1.2MB				
		Mono	8 bpp	600KB	29.30KB			1896KB/2016KB
			15/16 bpp	1.2MB				

Where KB = 1024 bytes and MB = 1024KB

15.2.3 Limitations

The following limitations apply to 90° SwivelView™:

- Only 8/15/16 bpp modes are supported – 4 bpp mode is not supported.
- Hardware cursor and ink images are not rotated – software rotation must be used. SwivelView™ Enable bit 0 must be set to 0 when the user is accessing the Hardware Cursor or the Ink Layer buffer.
- 90° SwivelView™ does not support BitBLTs.

15.3 180° SwivelView™

180° SwivelView™ is accomplished by fetching the display buffer image in the reverse address direction, starting at the bottom-right corner of the image. Unlike 90° SwivelView™, the 180° SwivelView™ image is not rotated in the display buffer. The image is simply **displayed** 180° clockwise rotated. Furthermore, a virtual window is not required and all color depths (4/8/15/16 bpp) are supported.

15.3.1 Register Programming

Reverse Display Buffer Fetching Address Direction

Set SwivelView™ Enable bit 1 to 1. During screen refresh, the direction of the address for display buffer fetching is reversed. This setting does not affect CPU to display buffer access in any way. SwivelView™ Enable bit 0 should be set to 0.

Display Start Address

The Display Start Address must be programmed to be at the bottom-right corner of the image, since the display is now refreshed in the reverse direction. The LCD Display Start Address register (REG[042h], REG[043h], REG[044h]) must be set accordingly.

LCD Display Start Address (words)

$= (MA\_Offset \times H) - (MA\_Offset - W) - 1$ for 15/16 bpp mode
$= (MA\_Offset \times H) - (MA\_Offset - W/2) - 1$ for 8 bpp mode
$= (MA\_Offset \times H) - (MA\_Offset - W/4) - 1$ for 4 bpp mode

where H is the height of the panel in number of lines, W is the width of the panel in number of pixels, and MA_Offset is the LCD Memory Address Offset.

Horizontal Panning

Horizontal panning works in the same way as when SwivelView™ is not enabled, except that the effect of the LCD Pixel Panning register is reversed:

- Increment/decrement LCD Display Start Address register pans the display window to the right/left.
- Increment/decrement LCD Pixel Panning register pans the display window to the left/right.

Vertical Panning

Vertical panning works in the same way as when SwivelView™ is not enabled:

- Increase/decrease LCD Display Start Address register by one memory address offset scrolls the display window down/up by 1 line.

15.3.2 Limitations

The following limitations apply to 180° SwivelView™:

- Hardware Cursor and Ink Layer images are not rotated – software rotation must be used.
- CRT/TV mode is not supported.
- 180° SwivelView™ does not support all BitBLTs.

15.4 270° SwivelView™

270° SwivelView™ is a combination of 90° SwivelView™ and 180° SwivelView™. The image stored in the display buffer is 90° rotated, and the image is further 180° rotated during screen refresh, resulting in a 270° rotated display image. The user must use a 1024 × 1024 pixel virtual window as in 90° SwivelView™. See Figure 15-1: "Relationship Between Screen Image and 90° Rotated Image in the Display Buffer," on page 195.

15.4.1 Register Programming

Enabling 90° Rotation on CPU Read/Write to Display Buffer

Set SwivelView™ Enable bit 0 to 1. All CPU access to the display buffer is translated to provide 90° clockwise rotation of the display image.

Reverse Display Buffer Fetching Address Direction

Set SwivelView™ Enable bit 1 to 1. During screen refresh, the direction of the address for display buffer fetching is reversed. This setting does not affect CPU to display buffer access in any way.

Memory Address Offset

The LCD Memory Address Offset register (REG[046h], REG[047h]) must be set for a 1024 pixel offset.

LCD Memory Address Offset (words)

= 1024	for 15/16 bpp mode
= 512	for 8 bpp mode

Display Start Address

The Display Start Address must be programmed to be at the bottom-right corner of the image, since the display is now refreshed in the reverse direction. The LCD Display Start Address register (REG[042h], REG[043h], REG[044h]) must be set accordingly.

LCD Display Start Address (words)
$$= ((\text{LCD Memory Address Offset}) \times H) - 1$$

where H is the height of the panel in number of lines.

Horizontal Panning

Horizontal panning is achieved by changing the LCD Display Start Address register. It works in the same way as in 90° SwivelView™ mode:

- Increase/decrease LCD Display Start Address register by 1024 (15/16 bpp mode) or 512 (8 bpp mode) pans the display window to the right/left by 1 pixel.

The amount the display window can be panned to the right is limited to 1024 pixels and limited by the amount of physical memory installed.

Vertical Scrolling

Vertical scrolling is achieved by changing the LCD Display Start Address register and/or the LCD Pixel Panning register. It works in the same way as in 90° SwivelView™ mode, except that the effect of the LCD Pixel Panning register is reversed:

- Increment/decrement LCD Display Start Address register in 8 bpp mode scrolls the display window up/down by 2 lines.
- Increment/decrement LCD Display Start Address register in 15/16 bpp mode scrolls the display window up/down by 1 line.
- Increment/decrement LCD Pixel Panning register in 8 bpp mode scrolls the display window down/up by 1 line.

15.4.2 Physical Memory Requirement

270° SwivelView™ mode has the same physical memory requirement as in 90° SwivelView™ mode.

15.4.3 Limitations

The following limitations apply to 270° SwivelView™:

- Only 8/15/16 bpp modes are supported – 4 bpp mode is not supported.
- Hardware Cursor and Ink Layer images are not rotated – software rotation must be used. SwivelView™ Enable bit 0 must be set to 0 when the user is accessing the Hardware Cursor or the Ink Layer memory.
- CRT/TV mode is not supported. SwivelView™ Enable bit 0 must be set to 0 when the user is accessing the CRT/TV display buffer.
- 270° SwivelView™ does not support BitBLTs.

16 EPSON Independent Simultaneous Display (EISD)

16.1 Introduction

EPSON Independent Simultaneous Display (EISD) allows the S1D13506 to display independent images on two different displays (LCD panel and CRT or TV). The LCD panel timings and mode setup are programmed through the Panel Configuration Registers (REG[03Xh]) and the LCD Display Mode Registers (REG[04Xh]). The CRT/TV timings and mode setup are programmed through the CRT/TV Configuration Registers (REG[05Xh]) and the CRT/TV Display Mode Registers (REG[06Xh]). The Ink Layer or Hardware Cursor can also be independently controlled on the two displays. The LCD Ink/Cursor Registers (REG[07Xh]) control the Ink/Cursor on the LCD display; the CRT/TV Ink/Cursor Registers (REG[08Xh]) control the Ink/Cursor on the CRT or TV. Each display uses its own Look-Up Table (LUT), although there is only one set of LUT Registers (REG[1E0h], REG[1E2h], REG[1E4h]). Use the LUT Mode Register (REG[1E0h]) to select access to the LCD and/or CRT/TV LUTs.

The pixel clock source for the two displays may also be independent. Use the Clock Configuration Registers (REG[014h], REG[018h]) to select the LCD pixel clock source and the CRT/TV pixel clock source, respectively. Typically, CLKI2 is used for the CRT/TV display, while CLKI is used for the LCD display. Memory clock may come from CLKI or BUSCLK.

To display different images on the LCD and CRT/TV, the two images should reside in non-overlapping areas of the display buffer, and the display start addresses point to the corresponding areas. The display buffer is mapped to the CPU address AB[20:0] linearly.

Example 1: Assuming a 2M byte display buffer, the LCD image may locate in the first 1M byte of the display buffer (AB[20:0] = 000000h-0FFFFFh), and the CRT/TV image may locate in the second 1M byte of the display buffer (AB[20:0] = 100000h-1FFFFFh).

The LCD and CRT/TV may display identical images by setting the display start addresses for the LCD and the CRT/TV to the same address. In this case only one image is needed in the display buffer. However, the display pipelines are still independent so the same image is fetched twice from the display buffer; once for the LCD refresh and once for the CRT/TV refresh.

16.2 Bandwidth Limitation

When EISD is enabled, the LCD and CRT/TV displays must share the total bandwidth available to the S1D13506. The result is that display modes with a high resolution or color depth may not be supported. In some cases, Ink Layers may not be possible on one or both of the displays. EISD increases the total demand for display refresh bandwidth and reduces CPU bandwidth, resulting in lower CPU performance.

In a few cases when EISD is enabled, the default LCD and CRT/TV Display FIFO High Threshold Control register values are not optimally set, causing display problems with one or both of the displays. This condition may be corrected by adjusting the values of the LCD and CRT/TV Display FIFO High Threshold Control registers (REG[04Ah] for LCD and REG[06Ah] for CRT/TV).

When the FIFO High Threshold Control register is set to 00h (default), the following settings are used:

- 11h for 4 bpp mode
- 21h for 8 bpp mode
- 23h for 15/16 bpp mode

Changing this register to a non-zero value sets the high threshold FIFO level to this value. This register may not exceed 59 decimal. The high threshold FIFO level controls how often display fetch requests are issued by the FIFO. In general, a higher high threshold FIFO level increases the bandwidth to that display pipe, and a lower level reduces it.

Most display problems may be corrected by increasing the associated high threshold FIFO level for that display. However, because the total available bandwidth is fixed, this change may create display problem for the other display. In this case, reducing the high threshold FIFO level for the other display instead may work. Sometimes, a combination of these two methods is required. Correcting EISD display problems by adjusting the FIFO High Threshold Control registers is mostly a trial-and-error process. While the user is free to experiment with these registers, recommended FIFO level settings for some of the more common EISD modes requiring non-default FIFO level settings are listed in Section 18.2, “Example Frame Rates” on page 209.

17 MediaPlug Interface

Winnov's MediaPlug Slave interface has been incorporated into the S1D13506. The MediaPlug Slave follows the *Specification For Winnov MediaPlug Slave, Local module*, Document Rev 0.3 with the following exceptions.

17.1 Revision Code

The MediaPlug Slave Revision Code can be determined by reading bits 11:8 of the LCMD register. The revision code for this implementation is 0011b.

17.2 How to enable the MediaPlug Slave

The MediaPlug Slave interface uses the upper eight pins of the LCD data bus (FPDAT[15:8]) for the data bus, clock, and control lines. When pin MD13 is high at the rising edge of RESET#, FPDAT[15:8] are dedicated to the MediaPlug interface.

Table 17-1: MediaPlug Interface Pin Mapping

S1D13506 Pin Names	IO Type	MediaPlug I/F
FPDAT8	O	VMPLCTL
FPDAT9	I	VMPRCTL
FPDAT10	IO	VMPD0
FPDAT11	IO	VMPD1
FPDAT12	IO	VMPD2
FPDAT13	IO	VMPD3
FPDAT14	O	VMPCLK
FPDAT15	O	VMPCLKN
DRDY or MA11	O	VMPEPWR

Note
If MediaPlug is enabled, any 16-bit LCD panel must use an external circuit to support FPDAT[15:8].

Either pin MA11 or pin DRDY can be configured as the MediaPlug power control output, VMPEPWR. This is selected by the states of MD14, MD7, MD6 at the rising edge of RESET# - see Table 5-6:, “Summary of Power-On/Reset Options,” on page 31.

VMPEPWR is controlled by bit 1 of the MediaPlug LCMD register.

18 Clocking

18.1 Frame Rate Calculation

18.1.1 LCD Frame Rate Calculation

The maximum LCD frame rate is calculated using the following formula.

$$\text{max. LCD Frame Rate} = \frac{\text{LCD PCLK}_{max}}{(\text{LHDP} + \text{LHNDP}) \times \left(\frac{\text{LVDP}}{n} + \text{LVNDP}\right)}$$

Where:

LCD PCLKmax= maximum LCD pixel clock frequency

LVDP = LCD Vertical Display Height
= (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1

LVNDP = LCD Vertical Non-Display Period
= REG[03Ah] bits [5:0] + 1

LHDP = LCD Horizontal Display Width
= (REG[032h] bits [6:0] + 1) x 8Ts

LHNDP = LCD Horizontal Non-Display Period
= (REG[034h] bits [4:0] + 1) x 8Ts

Ts = minimum LCD pixel clock (LPCLK) period

n = 1 for single panel
= 2 for dual panel

18.1.2 CRT Frame Rate Calculation

The maximum CRT frame rate is calculated using the following formula.

$$\text{max. CRT Frame Rate} = \frac{\text{CRT PCLK}_{max}}{(\text{CHDP} + \text{CHNDP}) \times (\text{CVDP} + \text{CVNDP})}$$

Where:

CRT PCLKmax= maximum CRT pixel clock frequency

CVDP = CRT Vertical Display Height
= (REG[057h] bits [1:0], REG[056h] bits [7:0]) + 1

CVNDP = CRT Vertical Non-Display Period
= REG[058h] bits [6:0] + 1

CHDP = CRT Horizontal Display Width
= (REG[050h] bits [6:0] + 1) x 8Ts

CHNDP = CRT Horizontal Non-Display Period
= (REG[052h] bits [5:0] + 1) x 8Ts

Ts = minimum CRT pixel clock (CPCLK) period

18.1.3 TV Frame Rate Calculation

The maximum TV frame rate is calculated using the following formula.

$$\text{max. TV Frame Rate} = \frac{\text{TV PCLK}_{max}}{(\text{THDP} + \text{THNDP}) \times (\text{TVDP} + \text{TVNDP} + 0.5)}$$

Where:

TV PCLKmax= maximum TV pixel clock frequency

TVDP = TV Vertical Display Height
= (REG[057h] bits [1:0], REG[056h] bits [7:0]) + 1

TVNDP = TV Vertical Non-Display Period
= REG[058h] bits [6:0] + 1

THDP = TV Horizontal Display Width
= (REG[050h] bits [6:0] + 1) x 8Ts

THNDP = TV Horizontal Non-Display Period
= (REG[052h] bits [5:0] x 8Ts) + 6 for NTSC output
= (REG[052h] bits [5:0] x 8Ts) + 7 for PAL output

Ts = minimum TV pixel clock (TPCLK) period

18.2 Example Frame Rates

For all example frame rates the following conditions apply:

- Dual panel buffer is enabled for dual panel.
- TV flicker filter is enabled for TV.
- MCLK is 40MHz.

18.2.1 Frame Rates for 640x480 with EISD Disabled

Table 18-1: Frame Rates for 640x480 with EISD Disabled

LCD Type		Ink	Horiz Res (pixels)	Vert Res (lines)	bpp	max PCLK (MHz)	min HNDP (pixels)	min VNDP (lines)	max Frame Rate (Hz)	CRT/ TV	Ink	Horiz Res (pixels)	Vert Res (lines)	bpp	PCLK (MHz)	HNDP (pixels)	VNDP (lines)	Frame Rate (Hz)
Passive Single / TFT		No	640	480	4	40	56	1	119	--	--	--	--	--	--	--	--	--
		No	640	480	8	40	64	1	118	--	--	--	--	--	--	--	--	--
		No	640	480	16	34	56	1	101	--	--	--	--	--	--	--	--	--
Mono Passive Dual		No	640	480	4	40	64	1	235	--	--	--	--	--	--	--	--	--
		No	640	480	8	40	72	1	233	--	--	--	--	--	--	--	--	--
		No	640	480	16	27	56	1	161	--	--	--	--	--	--	--	--	--
Color Passive Dual		No	640	480	4	35	64	1	206	--	--	--	--	--	--	--	--	--
		No	640	480	8	33	64	1	194	--	--	--	--	--	--	--	--	--
		No	640	480	16	23	48	1	138	--	--	--	--	--	--	--	--	--
Passive Single / TFT		Yes	640	480	4	40	56	1	119	--	--	--	--	--	--	--	--	--
		Yes	640	480	8	40	64	1	118	--	--	--	--	--	--	--	--	--
		Yes	640	480	16	30	48	1	90	--	--	--	--	--	--	--	--	--
Mono Passive Dual		Yes	640	480	4	39	64	1	229	--	--	--	--	--	--	--	--	--
		Yes	640	480	8	31	56	1	184	--	--	--	--	--	--	--	--	--
		Yes	640	480	16	22	48	1	132	--	--	--	--	--	--	--	--	--
Color Passive Dual		Yes	640	480	4	31	56	1	184	--	--	--	--	--	--	--	--	--
		Yes	640	480	8	26	48	1	156	--	--	--	--	--	--	--	--	--
		Yes	640	480	16	20	40	1	122	--	--	--	--	--	--	--	--	--
--	--	--	--	--	--	--	--	--	--	--	CRT	No	640	480	4	36	192	29	85
--	--	--	--	--	--	--	--	--	--	--	CRT	No	640	480	8	36	192	29	85
--	--	--	--	--	--	--	--	--	--	--	CRT	No	640	480	16	36	192	29	85
--	--	--	--	--	--	--	--	--	--	--	NTSC TV	No	640	480	4	14.32	270	22	62
--	--	--	--	--	--	--	--	--	--	--	NTSC TV	No	640	480	8	14.32	270	22	62
--	--	--	--	--	--	--	--	--	--	--	NTSC TV	No	640	480	16	14.32	270	22	62
--	--	--	--	--	--	--	--	--	--	--	PAL TV	No	640	480	4	17.73	495	72	56
--	--	--	--	--	--	--	--	--	--	--	PAL TV	No	640	480	8	17.73	495	72	56
--	--	--	--	--	--	--	--	--	--	--	PAL TV	No	640	480	16	17.73	495	72	56

= Example Frame Rates with Ink Layer Enabled

Table 18-1: Frame Rates for 640x480 with EISD Disabled (Continued)

LCD Type		Ink	Horiz Res (pixels)	Vert Res (lines)	bpp	max PCLK (MHz)	min HNDP (pixels)	min VNDP (lines)	max Frame Rate (Hz)	CRT/ TV	Ink	Horiz Res (pixels)	Vert Res (lines)	bpp	PCLK (MHz)	HNDP (pixels)	VNDP (lines)	Frame Rate (Hz)
--	--	--	--	--	--	--	--	--	--	CRT	Yes	640	480	4	36	192	29	85
--	--	--	--	--	--	--	--	--	--	CRT	Yes	640	480	8	36	192	29	85
--	--	--	--	--	--	--	--	--	--	CRT	Yes	640	480	16	31.5	200	20	75
--	--	--	--	--	--	--	--	--	--	NTSC TV	Yes	640	480	4	14.32	270	22	62
--	--	--	--	--	--	--	--	--	--	NTSC TV	Yes	640	480	8	14.32	270	22	62
--	--	--	--	--	--	--	--	--	--	NTSC TV	Yes	640	480	16	14.32	270	22	62
--	--	--	--	--	--	--	--	--	--	PAL TV	Yes	640	480	4	17.73	495	72	56
--	--	--	--	--	--	--	--	--	--	PAL TV	Yes	640	480	8	17.73	495	72	56
--	--	--	--	--	--	--	--	--	--	PAL TV	Yes	640	480	16	17.73	495	72	56

= Example Frame Rates with Ink Layer Enabled

18.2.2 Frame Rates for 800x600 with EISD Disabled

Table 18-2: Frame Rates for 800x600 with EISD Disabled

LCD Type		Ink	Horiz Res (pixels)	Vert Res (lines)	bpp	max PCLK (MHz)	min HNDP (pixels)	min VNDP (lines)	max Frame Rate (Hz)	CRT/ TV	Ink	Horiz Res (pixels)	Vert Res (lines)	bpp	PCLK (MHz)	HNDP (pixels)	VNDP (lines)	Frame Rate (Hz)
Color Passive Dual		No	800	600	4	40	64	1	153	--	--	--	--	--	--	--	--	--
		No	800	600	8	33	64	1	126	--	--	--	--	--	--	--	--	--
		No	800	600	16	23	48	1	90	--	--	--	--	--	--	--	--	--
Color Passive Dual		Yes	800	600	4	31	56	1	120	--	--	--	--	--	--	--	--	--
		Yes	800	600	8	26	48	1	101	--	--	--	--	--	--	--	--	--
		Yes	800	600	16	20	40	1	79	--	--	--	--	--	--	--	--	--
--	--	--	--	--	--	--	--	--	--	CRT	No	800	600	4	40	256	28	60
--	--	--	--	--	--	--	--	--	--	CRT	No	800	600	8	40	256	28	60
--	--	--	--	--	--	--	--	--	--	CRT	No	800	600	16	36	224	25	56
--	--	--	--	--	--	--	--	--	--	CRT	Yes	800	600	4	40	256	28	60
--	--	--	--	--	--	--	--	--	--	CRT	Yes	800	600	8	40	256	28	60
--	--	--	--	--	--	--	--	--	--	CRT	Yes	800	600	16	31.5	224	25	49

= Example Frame Rates with Ink Layer Enabled

18.2.3 Frame Rates for LCD and CRT (640x480) with EISD Enabled

Table 18-3: Frame Rates for LCD and CRT (640x480) with EISD Enabled

LCD Type	Ink	Horiz Res (pixels)	Vert Res (lines)	bpp	max PCLK (MHz)	min HNDP (pixels)	min VNDP (lines)	max Frame Rate (Hz)	CRT/ TV	Ink	Horiz Res (pixels)	Vert Res (lines)	bpp	PCLK(MHz)	HNDP (pixels)	VNDP (lines)	Frame Rate (Hz)
Passive Single / TFT	No	320	240	16	9.7	40	1	111	CRT	No	640	480	16	25.175	160	44	60
	No	640	240	16	9.7	40	1	59	CRT	No	640	480	16	25.175	160	44	60
	No	640	480	4	40	112	1	110	CRT	No	640	480	4	25.175	160	44	60
	No	640	480	8	27	96	1	76	CRT	No	640	480	8	25.175	160	44	60
Color Passive Dual	No	640	480	8	18	72	1	104	CRT	No	640	480	8	25.175	160	44	60
TFT	No	800	600	8	27	96	1	50	CRT	No	640	480	8	25.175	160	44	60
Color Passive Dual	No	800	600	4	27	80	1	101	CRT	No	640	480	4	25.175	160	44	60
	No	800	600	8	18	72	1	68	CRT	No	640	480	8	25.175	160	44	60
Passive Single / TFT	Yes	640	480	4	32	88	1	91	CRT	No	640	480	4	25.175	160	44	60
	Yes	640	480	8	20	72	1	58	CRT	No	640	480	8	25.175	160	44	60
Mono Passive Dual	Yes	640	480	4	25	80	1	144	CRT	No	640	480	4	25.175	160	44	60
	Yes	640	480	8	17	64	1	100	CRT	No	640	480	8	25.175	160	44	60
Color Passive Dual	Yes	640	480	4	22	64	1	129	CRT	No	640	480	4	25.175	160	44	60
	Yes	640	480	8	15	56	1	89	CRT	No	640	480	8	25.175	160	44	60
	Yes	800	600	4	22	64	1	84	CRT	No	640	480	4	25.175	160	44	60
Passive Single / TFT	No	640	240	8	20	72	1	116	CRT	Yes	640	480	8	25.175	160	44	60
	No	640	480	4	32	88	1	91	CRT	Yes	640	480	4	25.175	160	44	60
	No	640	480	8	20	72	1	58	CRT	Yes	640	480	8	25.175	160	44	60
Mono Passive Dual	No	640	480	4	24	72	1	139	CRT	Yes	640	480	4	25.175	160	44	60
	No	640	480	8	16	64	1	94	CRT	Yes	640	480	8	25.175	160	44	60
Color Passive Dual	No	640	480	4	21	64	1	123	CRT	Yes	640	480	4	25.175	160	44	60
	No	640	480	8	14	56	1	83	CRT	Yes	640	480	8	25.175	160	44	60
	No	800	600	4	21	64	1	80	CRT	Yes	640	480	4	25.175	160	44	60
Passive Single / TFT	Yes	640	240	8	16	56	1	95	CRT	Yes	640	480	8	25.175	160	44	60
	Yes	640	480	4	24	64	1	70	CRT	Yes	640	480	4	25.175	160	44	60
Mono Passive Dual	Yes	640	480	4	20	64	1	117	CRT	Yes	640	480	4	25.175	160	44	60
	Yes	640	480	8	13	56	1	77	CRT	Yes	640	480	8	25.175	160	44	60
Color Passive Dual	Yes	640	480	4	17	56	1	101	CRT	Yes	640	480	4	25.175	160	44	60
	Yes	640	480	8	12	48	1	72	CRT	Yes	640	480	8	25.175	160	44	60
	Yes	800	600	4	17	56	1	66	CRT	Yes	640	480	4	25.175	160	44	60

= Example Frame Rates with Ink Layer Enabled

18.2.4 Frame Rates for LCD and CRT (800x600) with EISD Enabled

Table 18-4: Frame Rates for LCD and CRT (800x600) with EISD Enabled

LCD Type	Ink	Horiz Res (pixels)	Vert Res (lines)	bpp	max PCLK (MHz)	min HNDP (pixels)	min VNDP (lines)	max Frame Rate (Hz)	CRT/ TV	Ink	Horiz Res (pixels)	Vert Res (lines)	bpp	PCLK (MHz)	HNDP (pixels)	VNDP (lines)	Frame Rate (Hz)
Passive Single / TFT	No	640	240	8	20	72	1	116	CRT	No	800	600	8	40	256	28	60
	No	640	480	4	40	112	1	110	CRT	No	800	600	4	40	256	28	60
	No	640	480	8	20	72	1	58	CRT	No	800	600	8	40	256	28	60
Color Passive Dual [1]	No	640	480	8	13	56	1	77	CRT	No	800	600	8	40	256	28	60
Color Passive Dual	No	800	600	4	24	72	1	91	CRT	No	800	600	4	40	256	28	60
Color Passive Dual [2]	No	800	600	8	15	56	1	58	CRT	No	800	600	8	40	256	28	60
TFT[3]	No	800	600	8	30	72	28	54	CRT	No	800	600	8	40	256	28	60
Passive Single / TFT	Yes	640	240	8	15	56	1	89	CRT	No	800	600	8	40	256	28	60
	Yes	640	480	4	29	80	1	83	CRT	No	800	600	4	40	256	28	60
Mono Passive Dual	Yes	640	480	4	23	72	1	134	CRT	No	800	600	4	40	256	28	60
	Yes	640	480	8	11	56	1	65	CRT	No	800	600	8	40	256	28	60
Color Passive Dual	Yes	640	480	4	19	56	1	113	CRT	No	800	600	4	40	256	28	60
Passive Single / TFT	No	640	240	4	27	72	1	157	CRT	Yes	800	600	4	40	256	28	60
	No	640	240	8	13	48	1	78	CRT	Yes	800	600	8	40	256	28	60
	No	640	480	4	27	72	1	78	CRT	Yes	800	600	4	40	256	28	60
Mono Passive Dual	No	640	480	4	21	64	1	123	CRT	Yes	800	600	4	40	256	28	60
Color Passive Dual	No	640	480	4	17	56	1	101	CRT	Yes	800	600	4	40	256	28	60
	No	640	480	8	8.8	40	1	53	CRT	Yes	800	600	8	40	256	28	60
Passive Single / TFT	Yes	640	240	4	20	56	1	119	CRT	Yes	800	600	4	40	256	28	60
	Yes	640	480	4	20	56	1	59	CRT	Yes	800	600	4	40	256	28	60
Mono Passive Dual	Yes	640	480	4	17	56	1	101	CRT	Yes	800	600	4	40	256	28	60
Color Passive Dual	Yes	640	480	4	14	48	1	84	CRT	Yes	800	600	4	40	256	28	60

= Example Frame Rates with Ink Layer Enabled

The FIFO values for these display modes must be set as follows:

1. REG[04Ah] must be set to 1Ah.
2. REG[04Ah] must be set to Fh.
3. REG[04Ah], REG[06Ah] must be set to 30h. REG[04Bh], REG[06Bh] must be set to 32h.

18.2.5 Frame Rates for LCD and NTSC TV with EISD Enabled

Table 18-5: Frame Rates for LCD and NTSC TV with EISD Enabled

LCD Type	Ink	Horiz Res (pixels)	Vert Res (lines)	bpp	max PCLK (MHz)	min HNDP (pixels)	min VNDP (lines)	max Frame Rate (Hz)	CRT/ TV	Ink	Horiz Res (pixels)	Vert Res (lines)	bpp	PCLK (MHz)	HNDP (pixels)	VNDP (lines)	Frame Rate (Hz)
Passive Single / TFT	No	320	240	16	5.3	32	1	62	NTSC TV	No	640	480	16	14.32	270	22	62
	No	640	240	16	9	32	1	55	NTSC TV	No	640	480	16	14.32	270	22	62
	No	640	480	4	31	120	1	84	NTSC TV	No	640	480	4	14.32	270	22	62
	No	640	480	8	18	88	1	51	NTSC TV	No	640	480	8	14.32	270	22	62
Mono Passive Dual	No	640	480	4	25	104	1	139	NTSC TV	No	640	480	4	14.32	270	22	62
	No	640	480	8	15	80	1	86	NTSC TV	No	640	480	8	14.32	270	22	62
Color Passive Dual	No	640	480	4	21	88	1	119	NTSC TV	No	640	480	4	14.32	270	22	62
	No	640	480	8	13	72	1	75	NTSC TV	No	640	480	8	14.32	270	22	62
Color Passive Dual	No	800	600	8	13	72	1	49	NTSC TV	No	640	480	8	14.32	270	22	62
Passive Single / TFT	Yes	640	480	4	24	96	1	67	NTSC TV	No	640	480	4	14.32	270	22	62
Mono Passive Dual	Yes	640	480	4	20	80	1	115	NTSC TV	No	640	480	4	14.32	270	22	62
	Yes	640	480	8	12	64	1	70	NTSC TV	No	640	480	8	14.32	270	22	62
Color Passive Dual	Yes	640	480	4	17	72	1	99	NTSC TV	No	640	480	4	14.32	270	22	62
	Yes	640	480	8	11	64	1	64	NTSC TV	No	640	480	8	14.32	270	22	62
Passive Single / TFT	No	640	240	4	19	72	1	110	NTSC TV	Yes	640	480	4	14.32	270	22	62
	No	640	240	8	12	64	1	70	NTSC TV	Yes	640	480	8	14.32	270	22	62
	No	640	480	4	19	72	1	55	NTSC TV	Yes	640	480	4	14.32	270	22	62
Mono Passive Dual	No	640	480	4	16	64	1	94	NTSC TV	Yes	640	480	4	14.32	270	22	62
	No	640	480	8	10	56	1	59	NTSC TV	Yes	640	480	8	14.32	270	22	62
Color Passive Dual	No	640	480	4	14	56	1	83	NTSC TV	Yes	640	480	4	14.32	270	22	62
	No	640	480	8	9.3	48	1	56	NTSC TV	Yes	640	480	8	14.32	270	22	62
Passive Single / TFT	Yes	640	240	4	16	64	1	94	NTSC TV	Yes	640	480	4	14.32	270	22	62
	Yes	640	240	8	10	56	1	59	NTSC TV	Yes	640	480	8	14.32	270	22	62
Mono Passive Dual	Yes	640	480	4	14	56	1	83	NTSC TV	Yes	640	480	4	14.32	270	22	62
	Yes	640	480	8	9	48	1	54	NTSC TV	Yes	640	480	8	14.32	270	22	62
Color Passive Dual	Yes	640	480	4	12	48	1	72	NTSC TV	Yes	640	480	4	14.32	270	22	62

= Example Frame Rates with Ink Layer Enabled

18.2.6 Frame Rates for LCD and PAL TV with EISD Enabled

Table 18-6: Frame Rates for LCD and PAL TV with EISD Enabled

LCD Type	Ink	Horiz Res (pixels)	Vert Res (lines)	bpp	max PCLK (MHz)	min HNDP (pixels)	min VNDP (lines)	max Frame Rate (Hz)	CRT/ TV	Ink	Horiz Res (pixels)	Vert Res (lines)	bpp	PCLK (MHz)	HNDP (pixels)	VNDP (lines)	Frame Rate (Hz)
Passive Single / TFT	No	640	480	4	31	120	1	84	PAL TV	No	640	480	4	17.73	495	72	56
	No	640	480	8	18	88	1	51	PAL TV	No	640	480	8	17.73	495	72	56
Mono Passive Dual	No	640	480	4	25	104	1	139	PAL TV	No	640	480	4	17.73	495	72	56
	No	640	480	8	15	80	1	86	PAL TV	No	640	480	8	17.73	495	72	56
Color Passive Dual	No	640	480	4	21	88	1	119	PAL TV	No	640	480	4	17.73	495	72	56
	No	640	480	8	13	72	1	75	PAL TV	No	640	480	8	17.73	495	72	56
	No	800	600	8	16	72	1	60	PAL TV	No	640	480	8	17.73	495	72	56
TFT	No	800	600	8	23	88	1	43	PAL TV	No	640	480	8	17.73	495	72	56
Passive Single / TFT	Yes	640	480	4	24	96	1	67	PAL TV	No	640	480	4	17.73	495	72	56
Mono Passive Dual	Yes	640	480	4	20	80	1	115	PAL TV	No	640	480	4	17.73	495	72	56
	Yes	640	480	8	12	64	1	70	PAL TV	No	640	480	8	17.73	495	72	56
Color Passive Dual	Yes	640	480	4	17	72	1	99	PAL TV	No	640	480	4	17.73	495	72	56
	Yes	640	480	8	11	64	1	64	PAL TV	No	640	480	8	17.73	495	72	56
Passive Single / TFT	No	640	240	4	19	72	1	110	PAL TV	Yes	640	480	4	17.73	495	72	56
	No	640	240	8	12	64	1	70	PAL TV	Yes	640	480	8	17.73	495	72	56
	No	640	480	4	19	72	1	55	PAL TV	Yes	640	480	4	17.73	495	72	56
Mono Passive Dual	No	640	480	4	16	64	1	94	PAL TV	Yes	640	480	4	17.73	495	72	56
	No	640	480	8	10	56	1	59	PAL TV	Yes	640	480	8	17.73	495	72	56
Color Passive Dual	No	640	480	4	14	56	1	83	PAL TV	Yes	640	480	4	17.73	495	72	56
	No	640	480	8	9.3	48	1	56	PAL TV	Yes	640	480	8	17.73	495	72	56
Passive Single / TFT	Yes	640	240	4	16	64	1	94	PAL TV	Yes	640	480	4	17.73	495	72	56
	Yes	640	240	8	10	56	1	59	PAL TV	Yes	640	480	8	17.73	495	72	56
Mono Passive Dual	Yes	640	480	4	14	56	1	83	PAL TV	Yes	640	480	4	17.73	495	72	56
	Yes	640	480	8	9	48	1	54	PAL TV	Yes	640	480	8	17.73	495	72	56
Color Passive Dual	Yes	640	480	4	12	48	1	72	PAL TV	Yes	640	480	4	17.73	495	72	56

= Example Frame Rates with Ink Layer Enabled

19 Power Save Mode

The S1D13506 has been designed for very low-power applications. During normal operation, internal clock networks are dynamically disabled when not required. Similarly, the LCD and/or CRT/TV pipelines are shut down when not required in the selected display mode. Additionally, the S1D13506 has a software initiated power save mode.

19.1 Display Modes

The S1D13506 resets with both displays inactive, i.e. neither the LCD nor CRT/TV pipelines are active. The displays are independently enabled/disabled by REG[1FCh] bits 2-0: the CRT/TV is instantaneously enabled/disabled by these bits; the LCD is powered up/down according to the sequences in Section 7.4, “Power Sequencing” on page 70.

19.2 Power Save Mode

Power save mode is invoked by setting REG[1F0h] bit 0 to 1. In power save mode, both displays are disabled: the CRT/TV is instantaneously disabled; the LCD is powered down according to the sequences in Section 7.4, “Power Sequencing” on page 70. Access to memory is not allowed and the memory controller merely refreshes the memory in the method selected by REG[021h]. Register access is allowed.

19.3 Power Save Status Bits

LCD Power Save Status bit

The LCD Power Save Status bit (REG[1F1h] bit 0), when 1, indicates that the panel is powered down. When this bit is 0, the panel is powered up, or in transition of powering up or down. The system may disable the LCD pixel clock source when this bit is 1. This bit is 1 after chip reset.

Memory Controller Power Save Status bit

The Memory Controller Power Save Status bit (REG[1F1h] bit 1, when 1, indicates that the DRAM interface is powered down - the DRAM is either in self-refresh mode or completely idle. This condition occurs shortly after power save mode is invoked, provided Self-Refresh or No Refresh is pre-selected (see REG[021h] bits 7-6); this condition will never occur if CBR Refresh is selected. When this bit is 0, the DRAM interface is active. The system may disable the memory clock source when this bit is 1. This bit is 0 after chip reset.

19.4 Power Save Mode Summary

Table 19-1: Power Save Mode Summary

Function	LCD Disabled	CRT/TV Disabled	Power Save Mode Enabled
LCD Display Active?	no	--	No
CRT/TV Display Active?	--	no	No
Register Access Possible?	Yes	Yes	Yes
Memory Access Possible?	Yes	Yes	No
LCD LUT Access Possible?	Yes[1]	--	Yes
CRT/TV LUT Access Possible?	--	Yes[2]	Yes
LCD interface	Forced Low	--	Forced Low
CRT/TV interface	--	No Output Current	No Output Current
DRAM interface	Active	Active	Refresh Only[3]
Host Interface	Active	Active	Active

Note

1. LCD pixel clock required.
2. CRT/TV pixel clock required.
3. Selectable; may observe CBR refresh, self-refresh or no refresh at all.

20 Clocks

20.1 Clock Selection

The following diagram provides a logical representation of the S1D13506 internal clocks.

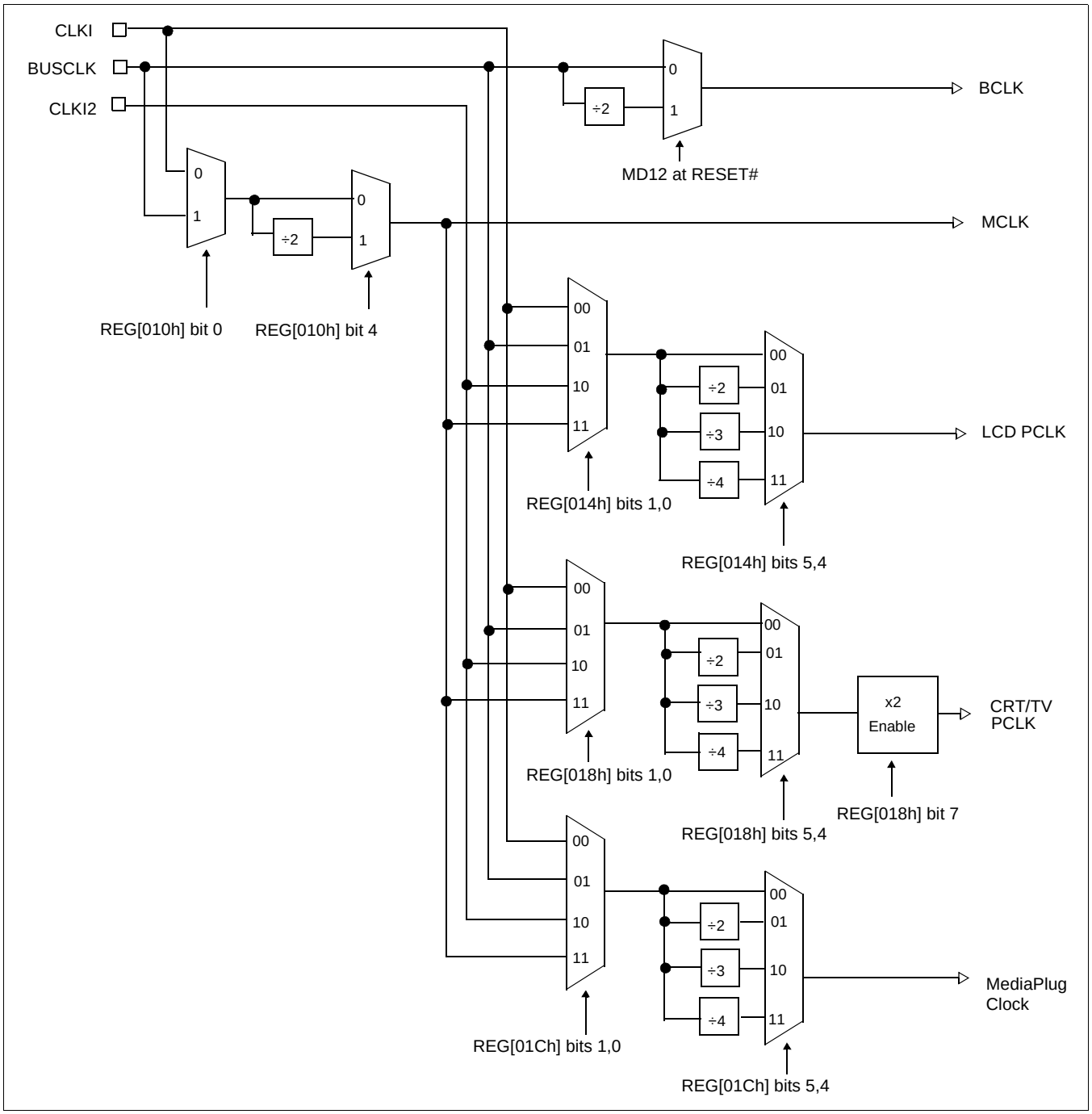

Figure 20-1: Clock Selection

20.2 Clock Descriptions

20.2.1 MCLK

MCLK should be configured as close to its maximum (40MHz) as possible. The S1D13506 contains sophisticated clock management, therefore, very little power is saved by reducing the MCLK frequency.

The frequency of MCLK is directly proportional to the bandwidth of the video memory. The bandwidth available to the CPU (for screen updates) is that left over after screen refresh takes its share. CPU bandwidth can be seriously reduced when the MCLK frequency is reduced, especially for high-resolution, high-color modes where screen refresh has high bandwidth requirements.

20.2.2 LCD PCLK

LCD PCLK should be chosen to match the optimum frame rate of the panel. See Section 18, “Clocking” on page 206 for details on the relationship between PCLK and frame rate, and for the maximum supportable PCLK frequencies for any given video mode.

Some flexibility is possible in the selection of PCLK. Panels typically have a range of permissible frame rates making it possible to choose a higher PCLK frequency and adjust the horizontal non-display period (see REG[052h]) to bring the frame-rate down to its optimal value.

20.2.3 CRT/TV PCLK

TVs and older CRTs usually have very precise frequency requirements, so it may be necessary to dedicate one of the clock inputs to this function. More recent CRTs work within a range of frequencies, so it may be possible to support them with BUSCLK or MCLK.

TV mode with flicker filter requires PCLK to be twice (2x) the standard NTSC (14.xxxMHz) and PAL (17.xxxMHz) clocks. A clock multiplier is used to create this clock, REG[018h] bit 7 is used to enable it. Note that the clock 2x clock could also be used for CRT support.

20.2.4 MediaPlug Clock

The MediaPlug Clock must be twice (2x) the frequency of VMPCLK. For timing see Section 7.7, “MediaPlug Interface Timing” on page 115. VMPCLK is typically in the range 6-8MHz so MediaPlug Clock must be in the range of 12-16MHz.

20.3 Clocks vs. Functions

The S1D13506 has five clock signals. Not all clock signals must be active for certain chip functions to be carried out. The following table shows which clocks are required for each chip function.

Table 20-1: Clocks vs. Functions

Function	Required Clocks				
	BUSCLK	**LCD PCLK**	**CRT/TV PCLK**	**MCLK**	**MediaPlug Clock**
Register read/write	Yes	No	No	No	No
LCD LUT read/write	Yes	Yes	--	--	--
CRT/TV LUT read/write	Yes	--	Yes	--	--
Memory read/write	Yes	--	--	Yes	--
2D Operation	Yes	--	--	Yes	--
MediaPlug Registers read/write	Yes	--	--	--	Yes
Power Save	--	--	--	--	--

Note

The S1D13506 contains sophisticated power management that dynamically shuts down clocks when not needed.

21 Mechanical Data

128-pin QFP15 surface mount package

Unit: mm

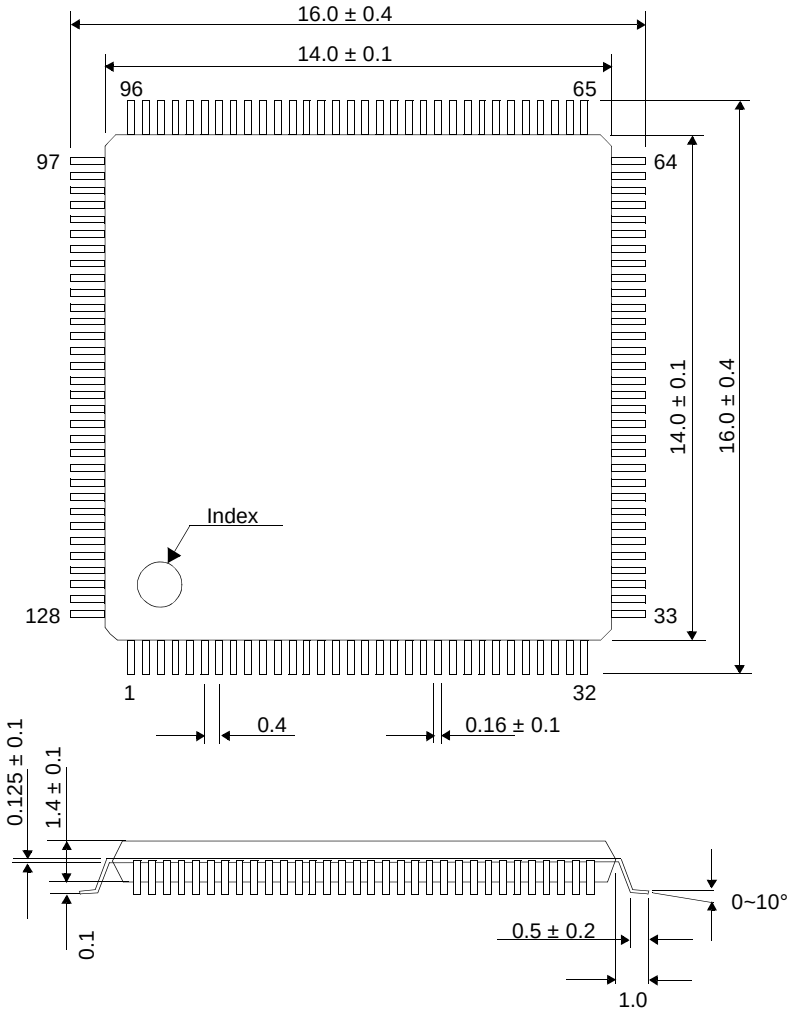

Figure 21-1: Mechanical Drawing QFP15

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22.1 Ordering Information

To order the S1D13506 Color LCD/CRT/TV Controller, contact the Epson sales representative in your area.

Change Record

X25B-A-001-12 Revision 12.2 - Issued: December 16, 2008

- changes from the previous revision are red
- release as revision 12.2 to align with Japan numbering
- section 23 - update Sales and Technical Support addresses

X25B-A-001-12 Revision 12.01 - Issued: September 19, 2007

- updated tagline and copyright
- REG[034h], fixed typo in REG[034h] minimum register value formula, should refer to REG[034h] instead of REG[032h]
- updated Sales and Technical Support addresses