Operating Guide

EPIA PD’s Digital I/O Function

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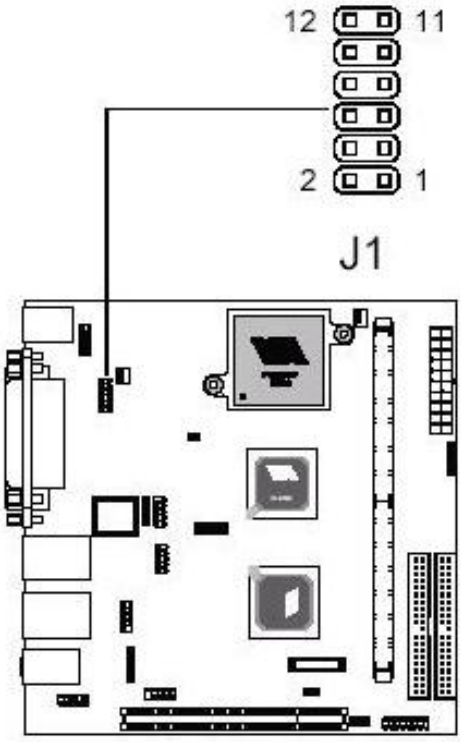
Digital I/O (J1: 4 GPI, 4 GPO) Introduction

Digital I/O Pin-header: J1

General purpose input and output for POS systems.

Pin	Signal	Pin	Signal
1	+5V	2	+12V
3	GPO5	4	GPI10
5	GPO6	6	GPI21
7	GPO7	8	GPI28
9	GPO12	10	GPI29
11	GND	12	GND



VT8235 GPI/O Control Porting Table

Signal Name	Pin No.	Signal Select Register	Signal Description
GPI10	D7	PMU_RXE4[3]	PMU_RXE4[3]=0:GPI10, GPI10 input value on PMIO_49[2]
GPI21	V1	PMU_RXE4[6] PMU_RXE5[2] PMIO_RX4E[5]	PMU_RXE4[6]=1 and PMU_RXE5[2]=0 and PMIO_RX4E[5]=1:GPI21 GPI21 input value on PMIO_4A[5]
GPI28	P25	PMU_RXE5[3] PMIO_RX4F[4]	PMU_RXE5[3]=1 and PMIO_RX4F[4]=1: GPI28 GPI28 input value on PMIO_4B[4]
GPI29	P24	PMU_RXE5[3] PMIO_RX4F[5]	PMU_RXE5[3]=1 and PMIO_RX4F[5]=1: GPI29 GPI29 input value on PMIO_4B[5]
GPO5	AC7	PMU_RXE4[0]	PMU_RXE4[0]=1:GPO5 output control on PMIO_4C[5]
GPO6	AF6	PMU_RXE4[1]	PMU_RXE4[1]=1:GPO6 output control on PMIO_4C[6]
GPO7	P4	PMU_RXE4[2]	PMU_RXE4[2]=0:GPO7 output control on PMIO_4C[7]
GPO12	A7	PMU_RXE4[4] ISA_RX53[7]	ISA_RX53[7]=0 and PMU_RXE4[4]=1:GPO12 GPO12 output control on PMIO_4D[4]

VT8235 Power Management I/O Base – Offset 8B-88

31 - 16 Reserved……always reads 0

15 - 7 Power Management I/O Register Base Address

Port Address for the base of the 128-byte Power Management I/O Register Block, corresponding to AD[15:7]. See "Power Management I/O Space Registers" in data sheet of VT8235 for definitions of the registers in the Power Management I/O Register Block.

6 - 0 0000001b

Digital Output Programming

Programming Construction:

Step1: Get PMIO Base Address

Step2: Enable GPI/GPO

Step3: Write GPO6 output

Program Example:

```
#define       VT8235      0x80008800
WORD wPmioBase;
/*************************************************************************/
/* inp(): IN data from I/O port by byte                                  */
/* inpd(): IN data from I/O port by double word                          */
/* outp(): OUT data to I/O port by byte                                  */
/* outpd(): OUT data to I/O port by double word                          */
/*************************************************************************/
/*************************************************************************/
/* GetPMIOBaseAddr                                                       */
/*************************************************************************/
GetPMIOBaseAddr()
{
 DWORD          pciAddr;
 /*
  * For (VT8235)
  * PMIO Base Address is located in PCI configuration space
  * Bus 0, device 17, function 0, offset 0x88
 */
 pciAddr    = VT8235 | 0x88;
 outpd(0x0CF8, pciAddr);
 wPmioBase = inpd(0x0CFC);
 wPmioBase &= 0xFFFE;
 printf("PMIO Base address = %x\n", wPmioBase);
} /* end GetPMIOBaseAddr */
/*************************************************************************
 * Enable and initialize GPO port (eg. Enable GPO 6)
 *************************************************************************/
GPOEnable()
```

```
{
  DWORD          pciAddr;
  DWORD          value;
  /*
    * For (VT8235)
    * GPO Control is located in PCI configuration space
    * Bus 0, device 17, function 0, offset 0xE4
  */
  pciAddr    = VT8235 | 0xE4;
  outpd(0x0CF8, pciAddr);
  value = inpd(0x0CFC);
  /*
    * eg. Enable GPO 6
    * GPO 6:    RxE4[1] = 1
  */
  value |= 0x00000002;                  /* set 1 to bit 1 */
  outpd(0x0CFC, value);
} /* end GPOEnable */
/*****************************************************************************
  * Put byte to GPO (eg. Pull high GPO 6)
  *****************************************************************************/
GPOSet()
{
  BYTE              data;
  /*
    * GPO 6 is in the offset 0x4C bit 6
  */
  data = inp(wPmioBase + 0x4C);
  data |= 0x40;
  /*
    * Out the value to the GPO io address
  */
  outp(wPmioBase + 0x4C, data);
} /* end GPOSet */
```