

➤ **Initial Program Code Example For 8051 MPU(8 Bit Interface):**

```

;-----
INITIAL_START:
    CALL DELAY40mS
    MOV  A,#38H          ;FUNCTION SET
    CALL WRINS_NOCHK    ;8 bit, N=1,5*7dot
    CALL DELAY30uS
    MOV  A,#38H          ;FUNCTION SET
    CALL WRINS_NOCHK    ;8 bit, N=1,5*7dot
    CALL DELAY30uS
    MOV  A,#14H          ;set bias
    CALL WRINS_CHK
    CALL DELAY30uS
    MOV  A,#78H          ;Contrast set adjustment
    CALL WRINS_CHK
    CALL DELAY30uS
    MOV  A,#5EH          ;Power/ICON/Contrast control
    CALL WRINS_CHK
    CALL DELAY30uS
    MOV  A,#6AH          ;Follower control
    CALL WRINS_CHK
    CALL DELAY30uS
    MOV  A,#0CH          ;DISPLAY ON
    CALL WRINS_CHK
    CALL DELAY30uS
    MOV  A,#01H          ;CLEAR DISPLAY
    CALL WRINS_CHK
    CALL DELAY2mS
    MOV  A,#06H          ;ENTRY MODE SET
    CALL WRINS_CHK      ;CURSOR MOVES TO RIGHT
    CALL DELAY30uS

```

```

;-----
MAIN_START:
    XXXX
    XXXX
    XXXX
    XXXX

```

```

;-----
WRINS_CHK:
    CALL CHK_BUSY
WRINS_NOCHK:
    CLR  RS              ;EX: Port 3.0
    CLR  RW              ;EX: Port 3.1
    SETB E               ;EX:Port 3.2
    MOV  P1,A            ;EX:Port 1=Data Bus
    CLR  E
    MOV  P1,#FFH        ;For Check Busy Flag
    RET

```

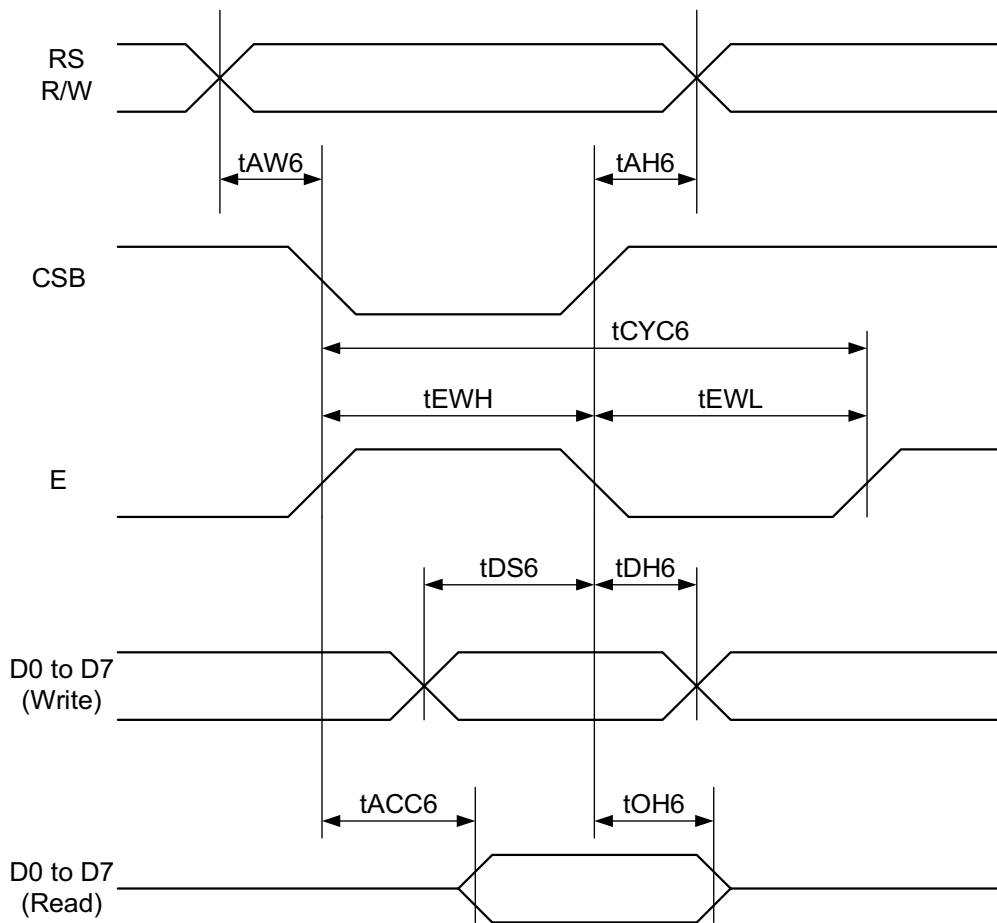
```

;-----
CHK_BUSY:
    CLR  RS              ;Check Busy Flag
    SETB RW
    SETB E
    JB   P1.7,$
    CLR  E
    RET

```

## AC Characteristics

### 68 Interface



( $T_a = 25^\circ\text{C}$ )

Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
				Min.	Max.	Min.	Max.	
Address hold time	RS	$t_{AH6}$	—	20	-	20	-	ns
Address setup time	RS	$t_{AW6}$		20	-	20	-	
System cycle time	RS	$t_{CYC6}$	—	400	-	280	-	ns
Data setup time	D0 to D7	$t_{DS6}$	—	100	-	80	-	ns
Data hold time	D0 to D7	$t_{DH6}$		40	-	20	-	
Access time	D0 to D7	$t_{ACC6}$	CL = 100 pF	-	500	-	400	ns
Output disable time	D0 to D7	$t_{OH6}$		300	-	150	-	
Enable H pulse time	E	$t_{EWH}$	—	200	-	120	-	ns
Enable L pulse time	E	$t_{EWL}$	—	150	-	130	-	ns

Note: All timing is specified using 20% and 80% of VDD as the reference.