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AllianceCORE™ Facts

Provided with Core	
Documentation	User Guide, Application note
Design File Formats	EDIF netlist
Constraints Files	.ucf and .pcf
Verification	Verilog Test Bench
Instantiation templates	Verilog Template file
Tools Used	
Simulation	Modelsim 5.8
Synthesis	Synplifypro 7.3
PAR	ISE6.2i
Support	
Support through email by HCL Technolgies	

Features

- Implements ANSI ATA/ATAPI-6 standard protocol
- Supports connection up to 2 ATA devices
- Configurable ATA interface operating with the Maximum data transfer rate of 100 MB/s
- Supports all PIO Modes 0,1,2,3,4
- Supports Multiword DMA modes 0,1,2
- Supports all Ultra DMA modes 0,1,2,3,4,5
- Supports SOC compatible PVCI interface to internal register map and PIO transfers
- PVCI interface support burst and back to back transfers.
- Supports FIFO interface for DMA transfers
- TWO Internal FIFOs of size 2K bytes (32-bit wide) for DATA IN and DATA OUT DMA operation.
- Level triggered interrupt to Host processor, combines internal as well as ATA Device specific interrupt.

Table 1: Resource Implemented Statistics

Family	Example Device	Fmax (MHz)	Slices[1]	IOB[2]	GCLK	BRAM	MULT	DCM/ DLL	MGT	PPC	Design Tools
Spartan-3™	XC3S400E-4	100	993	187	3	8	0	0	N/A	N/A	ISE 6.2i
Spartan-IIE™	XC2S300E-7	100	995	187	3	8	N/A	0	N/A	N/A	ISE 6.2i
Virtex-II Pro™	XC2VP7-5	100	947	187	3	8	0	0	0	0	ISE 6.2i
Virtex-II ™	XC2V250-4	100	947	187	3	8	0	0	N/A	N/A	ISE 6.2i

Notes:

1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details
2) Assuming not all core I/Os and clocks are routed off-chip
3) DCMs would be required to be instantiated as part of the complete clocking scheme taking into consideration the other IPs that are being integrated.

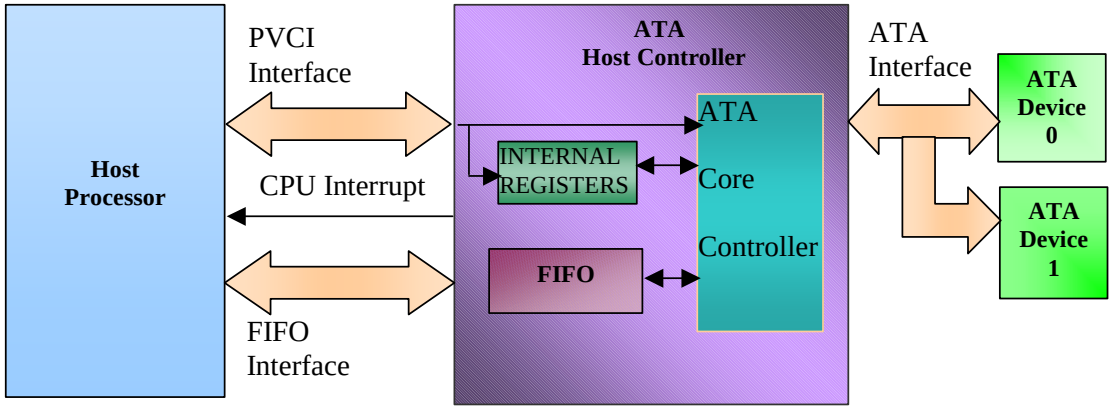

Figure 1 ATA host controller interface block diagram

Applications

ATA HOST controller provide an interface between a host processor and disk storage devices like Hard disc, CD-ROMs, CD-R, CD-RW, DVD, tape drives, some super-floppy drives (ZIP and LS-120) and changers that support ATA/ATAPI standards. The controller will be able to interface with general-purpose processors, micro controllers etc. that implement the software driver for the ATA/ATAPI storage device. The core can be thought of as an IP that can be easily integrated into FPGA based systems and provide a good solution for System on Chip (SOC) implementations.

The ATA host controller IP can be used as an interface between any host processor and ATA devices as shown in the figure 1. The major interfaces of this block are PVCI interface, FIFO interface and ATA interface. The PVCI and FIFO interface provides SOC based connectivity to the host processor and the ATA interface provide connectivity to a maximum of two ATA device.

General Description

The ATA Host controller provides an effective way of connecting the Host Processor with the Peripheral devices (ATA devices). The core implements the ANSI ATA/ATAPI-6 standard protocol. The Core provides an industry standard SOC bus namely PVCI to communicate with internal Register Mapping and the ATA Device Register. Also the core provides FIFO interface for the DMA data transfer. The core is designed in such a way that it can easily be used for the SOC development without much glue required. The Core supports all PIO, multiword and ultra DMA modes. The ATA modes can be easily selected through the configuration of internal registers.

Functional Description

The Figure 2 gives the skeletal view of ATA HOST controller. The PVCI controller controls the data transfer through PVCI bus to the ATA device and to the internal IP Core registers. FIFO interface of the core provides DMA data transfer from and to the DATA in and Data out FIFO. In DMA data in transfer, the Data in FIFO stores the data from ATA device, which is read by the host processor. In DMA data out transfer, the Data out FIFO stores the data from the host processor, which is written into ATA device. PIO controller generates ATA bus control signals for PIO data transfer (Read / Write), with respect to the mode selected. DMA controller controls the data and control signals for a DMA transfer with respect to the mode selected. CRC engine calculate the CRC for Ultra DMA transfer and send it to ATA Device at the end of transfer. ATA interface registers and enables the output signals to ATA Device.

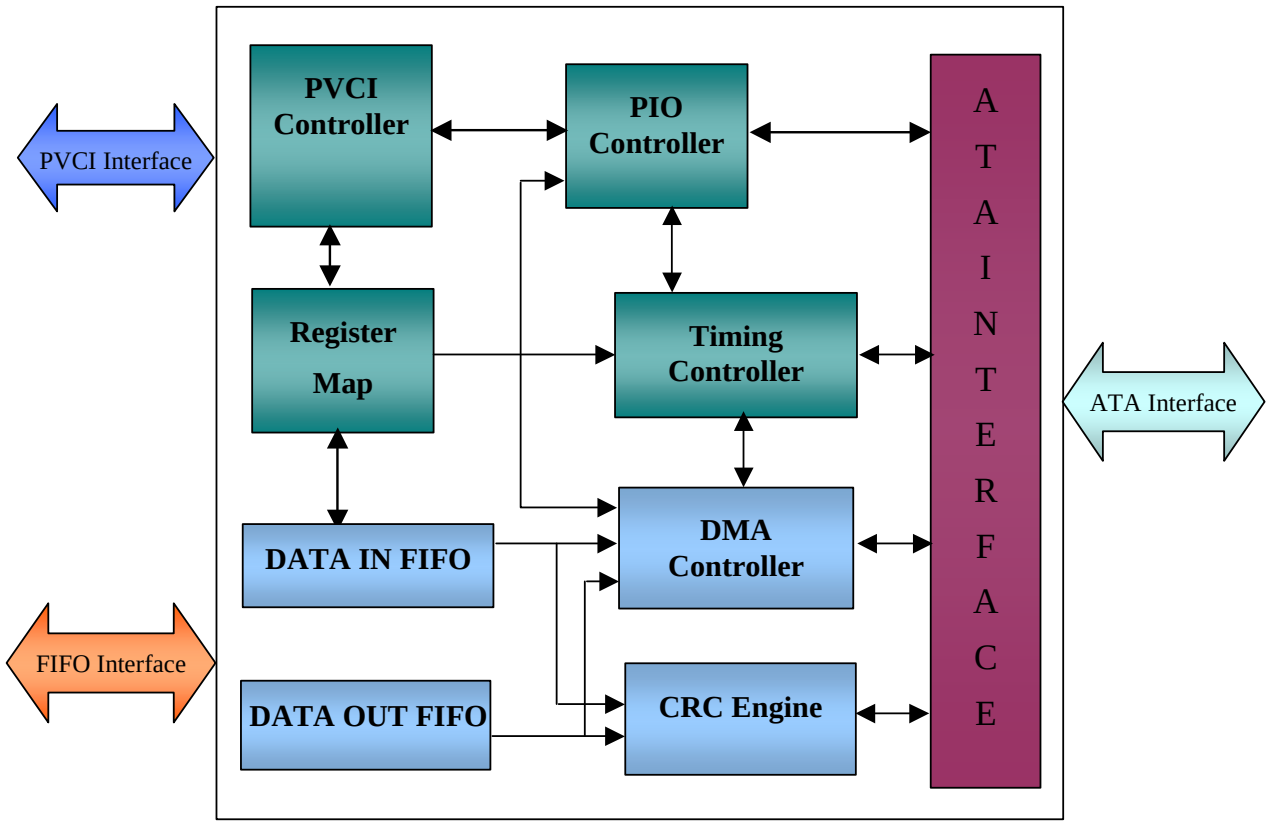

Figure 2 : ATA HOST Controller Block Diagram

PVCI controller

PVCI controller provides a target interface to the on chip PVCI bus. It performs handshake and generates response signals for PVCI bus. The host processor performs PIO Register/Data transfer to the ATA Device through PVCI bus. The PVCI controller Latch all command and data operation for PIO mode transfers to PIO controller. It also generate control signals to configure the internal registers MAP

Register Map

Register map is a set of registers used for configuration and status monitoring the ATA Host IP core. The ATA PIO, MDMA and UDMA mode selection, ATA device selection are selected by configuring the internal register.

Data in FIFO

Data in FIFO is an asynchronous first in first out memory queue data interface between host processor and DMA controller for ATA data in transfer in DMA mode. The DMA controller writes the data from ATA device to Data in FIFO through the ATA interface controller. The host processor reads data from the Data in FIFO.

Data out FIFO

Data out FIFO is an asynchronous first in first out memory queue data interface between host processor and DMA controller for ATA data out transfer in DMA mode. The host processor writes data to the Data out FIFO. The DMA controller reads the data from the Data out FIFO and transfers it to the ATA device through the ATA interface controller.

PIO Controller

The function of PIO controller is to control PIO read and write transfers to the ATA device. PIO controller is design to work in all modes (mode 0 to mode 4) of operation specified in ATAPI standard 6. It controls both Data and Register PIO transfers. Default mode on power up is mode 0. It supports IORDY based data transfer control.

DMA controller

The function of DMA controller block is to control Multiword and Ultra DMA transfers. DMA controller initiates, regulates and terminates DMA transaction in all modes specified in ATAPI-6 standard. It generate DMACK signal in response to external DMARQ signal from ATA Device and internal register settings.

Timing controller

Timing controller generate appropriate timing delays for PIO and DMA transfers. Delays are gnerated according to the timing values specified in ATAPI-6 standard. Delays generated, to control the ATA interface, are based on the mode selected and the device to which the transfer is targeted.

CRC engine

The function of the CRC engine is to calculate the CRC for Ultra DMA DATA IN and DATA OUT transfer and to buffer and control the DMA DATA transfer between FIFO and ATA interface. It also generates necessary control and status signals to ATA interface block, DMA block and FIFO block.

ATA Interface

ATA Interface block generates and receives ATA Bus signals, connecting IP Core and the ATA Devices. It registers and enables the output signals to ATA Device.

ATA host controller core I/O signals

Descriptions of all input and output signals related to ATA host controller are provided in Table 2.

Table 2: ATA host controller core I/O signals

Signal	Signal Direction	Description
Clock/Reset Interface		
ip_ata_reset_in_n	Input	Asynchronous active low IP Core hardware reset signal to ATA logic blocks.
ip_ata_clk_100_in	Input	IP core refernce clock to all internal ATA logic blocks . All ATA timing parameters are the derivatives of this clock. The clock frequency should be 100 MHZ.
ip_ata_clk_100_180p_in	Output	The clock input should be 180 degrees out of phase of the above ATA clock
fifo_clk_in	Input	Clock input to the write port of asynchronous Data out FIFO and read port of Data in FIFO of the IP core.
General processor interface signals		
ip_ata_dmarq_out	Output	DMA Request output from the IP core to the Host processor. Active HIGH signal. This signal is a bypassed signal of the DMARQ signal from ATA Device.
ip_doutfifo_sp_avail_out_n	Output	Active low assertion signal indicates the availability of free space (Equal to or higher than the threshold programmed in the IP core) in the Data out FIFO. The threshold value can be programmed in the register map.
ip_dinfifo_data_avail_out_n	Output	Active low assertion signal indicates the availability of quantity of data (Equal to or greater than the threshold) in the Data in FIFO. The threshold value can be programmed in the register map.
cpu_int_out_n	Output	Interrupt signal output to Host Processor from IP Core.

Signal	Signal Direction	Description
ATA Interface Signals		
ip_ata_cs_out_n [1:0]	Output	Chip select signal to the ATA device, used to select Command Block or Control Block Registers.
ip_ata_da_out [2:0]	Output	Device Address bits used by the host to access any register or data port in the ATA device.
ip_ata_dasp_in_n	Input	Asserted by the selected ATA device to show that device is active. During RESET protocol this signal is asserted by device 1 (Slave) to indicate its presence in the cable.
ip_ata_db_inout [15:0]	Inout	16-bit bi-directional data interface between the IP core and the device.
ip_ata_dmack_out_n	Output	DMA acknowledge, signal to respond the request from the ATA Device for a DMA transfer.
ip_ata_dmarq_in	Input	DMA request, asserted by the ATA device to indicate that it is ready for DMA transfer.
ip_ata_intrq_in	Input	Asserted by the selected ATA device to interrupt the host. Asynchronous Level Triggered signal.
ip_ata_dior_n_hrdy_n_hstb_out	Output	Read enable (DIOR-) for PIO Data/Register and Multiword DMA DATA IN transfer. (HDMARDY-) Host DMA ready Signal for Ultra DMA Data in transfers. (HSTROBE) Host strobe signal for ultra DMA data out transfers.
ip_ata_iordy_drdy_n_dstb_in	Input	(IORDY) input output ready signal for PIO Data/Register transfer. (DDMARDY-) ATA Device DMA ready signal for UDMA DATA OUT transfer. (DSTROBE) ATA Device strobe signal for UDMA DATA IN burst.
ip_ata_diow_n_stop_out	Output	(DIOW-) write enable signal for PIO Data/Register and Multiword DATA OUT DMA transfer. (STOP) stop signal for Ultra DMA transfer.
ip_ata_cblid_in_n	Input	Signal used to detect the presence of 80-conductor cable assembly at ATA device.
ip_ata_reset_out_n	Output	Hardware Reset, used by the host processor to reset the ATA devices. This signal is controlled through a RESET control register in REGMAP. Hardware reset is also asserted when external hardware reset is applied to the IP Core.
PVCI interface		
pvci_clock_in	Input	Synchronizes all PVCI transfers at the rising clock edge. The maximum clock frequency for this input is 100 MHz.
pvci_reset_in_n	Input	Active low asynchronous PVCI reset signal.
pvci_ack_out	Output	Active high signal acknowledge given by the IP Core to indicate that the 16 bit data can be transferred. .
pvci_val_in	Input	Valid signal indicates that the Host processor wishes to transfer a cell (i.e., 16 bits of data) to the ATA IP Core.
pvci_address_in [7:0]	Input	PVCI ADDRESS Bus to the IP core.
pvci_be_in [1:0]	Input	Byte enable. This is a field with 2 bits. one for each byte indicates which bytes of the cell (16 bit data) being transferred are enabled. Only 16 bit transfers are supported. Table shows the various data alignments defined for the PVCI data transfers. The entries labeled “XX” are “don’t cares” DATA Bus size / Transfer Size / pvci_be_in [1:0]|[0:1[/ W/R Data [15:8] / W/R Data [7:0] 16 / 16 / 00 / XX / XX 16 / 16 / 11 / Byte / Byte
pvci_rdata_out [15:0]	Output	PVCI Read Data bus from the IP core.

Signal	Signal Direction	Description
pvci_wdata_in [15:0]	Input	PVCI Write DATA bus to the IP core.
pvci_rd_wr_n_in	Input	Indicates PVCI read or write operation to the IP core. 1→ Read. 0 → Write.
pvci_eop_in	Input	Indicates a burst operation De-asserted by the Host processor to indicate that the transfer being performed will be followed with a transfer by the host processor to the next higher address. Low to High Indicates last transfer cell (16 bit data) in a transaction (i.e., in a burst).
pvci_error_out [2:0]	Output	Indicates error in transfer 000→Normal transfer (no error) XX0→Reserved 001→Reserved 011→Reserved 101→ Retry (Bus contention due to the DMA operation is in the ATA side) 111→ Abort (when time out given by the PIO controller for not generating the acknowledge signal)
FIFO interface signals		
dinfifo_rd_en_in	Input	Read Enable (request) to data in FIFO controller.
dinfifo_rd_ack_out	Output	Read Acknowledge handshake signal indicates that data was read from the data in FIFO and placed on the DOUT output pins on the previous FIFO clock edge while dinfifo_rd_en_in was active.
dinfifo_rd_err_out	Output	Read Error handshake signal indicates host processor that no data word was read from the data in FIFO on the previous FIFO clock edge while dinfifo_rd_en_in was active and subsequently data on Data output pins was not updated.
dinfifo_data_out [31:0]	Output	Data Output from the data in FIFO to host processor.
doutfifo_wr_en_in	Input	Write Enable (request) to data out FIFO controller.
doutfifo_wr_ack_ out	Output	Write Acknowledge handshake signal indicates that data was written to the data out FIFO on the previous CLK edge while doutfifo_wr_en_in was active.
doutfifo_wr_err_ out	Output	Write Error handshake signal indicates the host processor that no data word was written to the data out FIFO on the previous CLK edge while doutfifo_full_out was active.
doutfifo_data_in [31:0]	Input	Data input to data out FIFO from host processor.

Note :

An external reset circuit should be used for ATA reset and PVCI reset to assert asynchronously and de-assert synchronously with respect to their coresponding clock.

A external DCM or PLL should be used to output the ATA , PVCI and FIFO clock.

The ATA signal names that end with '–' are active low signal in the Description section.

IP Core Verification

The ATA HOST controller IP core has been verified by verilog test bench. The core was validated for all possible test cases and also included error test case. All necessary model were developed in verilog and random stimulus was generated to test the core under regression. The code is proved on a realized hardware using XC2S300EPQ208-7 device with an interface to a DSP processor and ATA hard disk.

Ordering Information

For more information about product details, please contact HCLT IP CORE SALES.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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