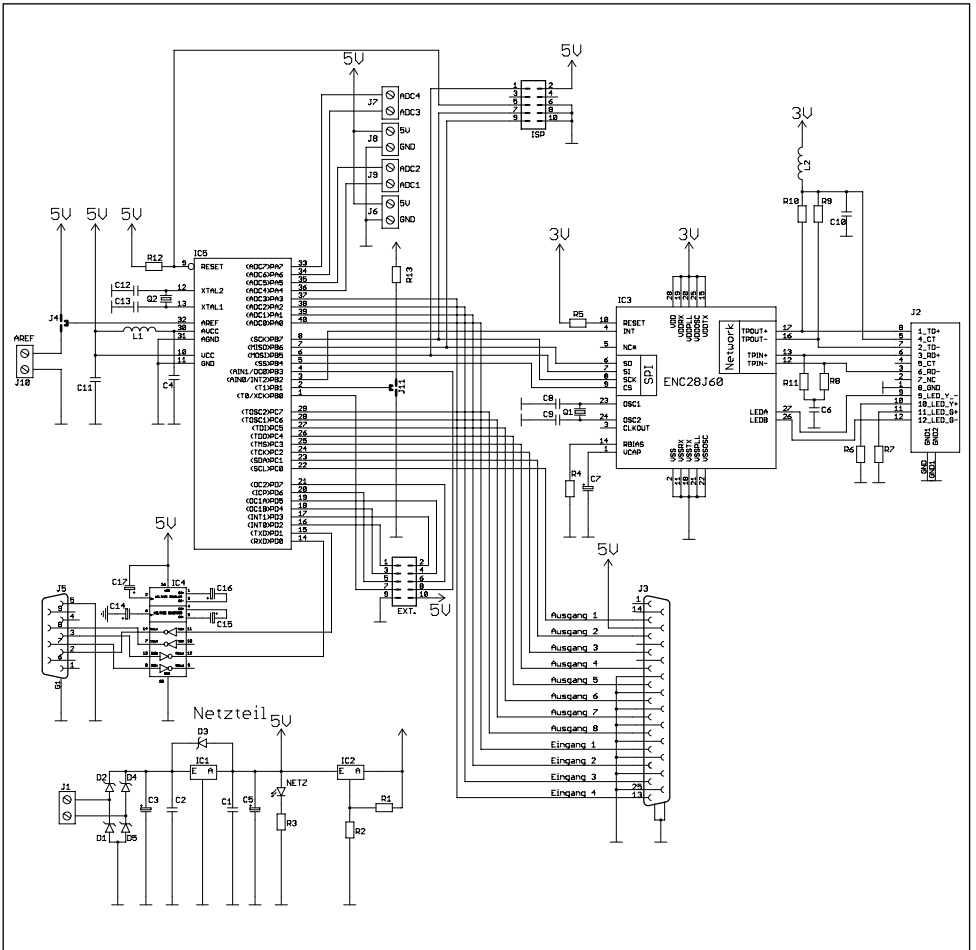




Schaltplan für das AVR-NET-IO-Board