Gain Selection

The AD621 has accurate, low temperature coefficient (TC), gains of 10 and 100 available. The gain of the AD621 is nominally set at 10; this is easily changed to a gain of 100 by simply connecting a jumper between Pins 1 and 8.

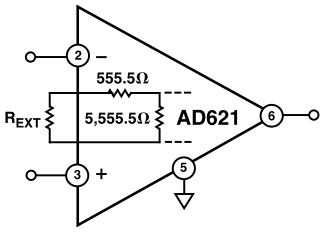

Figure 11. Programming the AD621 for Gains Between 10 and 100

As shown in Figure 11, the device can be programmed for any gain between 10 and 100 by connecting a single external resistor between Pins 1 and 8. Note that adding the external resistor will degrade both the gain accuracy and gain TC. Since the gain equation of the AD621 yields:

$$G = 1 + \frac{9\,(R_X + 6{,}111.111)}{(R_X + 555.555)}$$

This can be solved for the nominal value of external resistor for gains between 10 and 100:

$$R_X = \frac{(G-1)\,555.555 - 55{,}000}{(10 - G)}$$

Table III gives practical 1% resistor values for several common gains.

Table III. Practical 1% External Resistor Values for Gains Between 10 and 100

Desired Gain	Recommended 1% Resistor Value	Gain Error	Temperature Coefficient (TC)
10	∞ (Pins 1 and 8 Open)	*	5 ppm/°C max
20	4.42 kΩ	±10%	≈0.4 (50 ppm/°C + Resistor TC)
50	698 Ω	±10%	≈0.4 (50 ppm/°C + Resistor TC)
100	0 (Pins 1 and 8 Shorted)	*	5 ppm/°C max

*Factory trimmed–exact value depends on grade.

A High Performance Programmable Gain Amplifier

The excellent performance of the AD621 at a gain of 10 makes it a good choice to team up with the AD526 programmable gain amplifier (PGA) to yield a differential input PGA with gains of 10, 20, 40, 80, 160. As shown in Figure 12, the low offset of the AD621 allows total circuit offset to be trimmed using the offset null of the AD526, with only a negligible increase in total drift error. The total gain TC will be 9 ppm/°C max, with 2 µV/°C typical input offset drift. Bandwidth is 600 kHz to gains of 10 to 80, and 350 kHz at G = 160. Settling time is 13 µs to 0.01% for a 10 V output step for all gains.

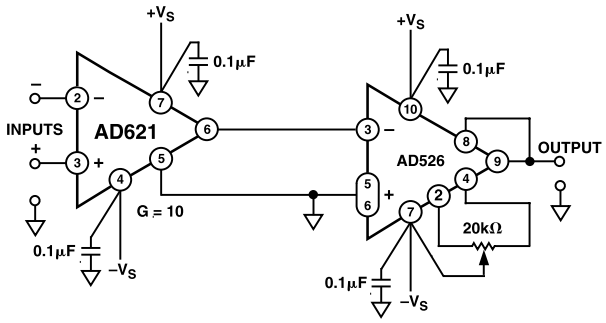

Figure 12. A High Performance Programmable Gain Amplifier

COMMON-MODE REJECTION

Instrumentation amplifiers like the AD621 offer high CMR which is a measure of the change in output voltage when both inputs arc changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

For optimal CMR, the reference terminal should be tied to a low impedance point, and differences in capacitance and resistance should be kept to a minimum between the two inputs. In many applications shielded cables are used to minimize noise, and for best CMR over frequency the shield should he properly driven. Figures 13 and 14 show active data guards that are configured to improve ac common-mode rejections by "bootstrapping" the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

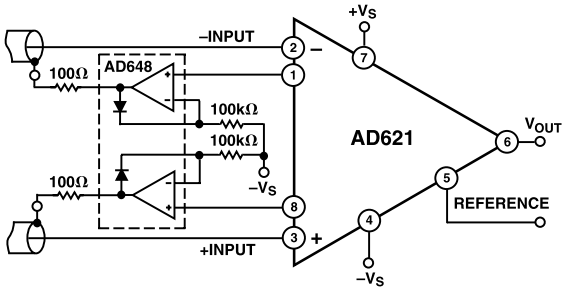

Figure 13. Differential Shield Driver, G = 10

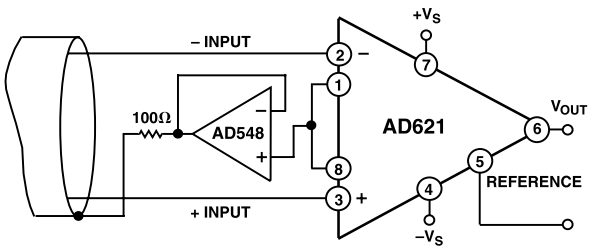

Figure 14. Common-Mode Shield Driver, G = 100