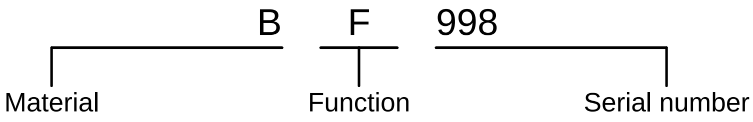
Conventions Used in Presenting Technical Data

Nomenclature for Semiconductor Devices According to Pro Electron

The part number of a semiconductor device consists of two letters followed by a serial number.

For example:



The **first letter** indicates the material used for the active part of the device.

A	GERMANIUM (Materials with a bandgap 0.6–1.0 eV) 1)
B	SILICON (Materials with a bandgap 1.0–1.3 eV) 1)
C	GALLIUM-ARSENIDE (Materials with a bandgap > 1.3 eV) 1)
R	COMPOUND MATERIALS (For example Cadmium-Sulphide)

The **second letter** indicates the circuit function.

A	DIODE: detection, switching or mixer
B	DIODE: variable capacitance
C	TRANSISTOR: low power, audio frequency
D	TRANSISTOR: power, audio frequency
E	DIODE: tunnel
F	TRANSISTOR: low power, high frequency
G	DIODE: oscillator and miscellaneous
H	DIODE: magnetic sensitive
K	HALL EFFECT DEVICE: in an open magnetic circuit
L	TRANSISTOR: power, high frequency
M	HALL EFFECT DEVICE: in a closed magnetic circuit
N	PHOTO COUPLER
P	DIODE: radiation sensitive
Q	DIODE: radiation generating
R	THYRISTOR: low power
S	TRANSISTOR: low power, switching
T	THYRISTOR: power
U	TRANSISTOR: power, switching
X	DIODE: multiplier, e.g., varactor, step recovery
Y	DIODE: rectifying, booster
Z	DIODE: voltage reference or voltage regulator transient suppressor diode

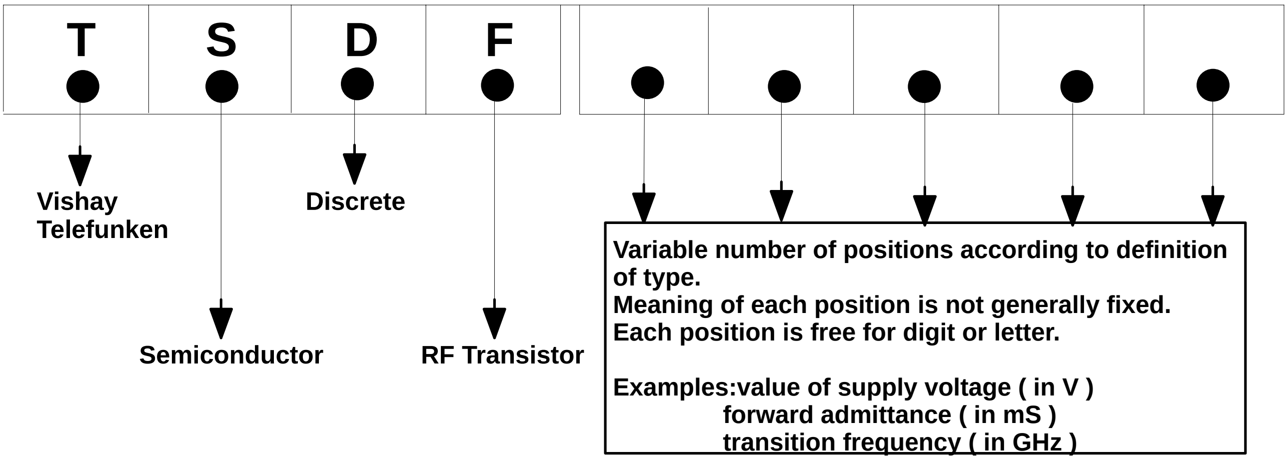
The **serial number** consists of:

- A four digit number from 100 to 9999 for devices primarily intended for consumer equipment.
- One letter (P, Q, R, etc.) and a three-digit number from 10 to 999 for devices primarily intended for professional equipment.

A version letter can be used to indicate a deviation of a single characteristic, either electrical or mechanical. This letter does not have a fixed meaning. The only exception is the use of the letter R, indicating reversed pinning or bending and W indicating SOT323 or SOT343 package.

1) The materials mentioned are examples

Most recent VISHAY Telefunken specific nomenclature for RF–Transistors



Variable number of positions according to definition of type.
Meaning of each position is not generally fixed.
Each position is free for digit or letter.

Examples: value of supply voltage (in V)
forward admittance (in mS)
transition frequency (in GHz)

Arrangement of Symbols

Letter symbols for current, voltage and power (according to DIN 41 785, sheet 1)

To represent current, voltage and power, a system of basic letter symbols are used. Capital letters are used for the representation of peak, mean, dc or root-mean-square values. Lower case letters are used for the representation of instantaneous values which vary with time.

Capital letters are used as subscripts to represent continuous or total values, while lower case letters are used to represent varying values.

The following table summarizes the rules given above.

Basic letter	
Upper-case	Upper-case
Instantaneous values which vary with time	Maximum (peak) average (mean) continuous (dc) or root-mean-square (RMS) values

Subscript(s)	
Upper-case	Upper-case
Varying component alone,i.e.,instantaneous, root-mean-square, maximum or average values	Continuous (without signal) or total (instantaneous, average or maximum) values

Letter symbols for impedance, admittances, two-port parameters etc.

For impedance, admittance, two-port parameters, etc., capital letters are used for the representation of external circuits of which the device is only a part. Lower case letters are used for the representation of electrical parameters inherent in the device.

The rules are not valid for inductance and capacitance. Both these quantities are denoted with capital letters.

Capital letters are used as subscripts for the designation of static (dc) values, while lower case letters are used for the designation of small-signal values.

If more than one subscript is used (h_{FE}, h_{fe}), the letter symbols are either all capital or all lower case.

If the subscript has numeric (single, double, etc.) as well as letter symbol(s) (such as h_{21E} or h_{21e}’), the differentiation between static and small-signal value is made only by a subscript letter symbol.

Other quantities (values) which deviate from the above rules are given in the list of letter symbols.

The following table summarizes the rules given above.

Basic letter	
Upper-case	Upper-case
Electrical parameters inherent in the semiconductor devices except inductances and capacitances	Electrical parameters of external circuits and of circuits in which the semiconductor device forms only a part; all inductances and capacitances

Subscript(s)	
Upper-case	Upper-case
Small-signal values	Static (dc) values

Examples:

G_P	Power gain
h_{FE}	DC forward current transfer ratio in common emitter configuration
Z_S	Source impedance
f_T	Transition frequency

List of Symbols for RF Transistors

AQL	Acceptable Quality Level
B,b	Base, base terminal
C	Capacitance, general
C,c	Collector, collector terminal
C_{ce}	Capacitance between collector and emitter, without parasitic capacitances
C_i	Short–circuit input capacitance
C_{ib}	Short–circuit input capacitance in common–base configuration
C_{ie}	Short–circuit input capacitance in common–emitter configuration
C_{issg1}	Gate 1–input capacitance in common–source configuration
C_{issg2}	Gate 2–input capacitance in common–source configuration
C_o	Short–circuit output capacitance
C_{ob}	Short–circuit output capacitance in common–base configuration
C_{oe}	Short–circuit output capacitance in common–emitter configuration
C_{oss}	Output capacitance in common–source configuration
C_{rss}	Feedback capacitance in common–emitter configuration
C_r	Short–circuit reverse transfer capacitance
C_{rb}	Feedback capacitance in common–base configuration
C_{re}	Feedback capacitance in common–emitter configuration
C_{cb}	Capacitance between collector and base without parasitic capacitances
C_{CBO}	Capacitance between collector and base with open emitter
C_{eb}	Capacitance between emitter and base without parasitic capacitances
C_{EBO}	Capacitance between emitter and base with an open collector
D	Drain
d_{iM}	Signal–to–intermodulation ratio
E,e	Emitter
E_{CB}	Collector base breakdown energy
E_L	Inductive energy
F, NF	Noise figure
f_{3dB}	3dB bandwidth
f_{IM}	Intermodulation frequency
f_{max}	Maximum frequency of oscillation
F_{opt}, NF_{opt}	Minimum noise figure
f_T	Transition frequency, gain bandwidth product
$F_{50\Omega}$, $NF_{50\Omega}$	Noise figure in 50Ω system
G,g	Gate
ΔG_p	Gain control range
g_i	Short–circuit input conductance
g_{ib}	Input conductance in common –base configuration, short circuit at output g_{ib}= Re (y_{ib})
g_{ie}	Input conductance in common –emitter configuration, short circuit at output g_{ie}= Re (y_{ie})
G_L	Load conductance
g_o	Short–circuit output conductance
g_{ob}	Output conductance in common –base configuration, short circuit at input g_{ob}= Re (y_{ob})
g_{oe}	Output conductance in common –base configuration, short circuit at input g_{ob}= Re (y_{oe})
g_r	Short–circuit reverse conductance
G_{pb}	Power gain in common–base configuration
G_{pe}	Power gain in common–emitter configuration
G_{ps}	Power gain in common–source configuration
G_S	Generator conductance
h_{FE}	DC forward current transfer ratio in common emitter configuration
h_{fe}	Short circuit forward current transfer ratio in common emitter configuration
I_B	DC base current
I_{bias}	Biasing current, device current
I_{BM}	Peak base current
I_C	DC collector current
I_{CBO}	Collector cut–off current with open emitter
I_{CEO}	Collector cut–off current with open base
I_{CER}	Collector cut–off current with a resistor R_{BE} connected between base and emitter

I_{CES}	Collector cut–off current, short between base and emitter
I_{CEV}	Collector cut–off current with reverse base–emitter voltage
I_{CEX}	Collector cut–off current with forward base–emitter voltage
I_{CM}	DC collector peak current
I_D	Drain current
I_{DSO}, I_{DSP}	Self–baised operating current
I_{DSS}	Drain–source saturation current
I_E	Emitter current
I_{EBO}	Emitter cut–off current with open collector
I_F	Forward current
I_{G1SS}	Gate1–source leakage current
I_{G2SS}	Gate2–source leakage current
IM_3	Intermodulation distortion third order
IP_3	Third order intercept point
I_{RM}	Reverse recovery current
K	Kelvin
L_s	Series inductance
m	Degree of modulation
M_A	Tightening torque
$P_{(-1dB)}$	Output power at 1dB gain compression
P_{in}	Input power
P_{out}	Output power
P_{tot}	Total power dissipation
r_{bb}	Basic intrinsic resistance
R_{BE}	Resistance connected between base and emitter
r_F	DC forward resistance
r_f	Differential forward resistance
R_{G1}	External resistor to gate1
R_{thChA}	Thermal resistance, channel ambient
R_{thJA}	Thermal resistance, junction and ambient
R_{thJC}	Thermal resistance, junction and case
s	Standing wave ratio (SWR)
S, s	Source
$\lvert S_{21}\rvert^2$	Transducer gain, power gain in 50Ω–system
S_{11}	Input reflection coefficient in 50Ω–system
S_{12}	Reverse transmission coefficient in 50Ω–system
S_{21}	Forward transmission coefficient in 50Ω–system
S_{22}	Output reflection coefficient in 50Ω–system
t	Time
t_d	Delay time
t_f	Fall time
t_{fr}	Forward recovery time
$\frac{t_p}{T}$	Duty cycle
t_{off}	Turn–off time
t_{on}	Turn–on time
t_p	Pulse duration (time)
t_r	Rise time
t_{rr}	Reverse recovery time
t_s	Storage time
T	Temperature, measured in centigrade
T	Absolute temperature in Kelvin
T	Period duration
T_{amb}	Ambient temperature (range)
T_{case}	Case temperature
Tch	Channel temperature
T_j	Junction temperature
TK	Temperature coefficient
T_{sd}	Soldering temperature
T_{stg}	Storage temperature (range)
V_{BB}	Base supply voltage
V_{BE}	Base–emitter voltage
V_{BEsat}	Base–saturation voltage
V_{CB}	Collector–base voltage
V_{CBO}	Collector–base voltage, open emitter
$V_{(BR)CBO}$	Breakdown voltage, collector–base, open emitter
V_{CC}	Collector supply voltage
V_{CE}	Collector–emitter voltage
V_{CEO}	Collector–emitter voltage, open base
$V_{(BR)CEO}$	Collector–emitter breakdown voltage, open base
V_{CER}	Collector–emitter voltage with a resistor R_{BE} connected between base and emitter
V_{CES}	Collector–emitter voltage, short between base and emitter

V_{CEsat}	Collector–emitter saturation voltage
$V_{CEsatdyn}$	Dynamic saturation voltage
V_{CEV}	Collector–emitter voltage with reverse base–emitter voltage
V_{CEW}	Collector–emitter working voltage
V_d	Device voltage
V_{DD}	Drain supply voltage
V_{DS}	Drain–source voltage
$V_{(BR)DS}$	Drain–source breakdown voltage
V_{EBO}	Emitter–base voltage with open collector
$V_{(BR)EBO}$	Emitter–base, breakdown voltage, open collector
$V_{(BR)ECO}$	Emitter–collector, breakdown voltage, open base
$\pm V_{(BR)G1SS}$	Gate 1–source breakdown voltage
$\pm V_{(BR)G2SS}$	Gate 2–source breakdown voltage
V_F	Forward voltage
V_{FP}	Turn on transient peak voltage
$V_{G1S(OFF)}$	Gate 1–source cut–off voltage
$V_{G2S(OFF)}$	Gate 2–source cut–off voltage
V_{GG}	Gate supply voltage
VSWR	Voltage standing wave ratio
y_{ib}	Short –circuit input admittance in common–base configuration (small–signal value)
y_{ie}	Short –circuit input admittance in common–emitter configuration (small–signal value)
y_r	Short –circuit reverse transfer admittance
$\|y_{re}\|$	Short–circuit reverse transfer admittance in common–emitter configuration (small signal value)
y_f	Short –circuit forward transfer admittance
$\|y_{fb}\|$	Short–circuit forward transfer admittance in common –base configuration (small signal value)
$\|y_{fs}\|$	Short–circuit forward admittance in a source configuration at a given operating point and frequency
$\|y_{21s}\|$	Short–circuit forward admittance in a source configuration at a given operating point and frequency
y_o	Short–circuit output admittance
y_{ob}	Short–circuit output admittance in common–base configuration (small–signal value)
y_{oe}	Short–circuit output admittance in common–emitter configuration (small–signal value)
$\|y_r\|$	Moduls of the short–circuit reverse transfer admittance
φ_r	Phase of the short–circuit reverse transfer admittance
$\|y_f\|$	Moduls of the short–circuit forward transfer admittance
φ_f	Phase of the short–circuit forward transfer admittance
φ	Phase angle
φ_{fb}	Phase of the short–circuit forward transfer admittance
φ_{fe}	Phase of the short–circuit forward transfer admittance y_{fe}
φ_{rb}	Phase of the short–circuit reverse transfer admittance y_{rb}
φ_{re}	Phase of the short–circuit reverse transfer admittance y_{re}
Z_0	System impedance
Z_L	Load impedance
Z_S	Source impedance

List of Symbols for Diodes

A	Anode
a	Distance (in mm)
b_{pn}	Normalized power factor
C	Capacitance, general
C_{case}	Case capacitance
C_D	Diode capacitance
C_i	Junction capacitance
C_L	Load capacitance
C_P	Parallel capacitance
F	Noise figure
f	Frequency
f_g	Cut-off-frequency
g	Conductance
I_F	Forward current
i_F	Forward current, instantaneous total value
I_{FAV}	Average forward current, rectified current
I_{FRM}	Repetitive peak forward current
I_{FSM}	Surge forward current, non-repetitive
I_{FWM}	Crest working forward current
I_R	Reverse current
i_R	Reverse current, instantaneous total value
I_{RAV}	Average reverse current
I_{RRM}	Repetitive peak reverse current
I_{RSM}	Non-repetitive peak reverse current
I_{RWM}	Crest working reverse current
I_S	Supply current
I_Z	Z-operating current
I_{ZM}	Z-maximum current
l	Length (in mm), (case-holder/soldering point)

LOCEP (local epitaxy)
A registrated trade mark of TEMIC for a process of epitaxial deposition on silicon. Applications occur in planer Z-diodes. It has an advantage compared to the normal process, with improved reverse current.

P	Power
P_{tot}	Total power dissipation
P_V	Power dissipation, general
P_{vp}	Pulse-power dissipation
Q	Quality
Q_{rr}	Reverse recovery charge
R_F	Forward resistance
r_f	Differential forward resistance
R_L	Load resistor
r_P	Parallel resistance, damping resistance
R_R	Reverse resistance
r_r	Differential reverse resistance
r_s	Series resistance
R_{thJA}	Thermal resistance between junction and ambient
R_{thJC}	Thermal reistance between junction and case
r_z	Differential Z-resistance in breakdown region (range) $r_z = r_{zj} + r_{zth}$
r_{zj}	Z-resistance at constant junction temperature, inherent Z-resistance
r_{zth}	Thermal part of the Z-resistance
T	Temperature, measured in centigrade
T	Absolute temperature, Kelvin temperature
T	Period duration
T_{amb}	Ambient temperature (range)
t_{av}	Integration time
T_{case}	Case temperature
t_{fr}	Forward recovery time
T_j	Junction temperature
TK	Temperature coefficient
T_L	Connecting lead temperature in the holder (soldering point) at the distance/(mm) from case
t_P	Pulse duration (time)
$\frac{t_p}{T}$	Duty cycle
t_r	Rise time
t_{rr}	Reverse recovery time
t_s	Storage time
T_{sd}	Soldering temperature
T_{stg}	Storage temperature (range)
$V_{(BR)}$	Breakdown voltage
V_F	Forward voltage
V_F	Forward voltage, instantaneous total value

V_{FAV}	Average forward voltage
V_o	Rectified voltage
V_{FSM}	Surge forward voltage, non-repetitive
V_{FRM}	Repetitive peak forward voltage
V_{FWM}	Crest working forward voltage
V_{HF}	RF voltage, RMS value
V_{HF}	RF voltage, peak value
V_R	Reverse voltage
V_R	Reverse voltage, instantaneous total value
V_{RSM}	Surge reverse voltage, non-repetitive

V_{RRM}	Repetitive peak reverse voltage
V_{RWM}	Crest working reverse voltage
V_S	Supply voltage
V_T	Temperature voltage
V_Z	Z-operating voltage
Z_{thp}	Thermal resistance – pulse operation
φ	Angle of current flow
η_r	Rectification efficiency
T_o	Time constant
ΔC_D	Capacitance deviation