teXet

TF-127

SERVICE MANUAL

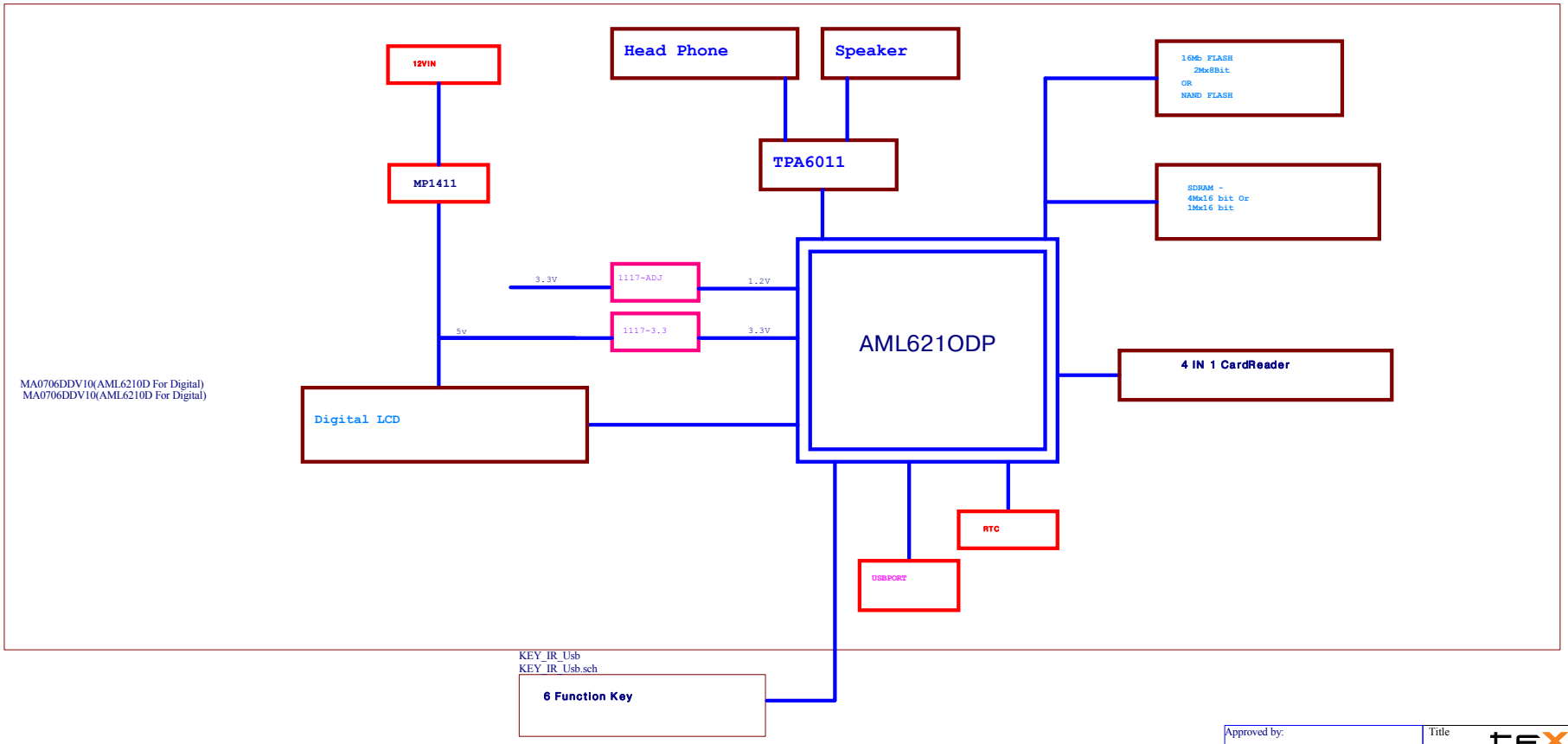
Premier confidential

Revision Table

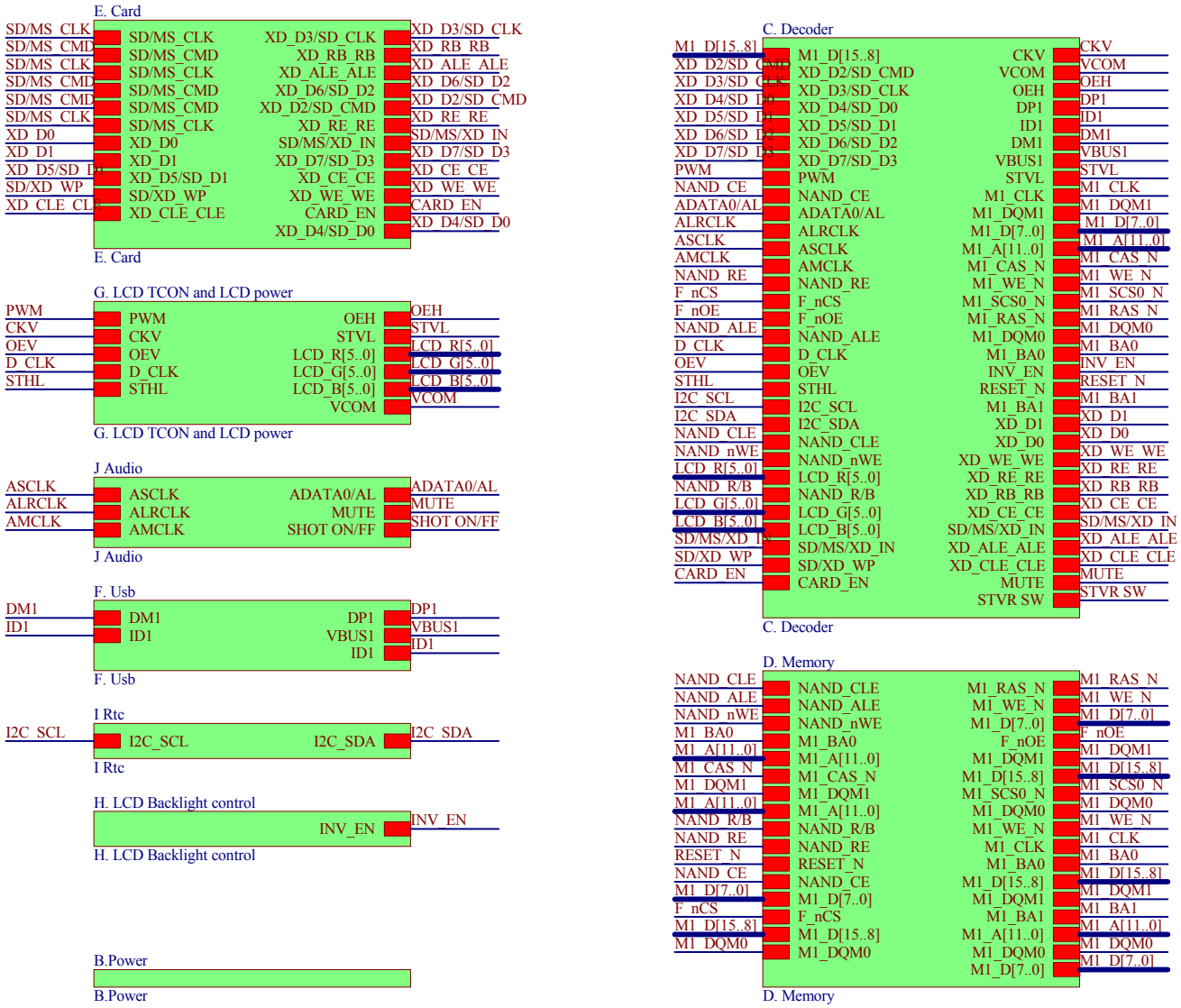
No.	Revision Date	REV	REVISION HISTORY
1	2009/06/01	1.1	Initial revision

Feature table

Main Chip:	AMLOGIC AML6210DP
Internal:	128MB SDRAM + 2MB NOR FLASH/256Mb Nand FLASH
Panel:	7" Analog TFT-LCD panels
Interfaces:	4-in-1 card-reader (MS/SDHC/MMC/XD) USB 2.0 Host Port 6 buttons



Approved by:	Title	teXet
Checked by:	Size: A3	Number: TF-127 Top Level Block Diagram.sch
	Revision: Ver01	
	Date: 10-Jun-2009	Sheet of 1 of 12



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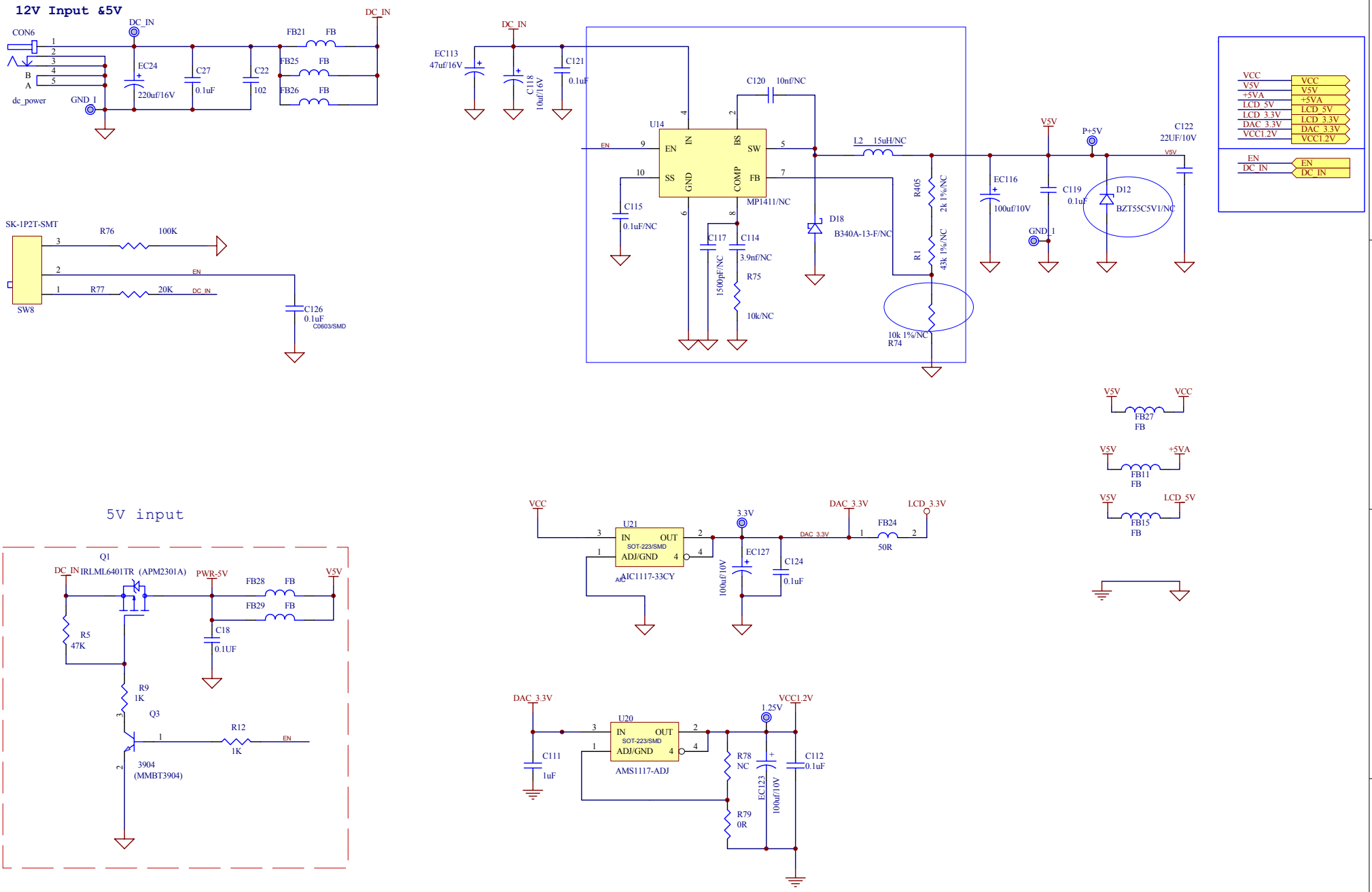
Checked by:	Size: B	Number: TF-127	Revision: Ver01
	Date: 10-Jun-2009	Sheet of 2 of 12	



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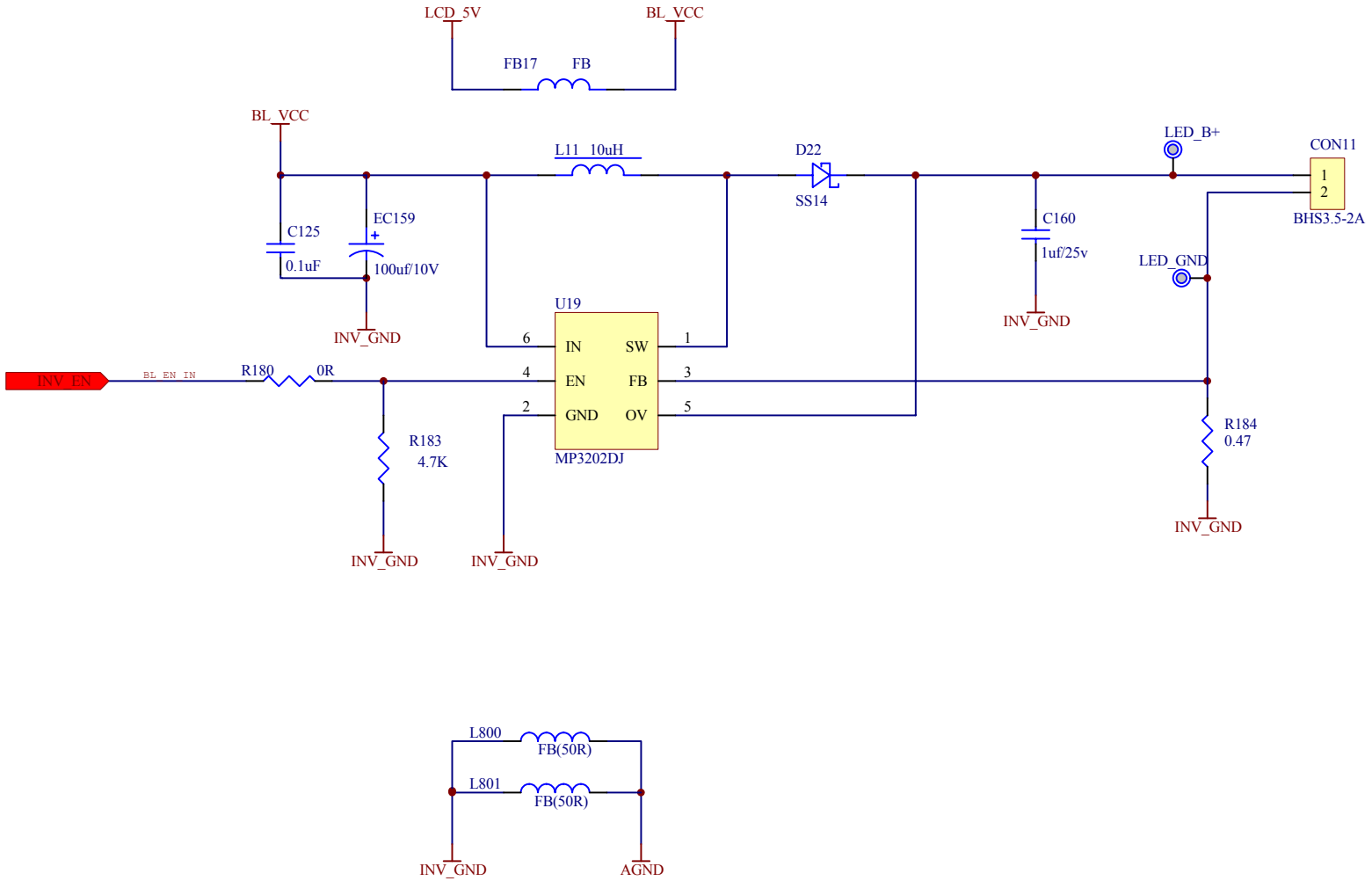
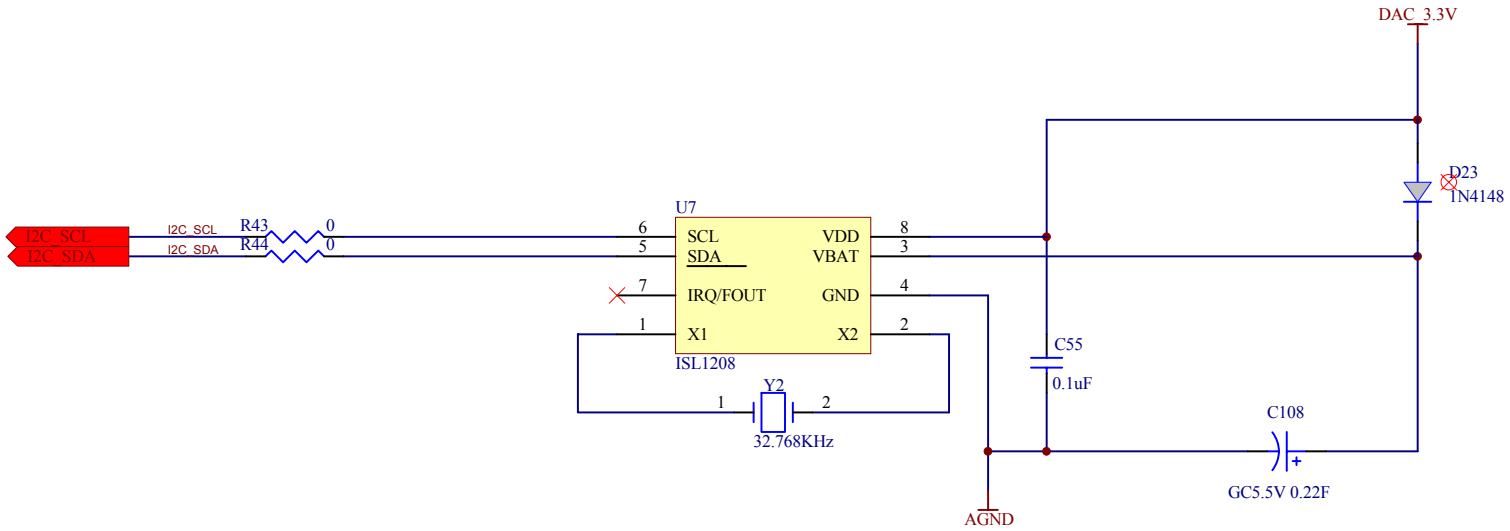
	Date: 10-Jun-2009	Sheet of 3 of 12	



BackLight

Approved by:	Title: texet	
Checked by:	Size: A4	Number: TF-127 H. LCD Backlight control — Revision: Ver01
	Date: 10-Jun-2009	Sheet of 9 of 12



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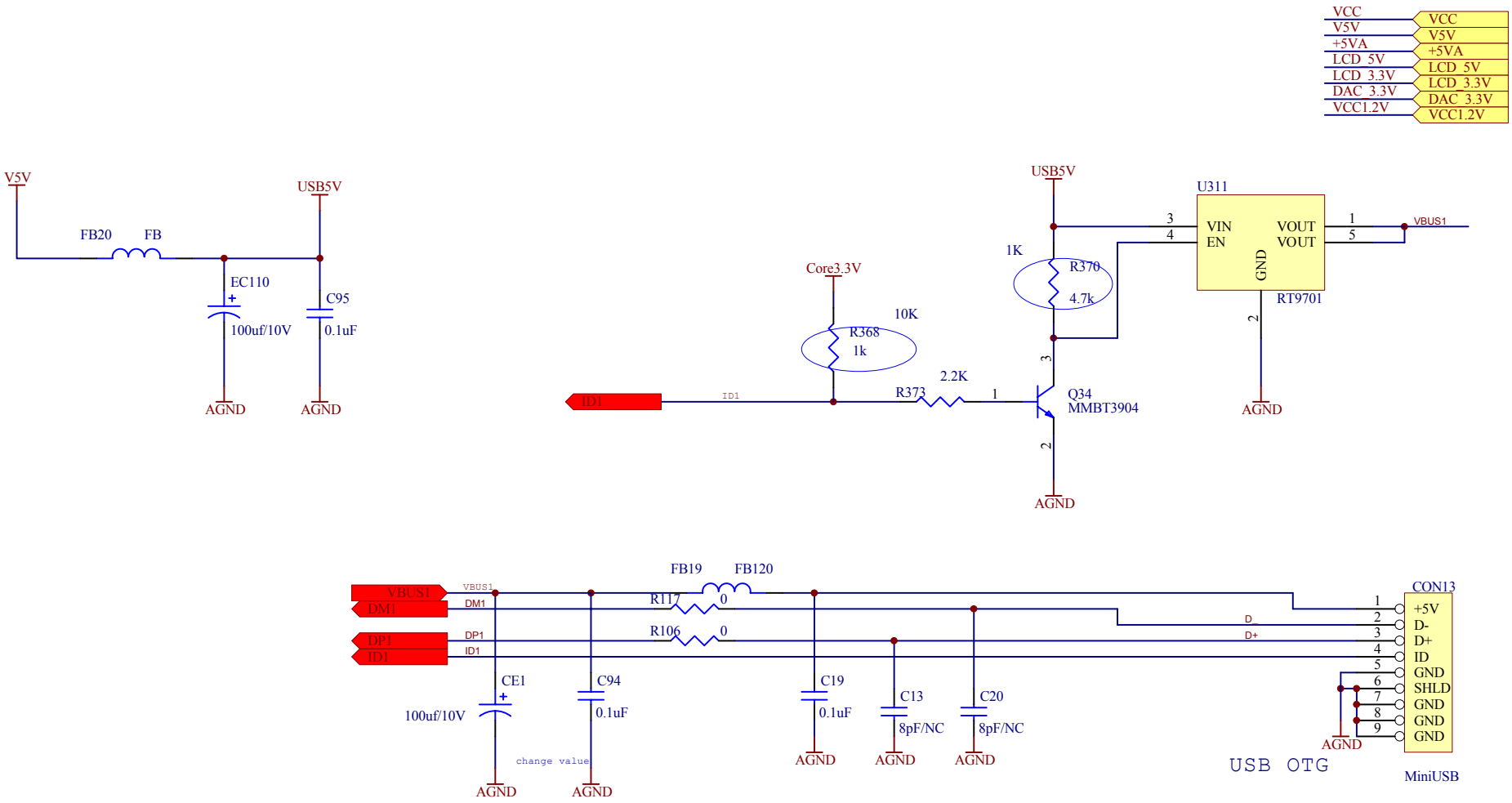
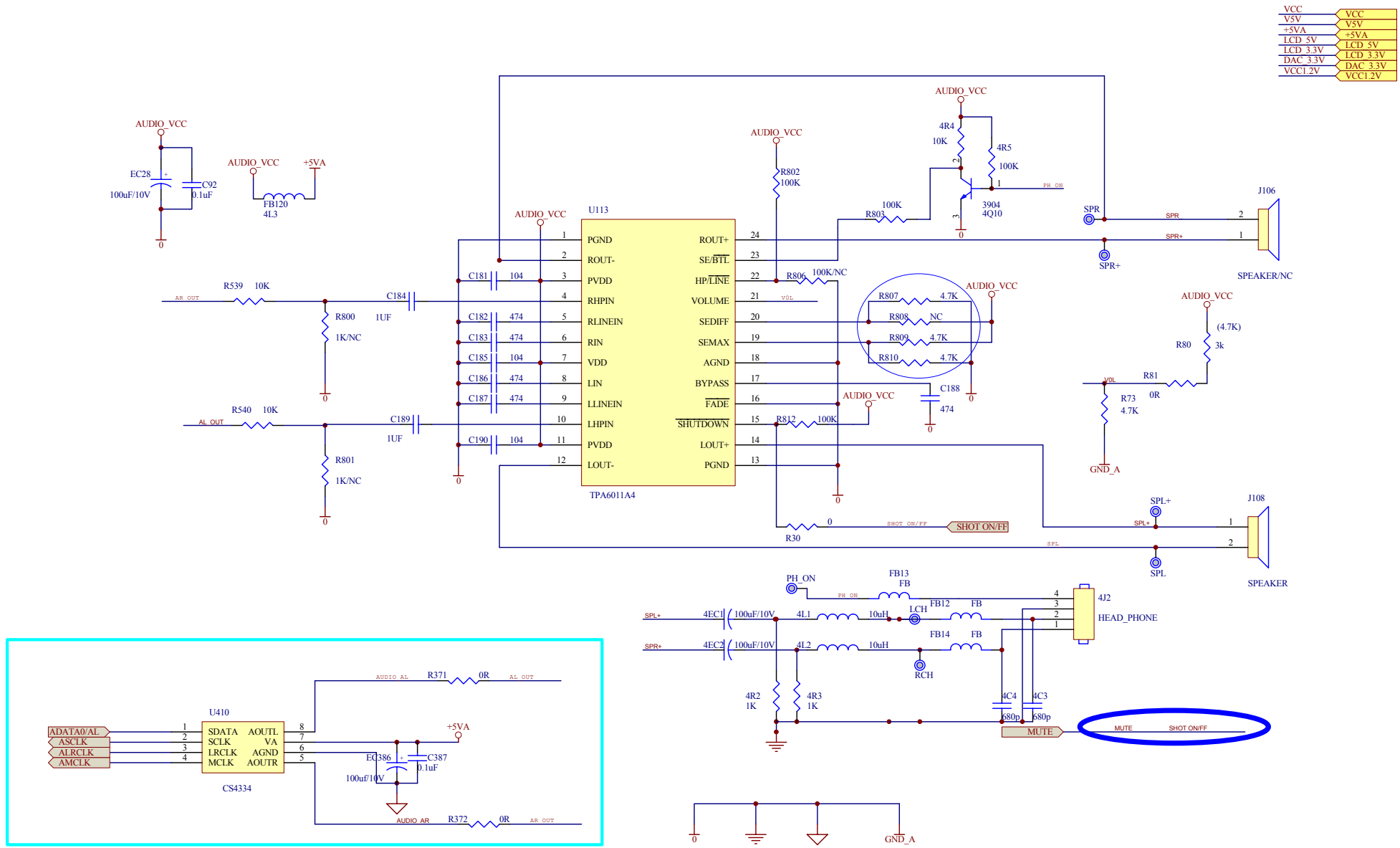
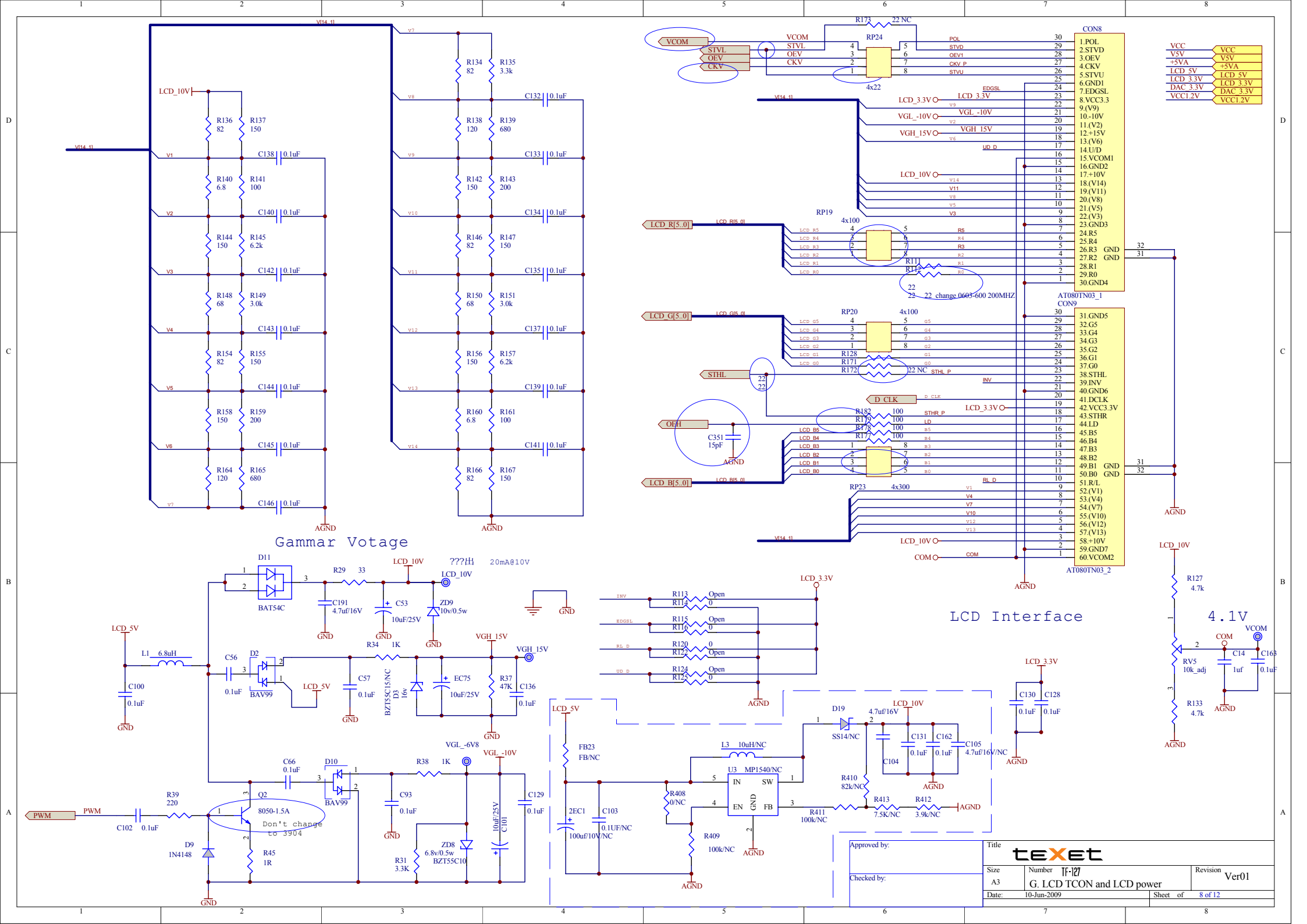
Checked by:	Size A4	Number I Rtc TF-127	Revision Ver01
	Date: 10-Jun-2009	Sheet of 10 of 12	



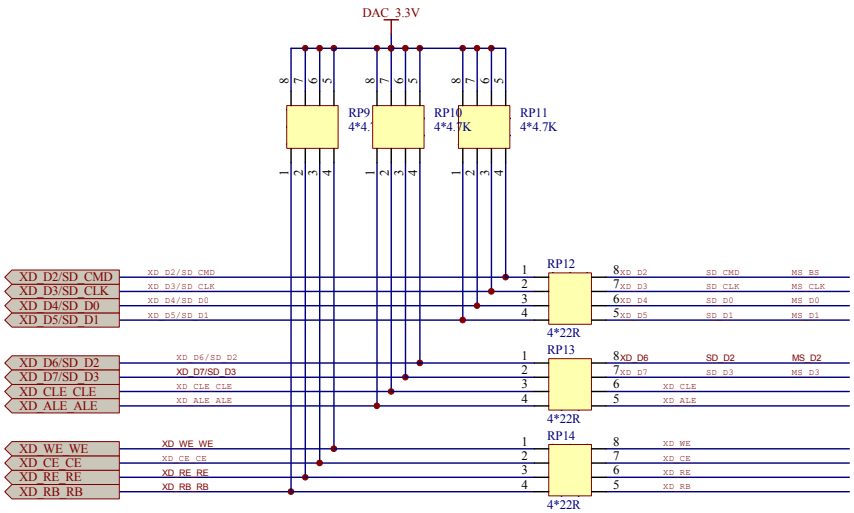
Approved by:	Title: texet	
Checked by:	Size: A4	Number: F. Usb TF-127
	Revision: Ver01	
	Date: 10-Jun-2009	Sheet of 7 of 12

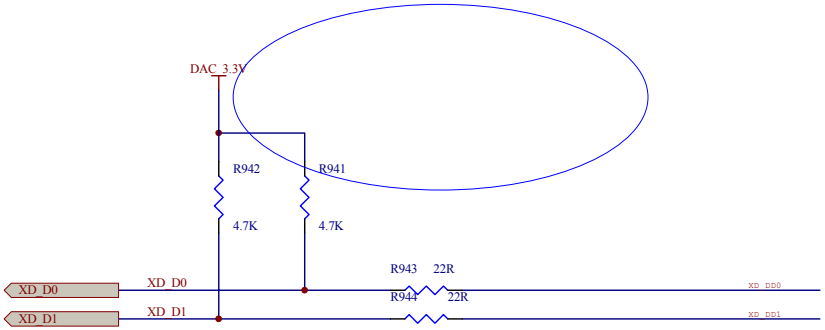


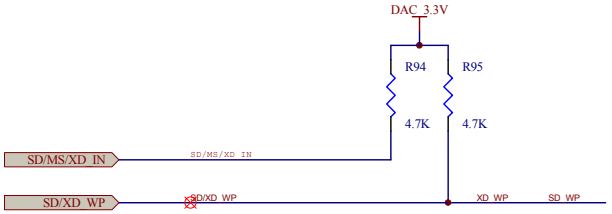
Approved by:	Title	teXet	
Checked by:	Size A3	Number J Audio TF-127	Revision Ver01
	Date: 10-Jun-2009	Sheet of 11 of 12	

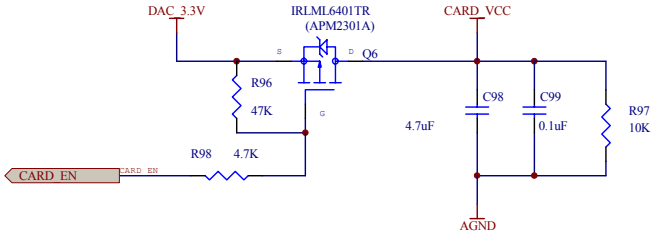

Gammar Votage
LCD Interface
4.1V
CON8
CON9
AT080TN03_1
AT080TN03_2
RP19
RP20
RP23
RP24
4x100
4x300
4x22
22 NC
22_change 0603-600 200MHZ
BAT54C
BAV99
BZT55C15/NC
BZT55C10
8050-1.5A
Don't change to 3904
1N4148
SS14/NC
MP1540/NC
0.1UF/NC
100uf/10V/NC
0/NC
100k/NC
82k/NC
7.5K/NC
3.9k/NC
100k/NC
RV5
10k_adj
TF-127
G. LCD TCON and LCD power
Ver01
10-Jun-2009
8 of 12
Approved by:
Checked by:
texet

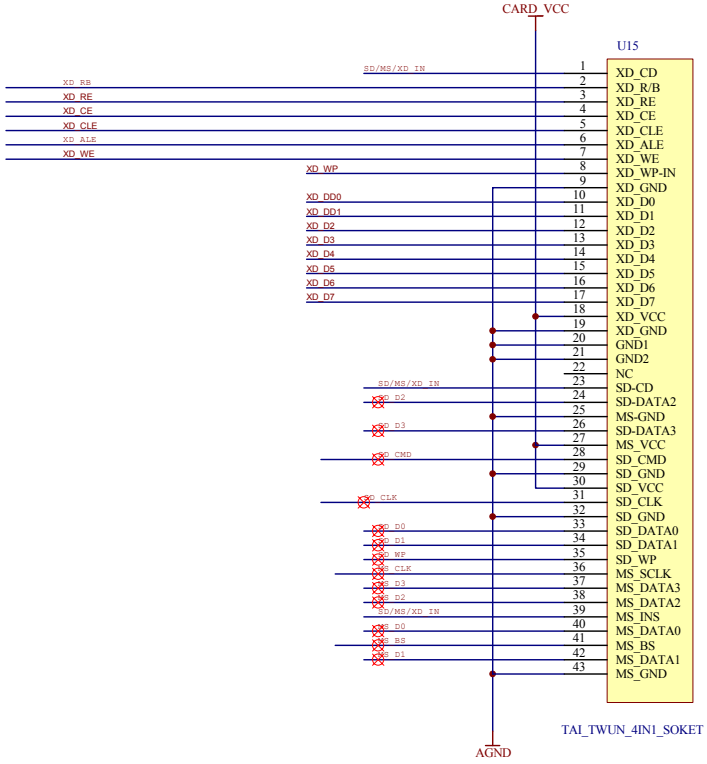
CARD PART

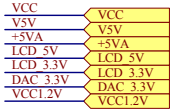




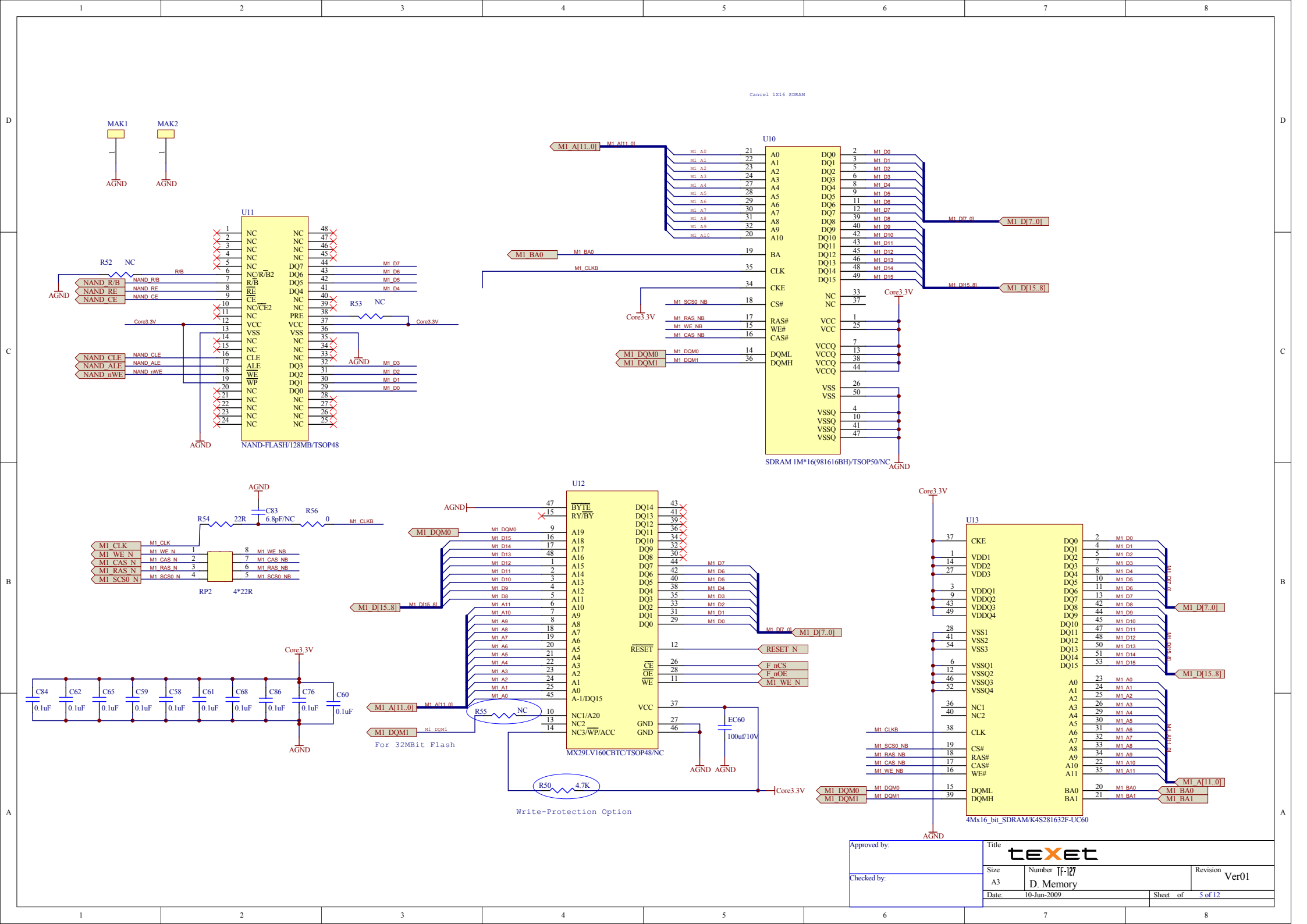


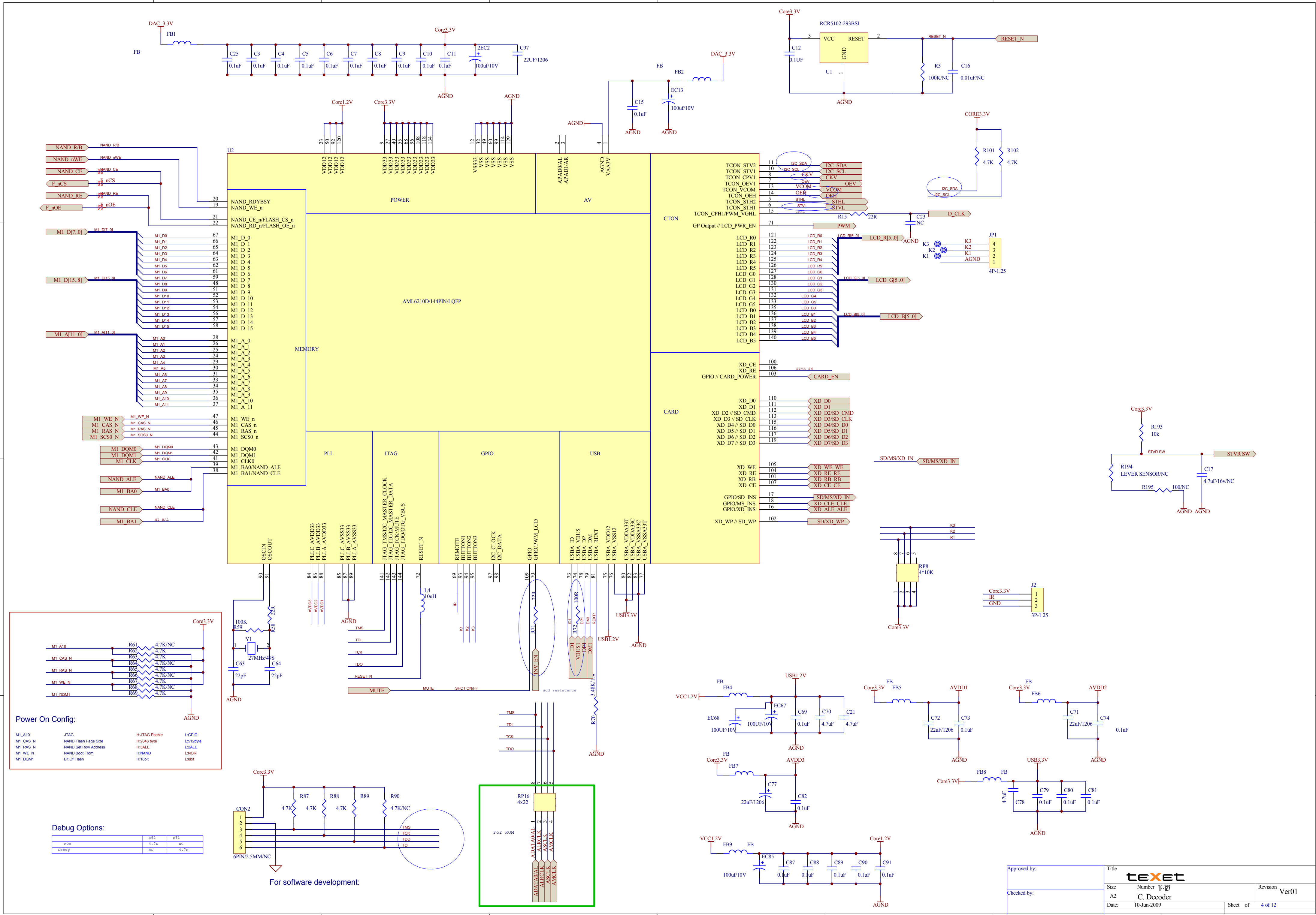






Approved by:	Title		
Checked by:	Size A3	Number E. Card TF-127	Revision Ver01
	Date: 10-Jun-2009	Sheet of 6 of 12	


Cancel 1X16 SDRAM
MAK1
MAK2
AGND
U11
NAND-FLASH/128MB/TSOP48
R52 NC
R53 NC
Core3.3V
NAND_R/B
NAND_RE
NAND_CE
NAND_CLE
NAND_ALE
NAND_nWE
U10
SDRAM 1M*16(981616BH)/TSOP50/NC
M1_A[11..0]
M1_BA0
M1_CLKB
M1_SCS0_NB
M1_RAS_NB
M1_WE_NB
M1_CAS_NB
M1_DQM0
M1_DQM1
M1_D[7..0]
M1_D[15..8]
R54 22R
C83 6.8pF/NC
R56 0
M1_CLK
M1_WE_N
M1_CAS_N
M1_RAS_N
M1_SCS0_N
RP2 4*22R
U12
MX29LV160CBTC/TSOP48/NC
For 32MBit Flash
R55 NC
R50 4.7K
Write-Protection Option
EC60 100uf/10V
RESET_N
F_nCS
F_nOE
M1_WE_N
C84 C62 C65 C59 C58 C61 C68 C86 C76 C60 0.1uF
U13
4Mx16_bit_SDRAM/K4S281632F-UC60
Approved by:
Checked by:
Title
texet
Size A3
Number TF-127
D. Memory
Revision Ver01
Date: 10-Jun-2009
Sheet of 5 of 12



DAC_3.3V
FB1
FB
C25 C3 C4 C5 C6 C7 C8 C9 C10 C11
0.1uF
2EC2
100uF/10V
C97
22UF/1206
Core3.3V
AGND
Core1.2V
Core3.3V
U2
NAND_R/B
NAND_nWE
NAND_CE
F_nCS
NAND_RE
F_nOE
M1_D[7..0]
M1_D[15..8]
M1_A[11..0]
M1_WE_N
M1_CAS_N
M1_RAS_N
M1_SCS0_N
M1_DQM0
M1_DQM1
M1_CLK
NAND_ALE
M1_BA0
NAND_CLE
M1_BA1
NAND_RDYBSY
NAND_WE_n
NAND_CE_n/FLASH_CS_n
NAND_RD_n/FLASH_OE_n
M1_D_0 … M1_D_15
M1_A_0 … M1_A_11
M1_WE_n
M1_CAS_n
M1_RAS_n
M1_SCS0_n
M1_DQM0
M1_DQM1
M1_CLK0
M1_BA0/NAND_ALE
M1_BA1/NAND_CLE
MEMORY
POWER
AV
CTON
CARD
PLL
JTAG
GPIO
USB
AML6210D/144PIN/LQFP
VDD12
VDD33
VSS33
VSS
APAD0/AL
APAD1/AR
AGND
VAA3V
TCON_STV2
TCON_STV1
TCON_CPV1
TCON_OEV1
TCON_VCOM
TCON_OEH
TCON_STH2
TCON_STH1
TCON_CPH1/PWM_VGHL
GP Output // LCD_PWR_EN
LCD_R0 … LCD_R5
LCD_G0 … LCD_G5
LCD_B0 … LCD_B5
I2C_SDA
I2C_SCL
CKV
OEV
VCOM
OEH
STHL
STVL
PWM
D_CLK
R15
22R
C23
NC
LCD_R[5..0]
LCD_G[5..0]
LCD_B[5..0]
XD_CE
XD_RE
GPIO // CARD_POWER
CARD_EN
XD_D0
XD_D1
XD_D2 // SD_CMD
XD_D3 // SD_CLK
XD_D4 // SD_D0
XD_D5 // SD_D1
XD_D6 // SD_D2
XD_D7 // SD_D3
XD_WE
XD_RE
XD_RB
XD_CE
GPIO/SD_INS
GPIO/MS_INS
GPIO/XD_INS
XD_WP // SD_WP
SD/MS/XD_IN
SD/XD_WP
OSCIN
OSCOUT
PLLC_AVDD33
PLLB_AVDD33
PLLA_AVDD33
PLLC_AVSS33
PLLB_AVSS33
PLLA_AVSS33
JTAG_TMS/I2C_MASTER_CLOCK
JTAG_TDI/I2C_MASTER_DATA
JTAG_TCK/MUTE
JTAG_TDO/OTG_VBUS
RESET_N
REMOTE
BUTTON1
BUTTON2
BUTTON3
I2C_CLOCK
I2C_DATA
GPIO
GPIO/PWM_LCD
USBA_ID
USBA_VBUS
USBA_DP
USBA_DM
USBA_REXT
USBA_VDD12
USBA_VSS12
USBA_VDDA33T
USBA_VDDA3C
USBA_VSSA3C
USBA_VSSA33T
100K
R59
R58
22R
Y1
27MHz/49S
C63
22pF
C64
22pF
L4
10uH
TMS
TDI
TCK
TDO
RESET_N
MUTE
SHOT ON/FF
R71
22R
INV_EN
add resistence
R72
100R
ID
VBUS
DP
DM
R70
3.48K/1%
USB3.3V
USB1.2V
Core3.3V
RCR5102-293BSI
VCC
RESET
GND
U1
C12
0.1UF
R3
100K/NC
C16
0.01uF/NC
RESET_N
DAC_3.3V
FB2
C15
0.1uF
EC13
100uF/10V
CORE3.3V
R101
4.7K
R102
4.7K
K3
K2
K1
JP1
4P-1.25
Core3.3V
R193
10k
STVR SW
R194
LEVER SENSOR/NC
R195
100/NC
C17
4.7uF/16v/NC
RP8
4*10K
J2
IR
GND
3P-1.25
VCC1.2V
FB4
EC68
100UF/10V
EC67
100UF/10V
C69
0.1uF
C70
4.7uF
C71
4.7uF
FB5
AVDD1
C72
22uF/1206
C73
0.1uF
FB6
AVDD2
C71
22uF/1206
C74
0.1uF
FB7
AVDD3
C77
22uF/1206
C82
0.1uF
FB8
USB3.3V
C78
4.7uF
C79 C80 C81
0.1uF
FB9
Core1.2V
EC85
100uF/10V
C87 C88 C89 C90 C91
0.1uF
R61 R62 R63 R64 R65 R66 R67 R68 R69
4.7K/NC
4.7K
M1_A10
M1_CAS_N
M1_RAS_N
M1_WE_N
M1_DQM1
CON2
6PIN/2.5MM/NC
R87 R88 R89 R90
4.7K
4.7K/NC
RP16
4x22
For ROM
ADATA0/AL
ALRCLK
ASCLK
AMCLK

Power On Config:

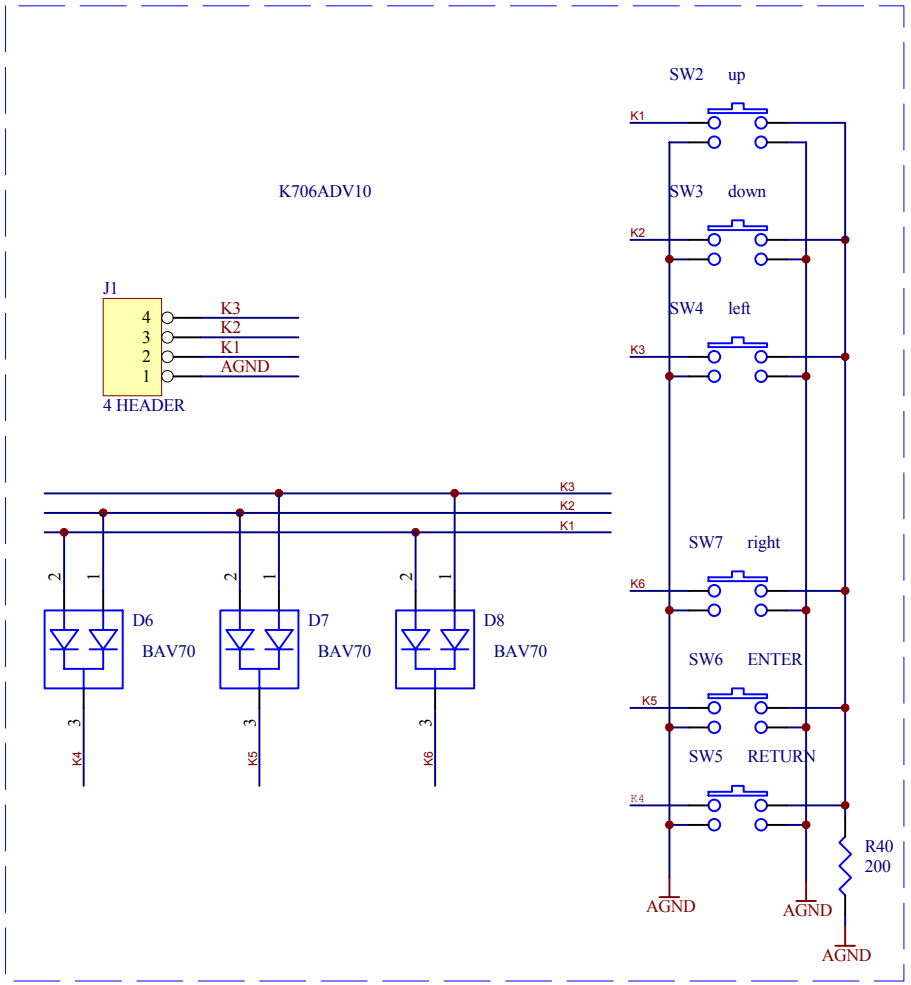
M1_A10	JTAG	H:JTAG Enable	L:GPIO
M1_CAS_N	NAND Flash Page Size	H:2048 byte	L:512byte
M1_RAS_N	NAND Set Row Address	H:3ALE	L:2ALE
M1_WE_N	NAND Boot From	H:NAND	L:NOR
M1_DQM1	Bit Of Flash	H:16bit	L:8bit

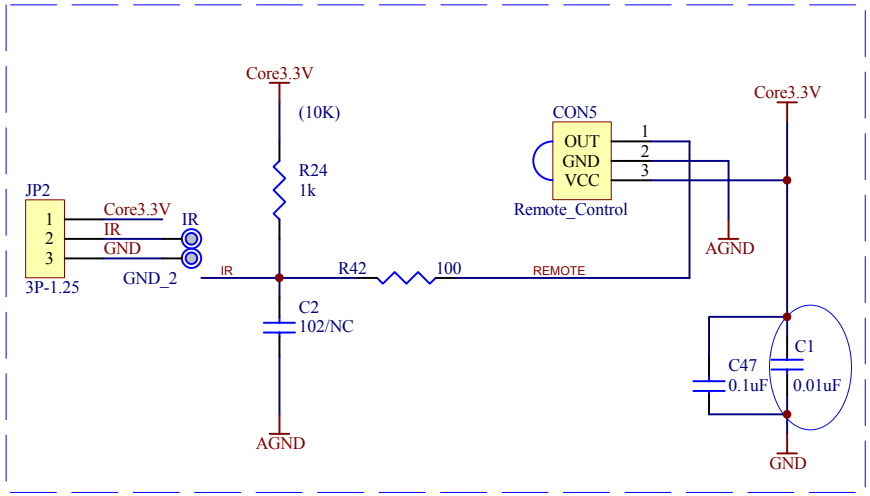
Debug Options:

	R62	R61
ROM	4.7K	NC
Debug	NC	4.7K

For software development:

Approved by:	Title: texet	
Checked by:	Size: A2 · Number: TF-127 · C. Decoder	Revision: Ver01
	Date: 10-Jun-2009	Sheet 4 of 12





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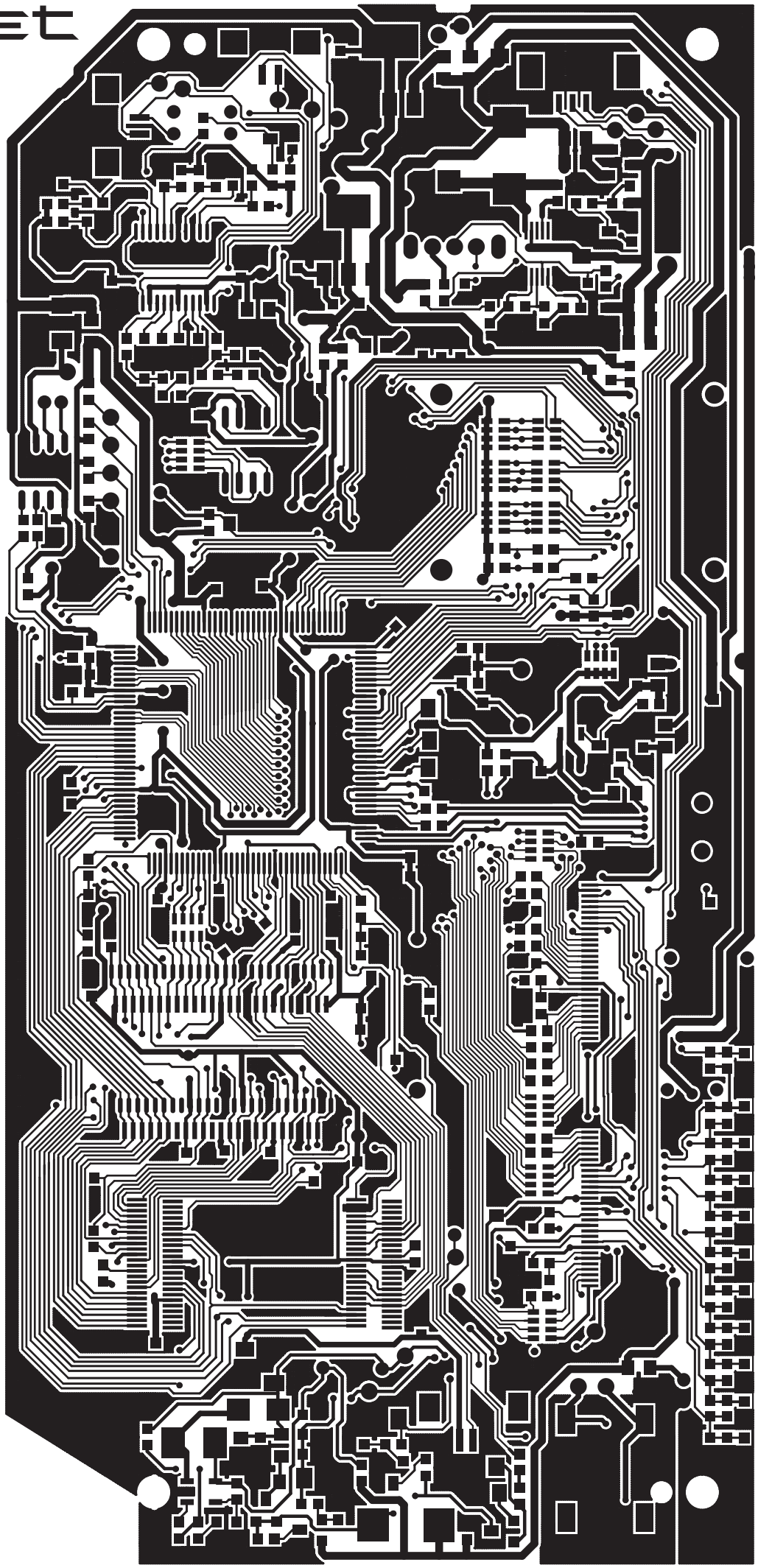
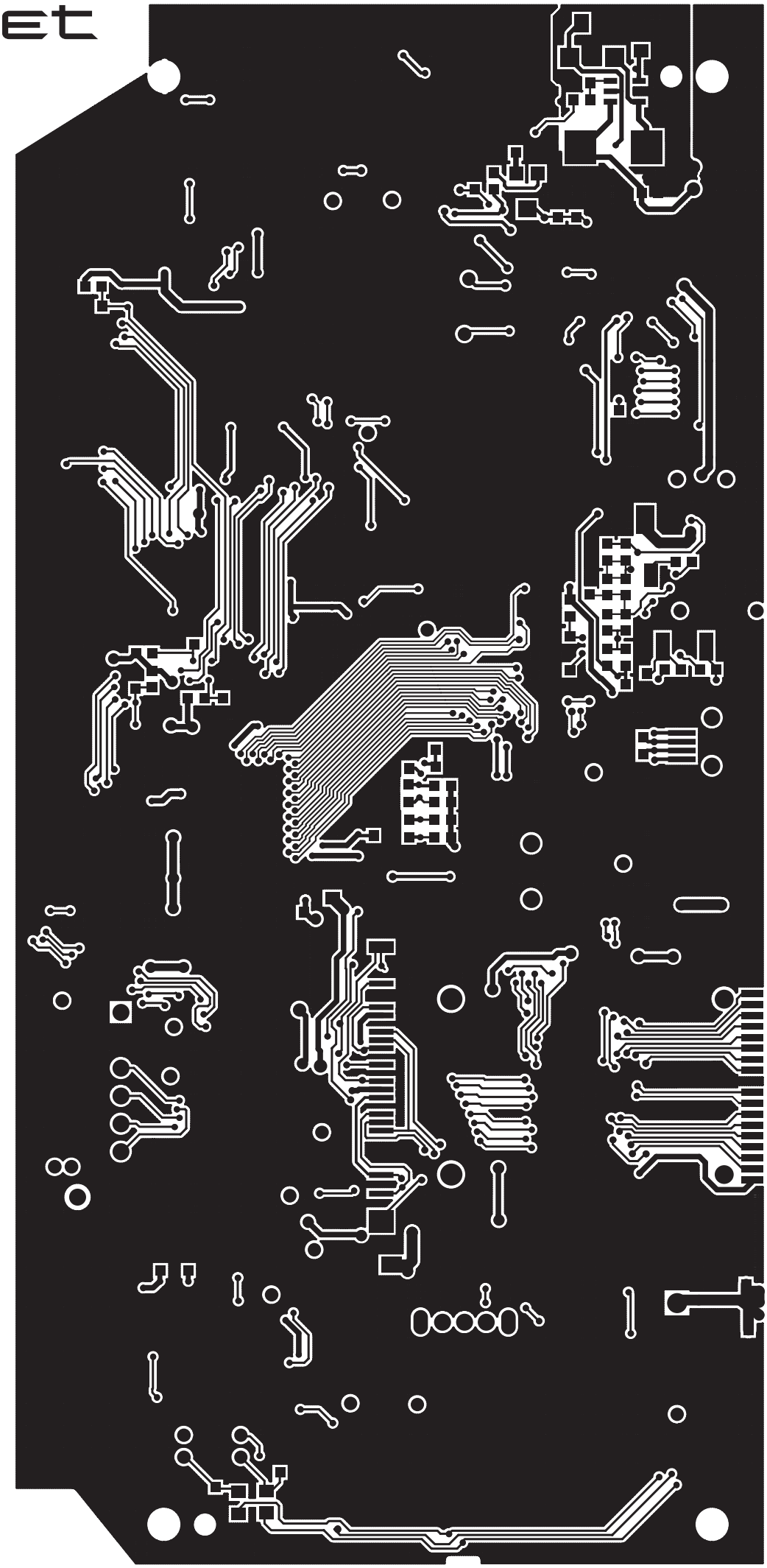
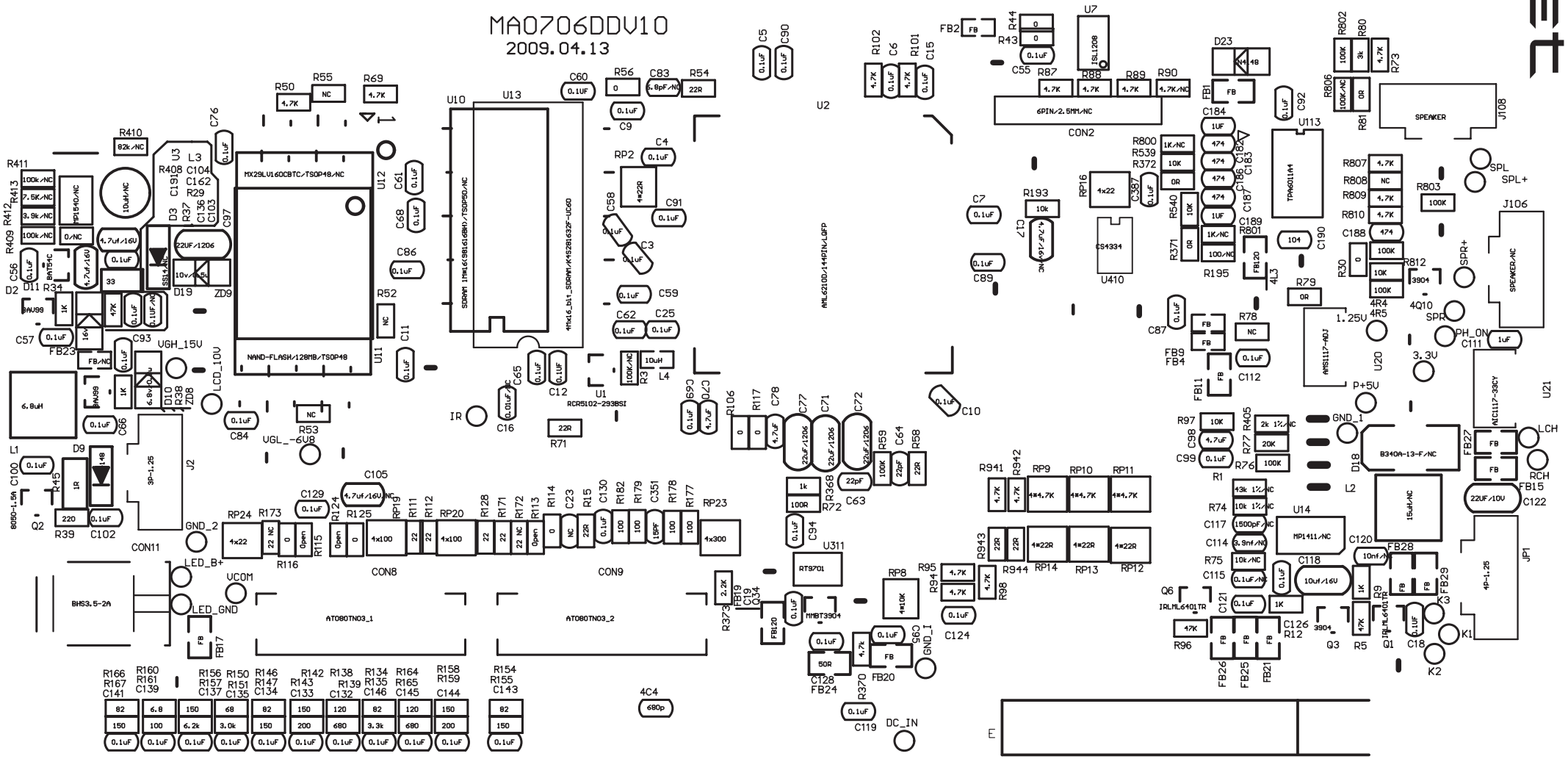
	Revision: Ver01	
	Date: 10-Jun-2009	Sheet of 12 of 12






MA0706DDV10
2009.04.13
MX29LV160CBTC/TSOP48/NC
NAND-FLASH/128MB/TSOP48
SDRAM 1Mx16/8Mx16/4Mx16/TSOP50/NC
4Mx16_b1_SDRAM/K4S281632F-UC60
RCR5102-293BSI
AML6210D/144PIN/LQFP
6PIN/2.5MM/NC
CON2
SPEAKER
SPL
SPL+
SPR+
SPR-
PH_ON
1.25V
3.3V
P+5V
GND_1
LCD_10V
VGH_15V
VGL_-6V8
LED_B+
LED_GND
VCOM
IR
LCH
RCH
DC_IN
CON11
CON8
CON9
ATO80TN03_1
ATO80TN03_2
BHS3.5-2A
3P-1.25
4P-1.25
SPEAKER/NC
TPA6011A4
CS4334
MP1411/NC
MP1540/NC
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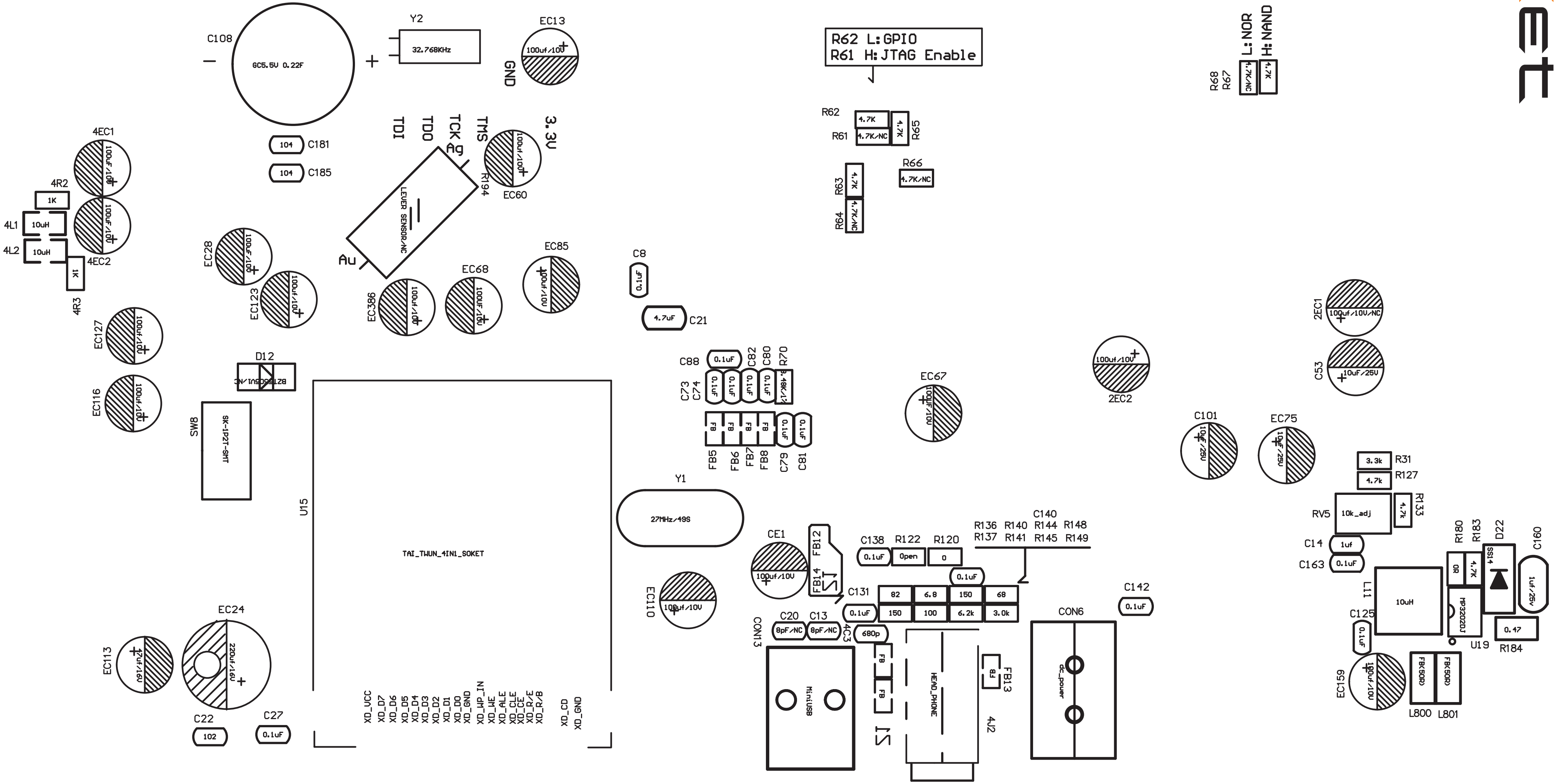
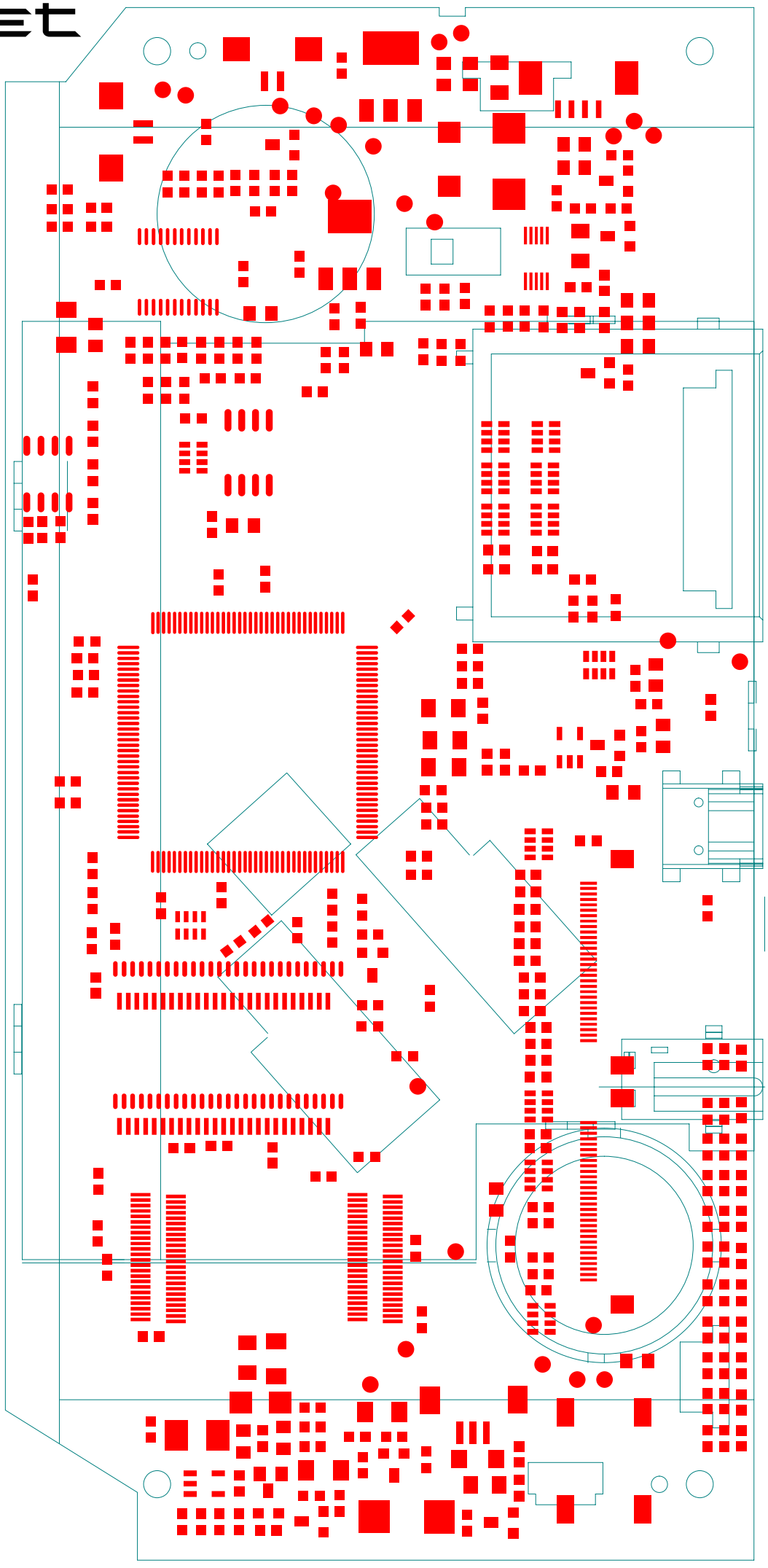
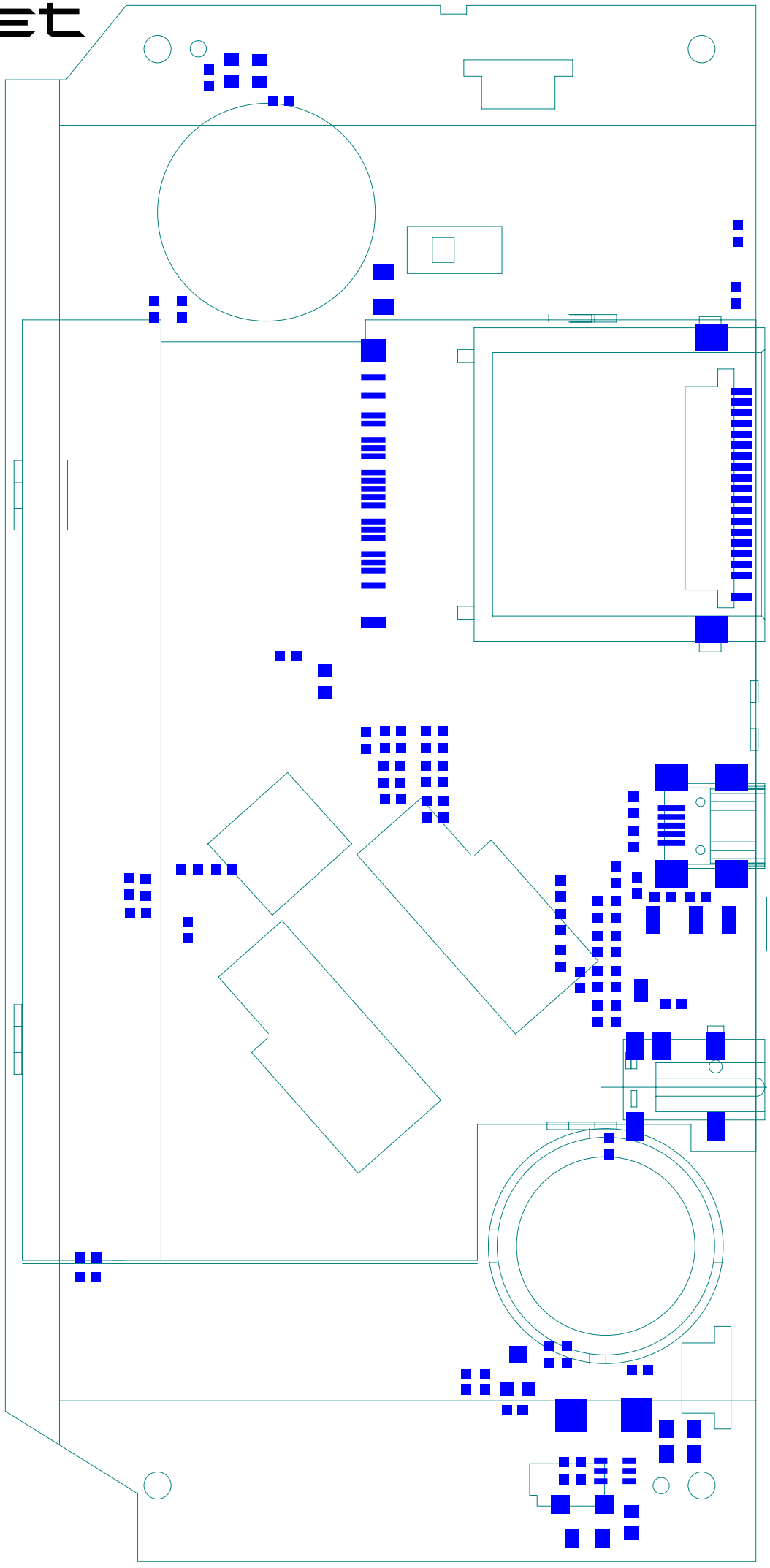
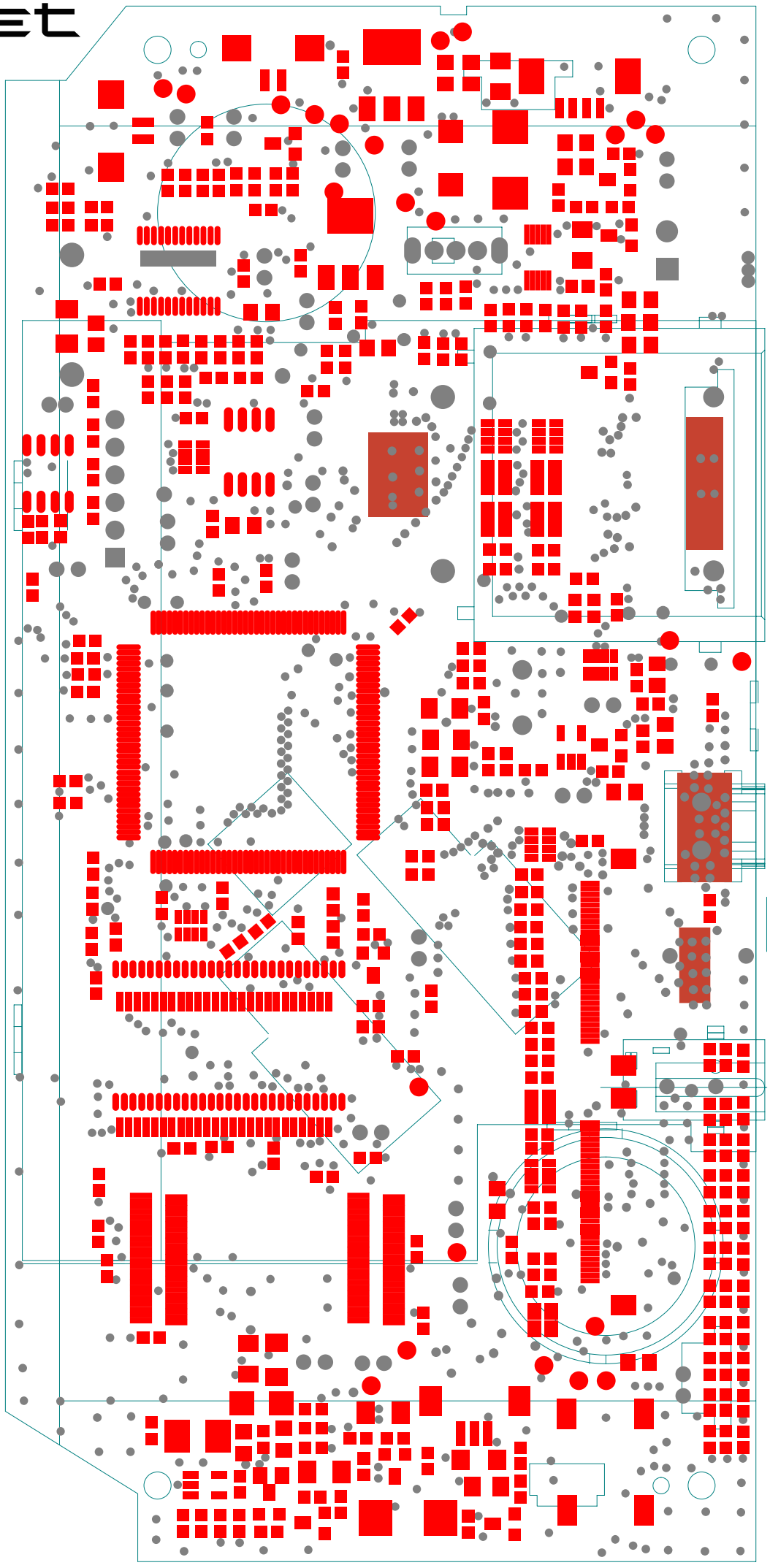
AMS1117-33CY
B340A-13-F/NC
ISL1208

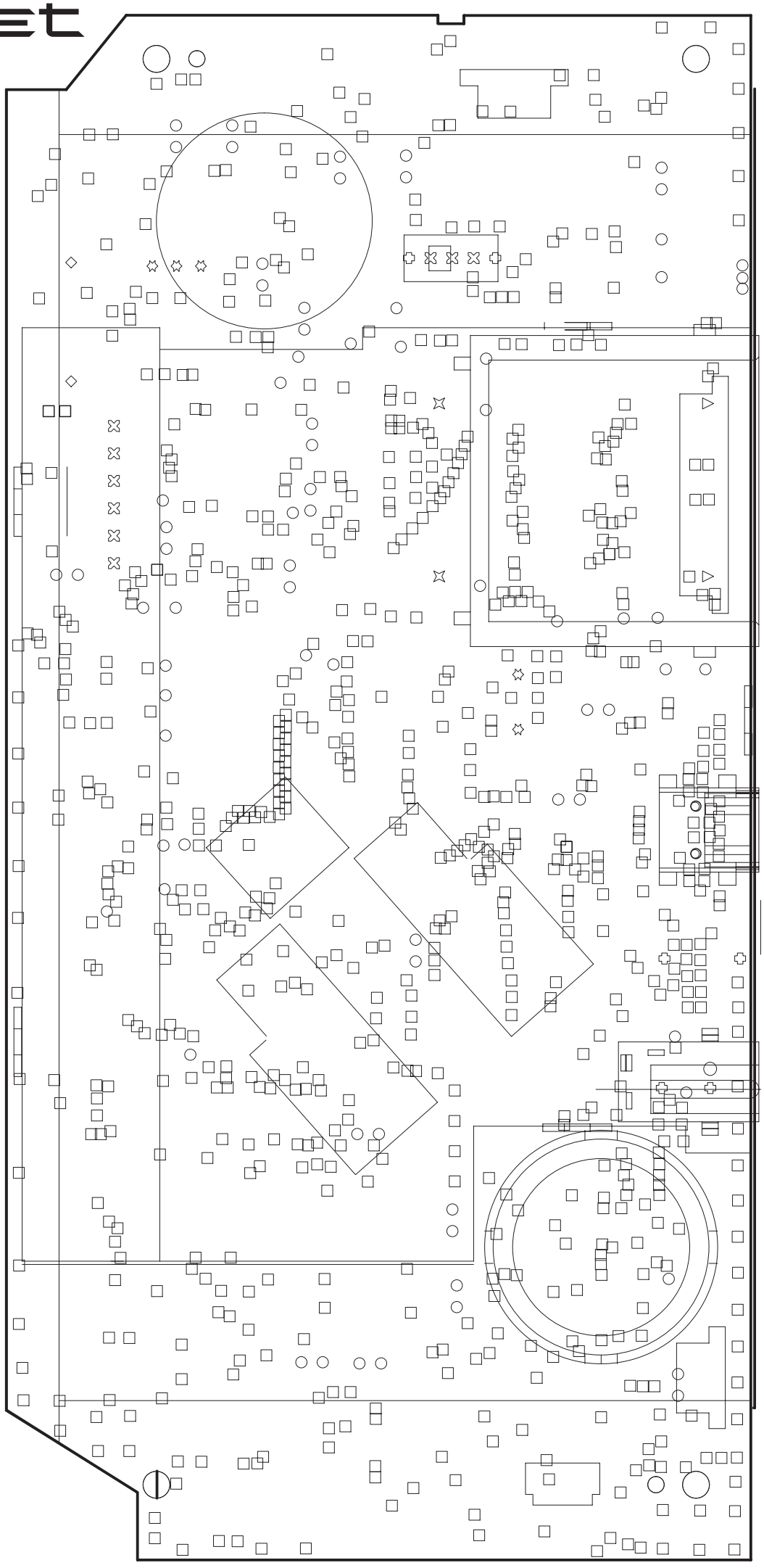

R62 L:GPIO
R61 H:JTAG Enable
L:NOR
H:NAND
TDI TDO TCK TMS
3.3V
GND
LEVER SENSOR/NC
TAI_TWUN_4IN1_SOKET
U15
27MHz/49S
32.768KHz
MiniUSB
HEAD_PHONE
dc_power
CON6
CON13
SK-1P2T-SMT
10k_adj
MP3202DJ
XD_VCC XD_D7 XD_D6 XD_D5 XD_D4 XD_D3 XD_D2 XD_D1 XD_D0 XD_GND XD_WP_IN XD_WE XD_ALE XD_CLE XD_CE XD_R/E XD_R/B XD_CD XD_GND

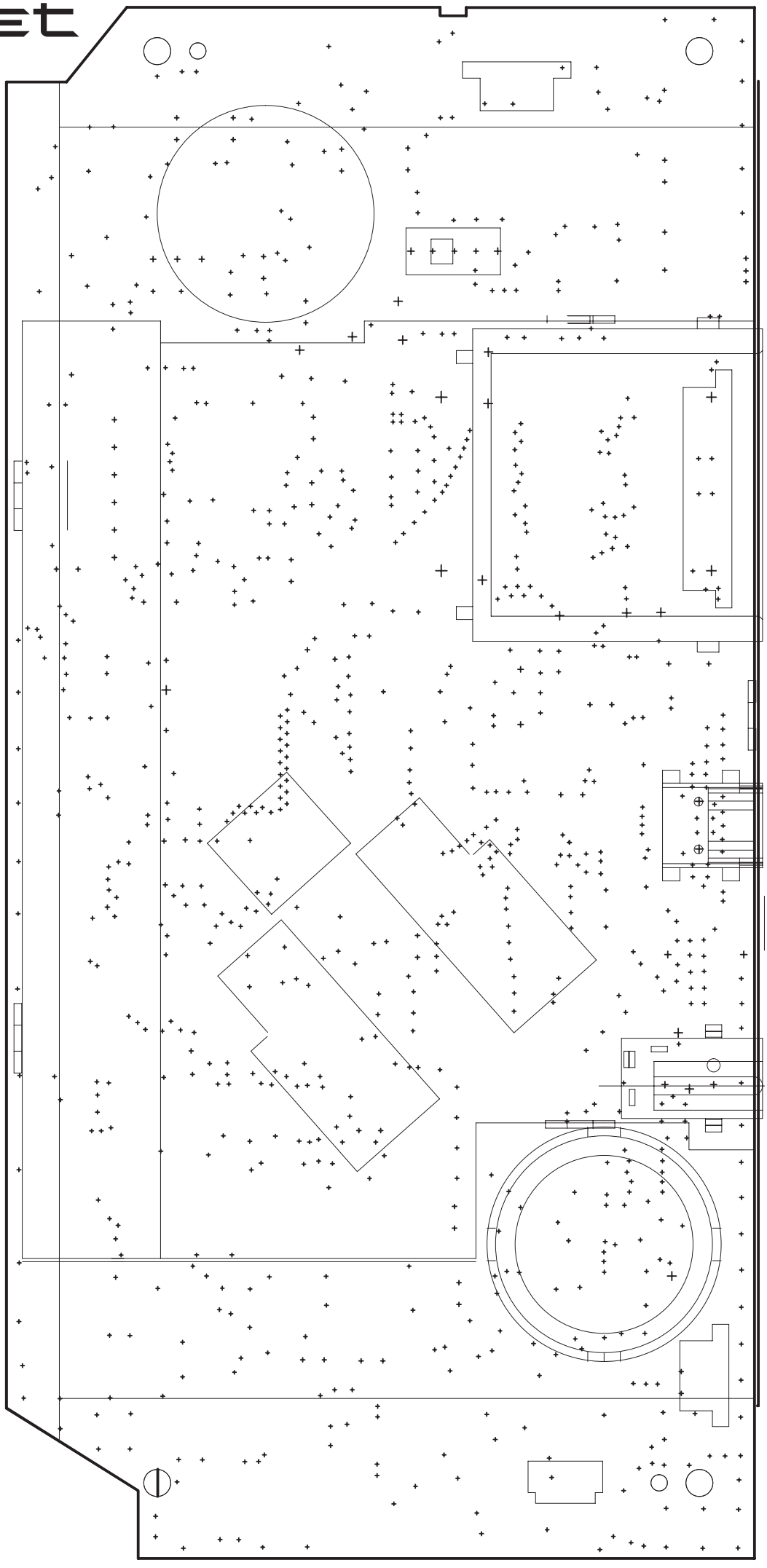
TF-127

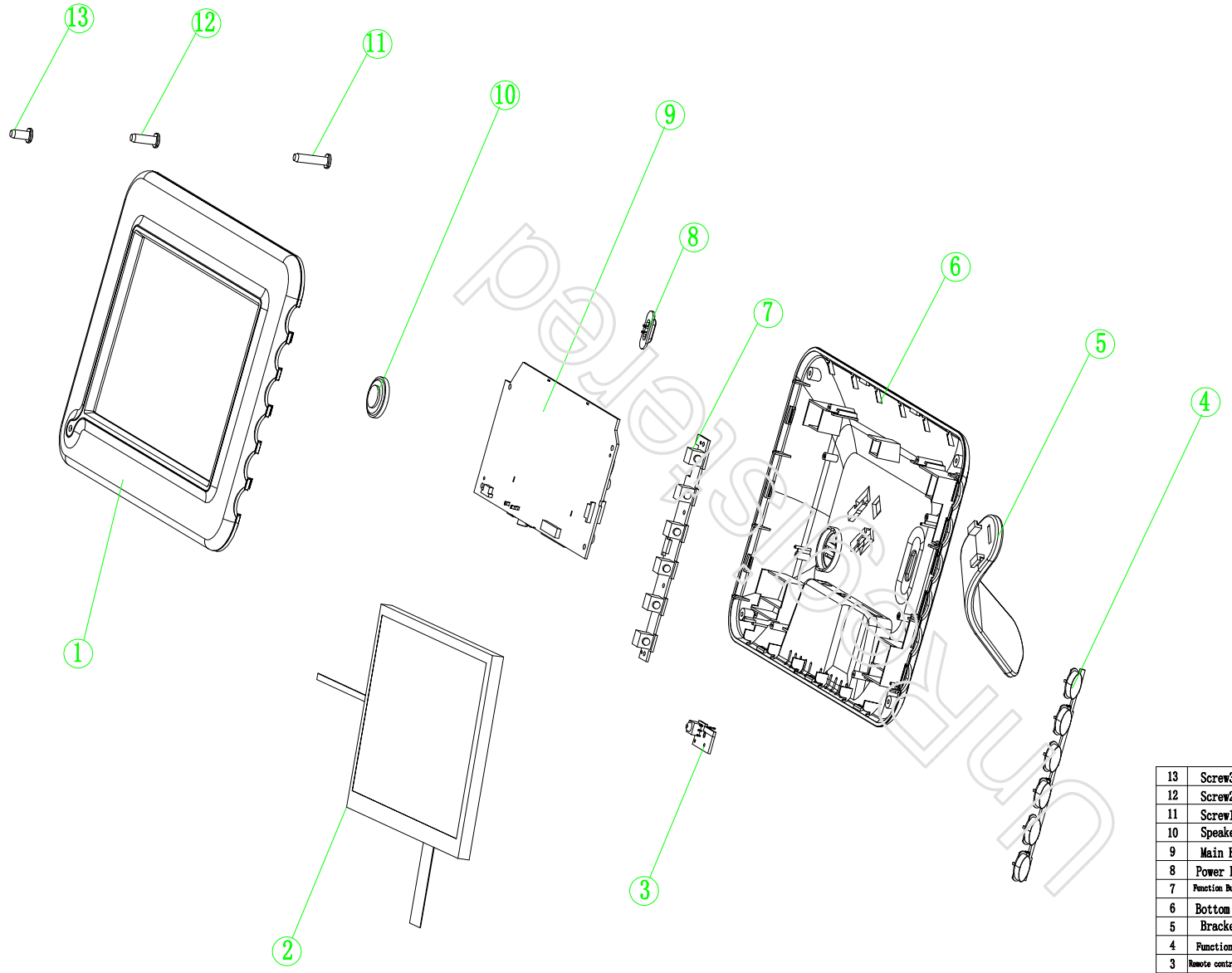












NO.	PARTS NAME	PARTS NO.	Q'TY	MATERIAL	REMARK
13	Screw3		3		1.7*4CBHNI
12	Screw2		4		1.7*5CBHNI
11	Screw1		4		1.7*6CBHNI
10	Speaker		1		
9	Main Board		1		
8	Power Button		1	ABS	
7	Function Button PCB		1		
6	Bottom Cover		1	ABS	
5	Bracket		1	ABS	
4	Function Button		1	ABS	
3	Remote control panels		1		
2	Screen(7Inch)		1		
1	Panel and Middle-Panel		1	ABS	

DEMENTION	TOLERANCE
≤3~10	±0.05
≤10~50	±0.10
≤50~100	±0.15
≤100~500	±0.20
ANGLE	±0.5

MODEL	TF-127			texet	
REV					
UNIT	mm	DSGN	ZHONG WEI JUN	DATE	2009.07.14
SCALE		CHK		DATE	
SHEET	TOTAL	APPR		DATE	

INNOLUX DISPLAY CORPORATION

LCD MODULE

SPECIFICATION

Customer: _____

Model Name: AT070TN82

SPEC NO.: A070-82-TT-01

Date: 2008/07/22

Version: 01

■Preliminary Specification

□Final Specification

For Customer's Acceptance

Approved by	Comment

Approved by	Reviewed by	Prepared by
Joe Lin 2008/07/31	Hans Chen 2008/07/31	Kevin Chen 2008/07/31

INNOLUX

Record of Revision

Version	Revise Date	Page	Content
Pre-spec. 01	2008/07/22		Initial release.

INNOLUX

Contents

1. General Specifications

No.	Item	Specification	Remark
1	LCD size	7.0 inch(Diagonal)	
2	Driver element	a-Si TFT active matrix	
3	Resolution	800 × 3(RGB) × 480	
4	Display mode	Normally white, Transmissive	
5	Dot pitch	0.0635(W) × 0.1905(H) mm	
6	Active area	152.4 (W) × 91.44 (H) mm	
7	Module size	165(W) × 104(H) × 5.5(D) mm	Note1
8	Surface treatment	Anti-Glare	
9	Color arrangement	RGB-stripe	
10	Interface	Digital	
11	Backlight power consumption	(1.782W) (Typ.)	
12	Panel power consumption	0.437W (Typ.)	
13	Weight	TBD	

Note1: Refer to Mechanical Drawing.

2. Pin Assignment

2.1. TFT LCD Panel Driving Section

FPC Connector is used for the module electronics interface. The recommended model is P-TWO “AF 730L-A2G1T” manufactured by P-TWO.

Pin No.	Symbol	I/O	Function	Remark
1	POL	I	Polarity selection	
2	STVD	I/O	Vertical start pulse input when U/D= H	Note 1
3	OEV	I	Output enable	
4	CKV	I	Vertical clock	
5	STVU	I/O	Vertical start pulse input when U/D= L	Note 1
6	GND	P	Power Ground	
7	EDGSL	I	Select rising edge or falling edge	
8	DV_{DD}	P	Power for Digital Circuit	
9	V9	I	Gamma voltage level 9	
10	V_{GL}	P	Gate OFF voltage	
11	V2	I	Gamma voltage level 2	
12	V_{GH}	P	Gate ON voltage	
13	V6	I	Gamma voltage level 6	
14	U/D	I	Up/down selection	Note 1,2
15	V_{COM}	I	Common voltage	
16	GND	P	Power Ground	
17	AV_{DD}	P	Power Voltage for Analog Circuit	
18	V14	I	Gamma voltage level 14	
19	V11	I	Gamma voltage level 11	

20	V8	I	Gamma voltage level 8	
21	V5	I	Gamma voltage level 5	
22	V3	I	Gamma voltage level 3	
23	GND	P	Power Ground	
24	R5	I	Red data(MSB)	
25	R4	I	Red data	
26	R3	I	Red data	
27	R2	I	Red data	
28	R1	I	Red data	
29	R0	I	Red data(LSB)	
30	GND	P	Power Ground	
31	GND	P	Power Ground	
32	G5	I	Green data(MSB)	
33	G4	I	Green data	
34	G3	I	Green data	
35	G2	I	Green data	
36	G1	I	Green data	
37	G0	I	Green data(LSB)	
38	STHL	I/O	Horizontal start pulse input when R/L = L	Note 1
39	REV	I	Control signal are inverted or not	Note3
40	GND	I	Power Ground	
41	DCLK	I	Sample clock	
42	DV_{DD}	P	Power Voltage for Digital Circuit	
43	STHR	I/O	Horizontal start pulse input when R/L =H	Note 1
44	LD	I	Latches the polarity of outputs and Switches the new data to outputs	

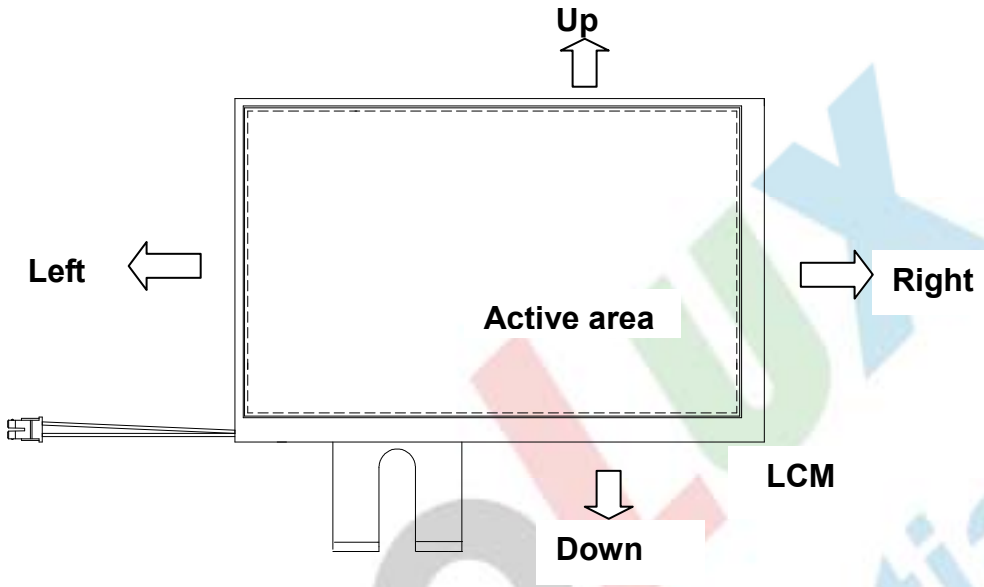
45	B5	I	Blue data (MSB)	
46	B4	I	Blue data	
47	B3	I	Blue data	
48	B2	I	Blue data	
49	B1	I	Blue data	
50	B0	I	Blue data (LSB)	
51	R/L	I	Right/ left selection	Note 1,2
52	V1	I	Gamma voltage level 1	
53	V4	I	Gamma voltage level 4	
54	V7	I	Gamma voltage level 7	
55	V10	I	Gamma voltage level 10	
56	V12	I	Gamma voltage level 12	
57	V13	I	Gamma voltage level 13	
58	AV_{DD}	P	Power for Analog Circuit	
59	GND	P	Power Ground	
60	V_{COM}	I	Common voltage	

I: input, O: output, P: Power

Note 1: Selection of scanning mode

Setting of scan control input		IN/OUT state for start pulse				Scanning direction
U/D	R/L	STVD	STVU	STHR	STHL	
GND	DV_{DD}	O	I	I	O	Up to down, left to right
DV_{DD}	GND	I	O	O	I	Down to up, right to left
GND	GND	O	I	O	I	Up to down, right to left
DV_{DD}	DV_{DD}	I	O	I	O	Down to up, left to right

Note 2: Definition of scanning direction.
Refer to the figure as below:



Note 3: When REV="L", it's under normal operation.
When REV="H", these data will be inverted.

2.2. Backlight Unit Section

LED Light Bar Connector is used for the integral backlight system.
The recommended model is BHSR-02VS-1 manufactured by JST.

Pin No.	Symbol	I/O	Function	Remark
1	V_{LED+}	P	Power for LED backlight anode	Pink
2	V_{LED-}	P	Power for LED backlight cathode	White

3. Operation Specifications

3.1. Absolute Maximum Ratings

(Note 2)

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Power voltage	DV_{DD}	-0.5	5	V	
	AV_{DD}	-0.5	13.5	V	
	V_{GH}	-0.3	20.0	V	
	V_{GL}	-13.0	0.3	V	
	V_{GH}-V_{GL}	-	33.0	V	
Input signal voltage	V1~V7	0.4 AV_{DD}	AV_{DD}+0.3	V	Note 1
	V8~V14	-0.3	0.6AV_{DD}	V	
Operation Temperature	T_{OP}	-30	85	℃	
Storage Temperature	T_{ST}	-30	85	℃	
LED Reverse Voltage	Vr	-	1.2	V	Each LED Note 3
LED Forward Current	IF	-	25	mA	Each LED

Note 1: AV_{DD}-0.1≥ V1≥ V2≥ V3≥ V4≥ V5≥ V6≥ V7,
V8≥ V9≥ V10≥ V11≥ V12≥ V13≥ V14≥ AV_{SS}+0.1.

Note 2: The absolute maximum rating values of this product are not allowed to be exceeded at any times. A module should be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme condition, the module may be permanently destroyed.

Note 3: Vr Conditions: Zener Diode 20mA

3.2. Typical Operation Conditions

(Note 1)

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	DV_{DD}	3.0	3.3	3.6	V	Note 2
	AV_{DD}	10.2	10.4	10.6	V	
	V_{GH}	15.3	16.0	16.7	V	
	V_{GL}	-7.7	-7.0	-6.3	V	
Input signal voltage	V_{COM}	-	4.1	-	V	(V1+V14)/2 =5.2V
	V1~V7	0.4 AV_{DD}	-	AV_{DD} -0.1	V	
	V8~V14	0.1	-	0.6 AV_{DD}	V	
Input logic high voltage	V_{IH}	0.7 DV_{DD}	-	DV_{DD}	V	Note 3
Input logic low voltage	V_{IL}	0	-	0.3 DV_{DD}	V	

Note 1: Be sure to apply DV_{DD} and V_{GL} to the LCD first, and then apply V_{GH}.
Note 2: DV_{DD} setting should match the signals output voltage (refer to Note 3) of customer's system board.
Note 3: POL, STVD, OEV, CKV, STVU, EDGSL, U/D, STHL, REV, DCLK, STHR, LD, R/L. R0~R5, G0~G5, B0~B5.

3.2.1. Current Consumption

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Current for Driver	I_{GH}	-	0.2	0.5	mA	V_{GH} =16.0V
	I_{GL}	-	0.2	1.0	mA	V_{GL} = -7.0V
	IDV_{DD}	-	5.0	10.0	mA	DV_{DD} =3.3V
	IAV_{DD}	-	40.0	50.0	mA	AV_{DD} =10.4V

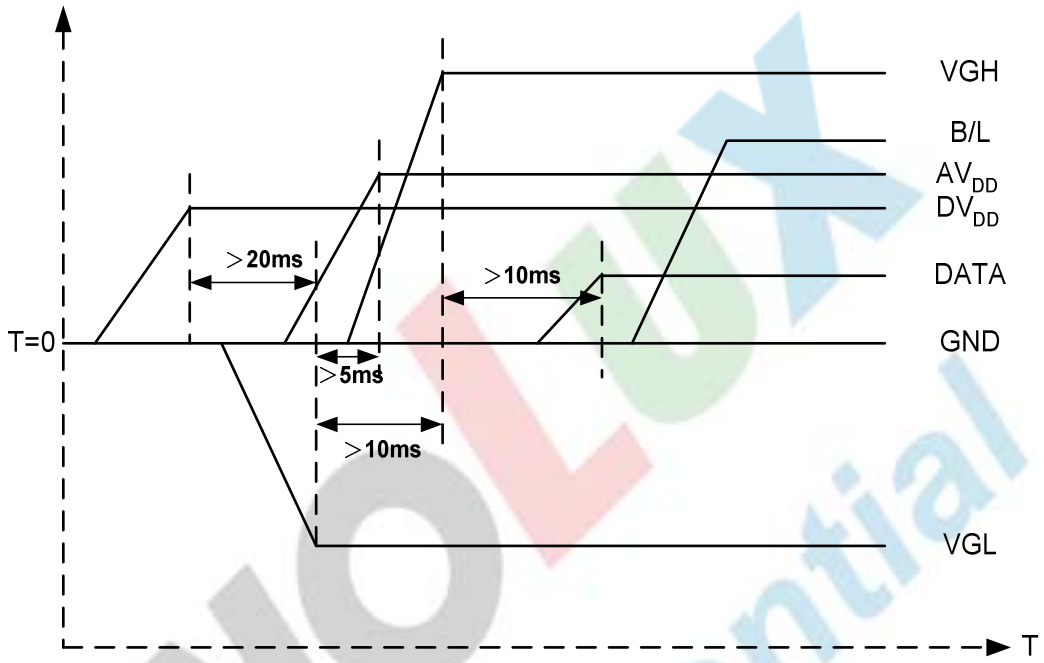
3.2.2. Backlight Driving Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Voltage for LED Backlight	V_L	(9.3)	(9.9)	(10.5)	V	Note1
Current for LED Backlight	I_L	(170)	(180)	(200)	mA	
LED life time	-	20,000	-	-	Hr	Note 2

Note 1: The Voltage for LED Backlight is defined at Ta=25℃ and I_L =180mA.
Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and I_L =180mA. The LED lifetime could be decreased if operating I_L is larger than 180 mA.

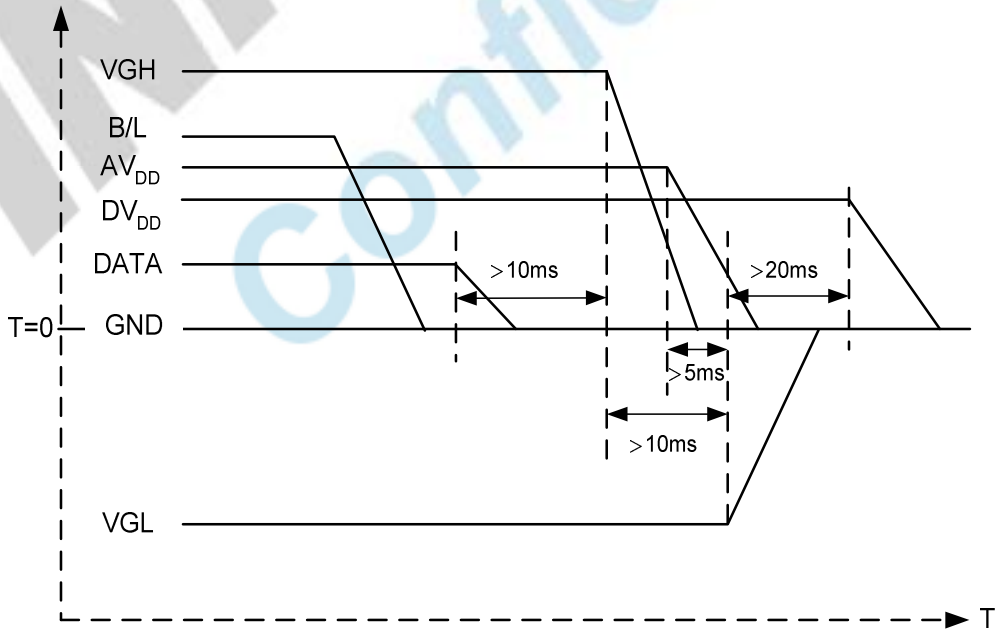
3.3. Power Sequence

1. Power on:



DV_{DD}→VGL→VGH→Data→B/L

2. Power off:



B/L→Data→VGH→VGL→DV_{DD}

Note: Data include DCLK,POL,OEV,CKV,STVU,STVD,STHL,STHR,LD,R0~R5,G0~G5,B0~B5

3.4. Timing Characteristics

3.4.1. Timing Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
DCLK frequency	Fdclk	-	40	45	MHz	
DCLK cycle	Tcph	22	25	-	ns	
DCLK pulse width	Tcw	8	-	-	ns	
Data set-up time	Tsu	4	-	-	ns	
Data hold time	Thd	2	-	-	ns	
Time that the last data to LD	Tld	1	-	-	Tcph	
Pulse width of LD	Twld	2	-	-	Tcph	
Time that LD to STHL/R	Tlds	5	-	-	Tcph	
POL set-up time	Tpsu	6	-	-	ns	
POL hold time	Tphd	6	-	-	ns	
CKV frequency	Fvclk	-	-	200	KHz	
CKV rise time	Trck	-	-	100	ns	
CKV falling time	Tfck	-	-	100	ns	
CKV pulse width	PWCLK	500	-	-	ns	
Horizontal display timing range	Tdh	-	800	-	Tcph	
Horizontal timing range	Th	-	1056	-	Tcph	
STVU/D setup time	Tsuv	200	-	-	ns	
STVU/D hold time	Thdv	300	-	-	ns	
STVU/D delay time	Tdt	-	-	500	ns	
Driver output delay time	Tdo	-	-	900	ns	

Output rise time	Ttlh	-	500	1000	ns	
Output falling time	Tthl	-	400	800	ns	
OEV pulse width	Twcl	1	-	-	us	
OEV to Driver output delay time	Toe	-	-	900	ns	
Horizontal lines per field	Tv	512	525	610	Tdh	
Vertical display timing range	Tvd	-	480	-	Tdh	

3.4.2. Timing Diagram

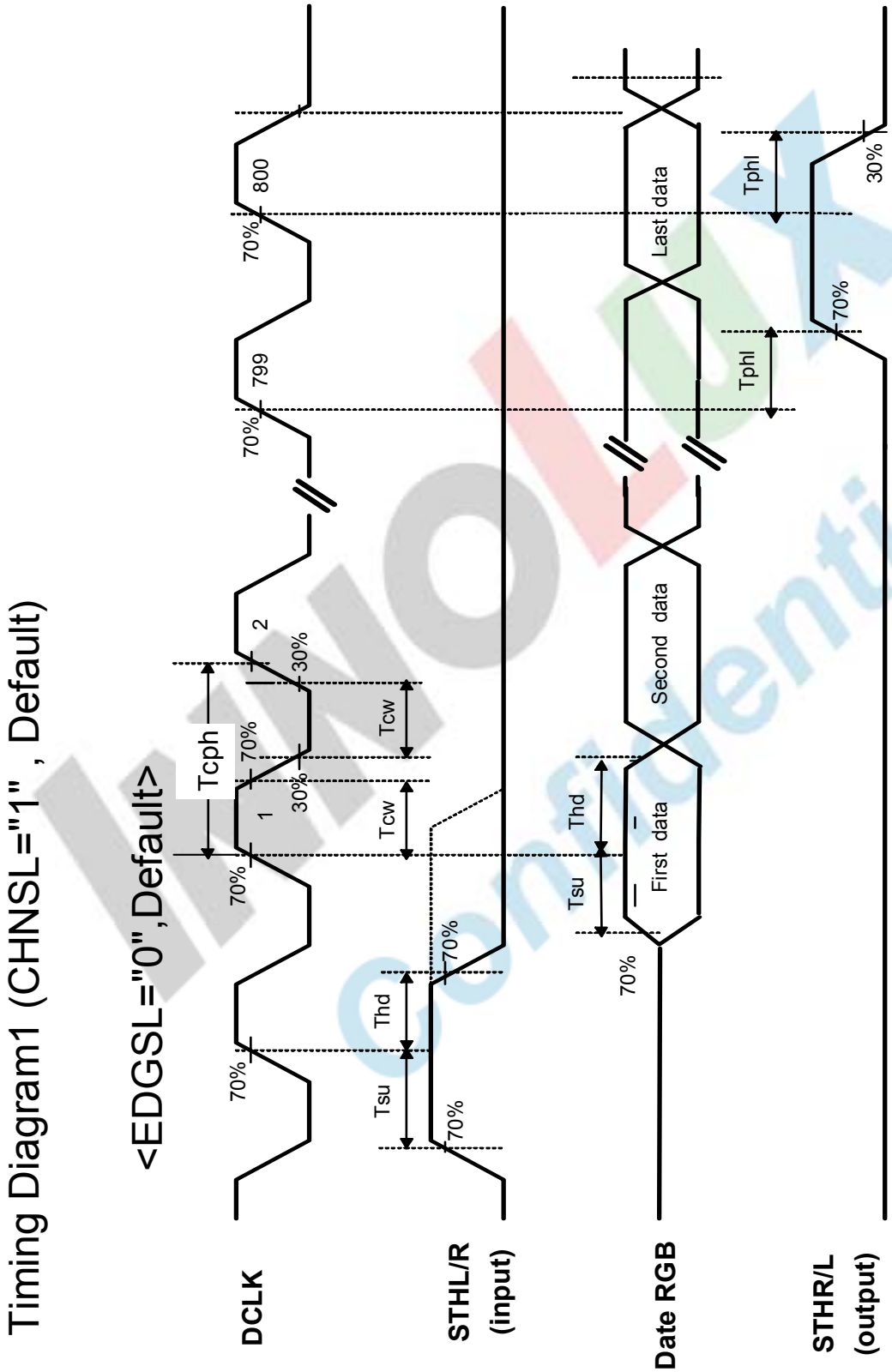


Fig.3-1 operation model 1

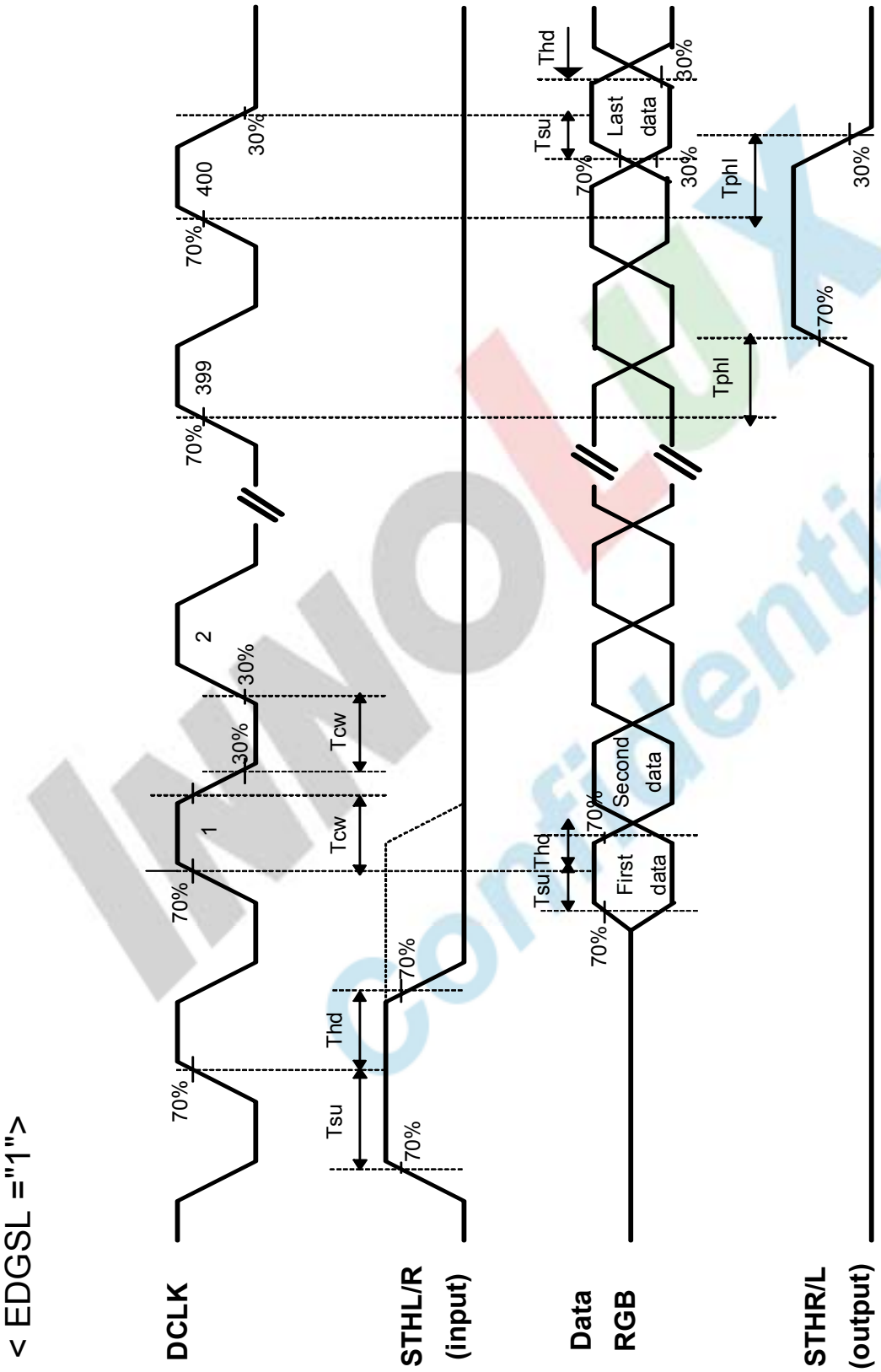


Fig.3-2 operation model 2

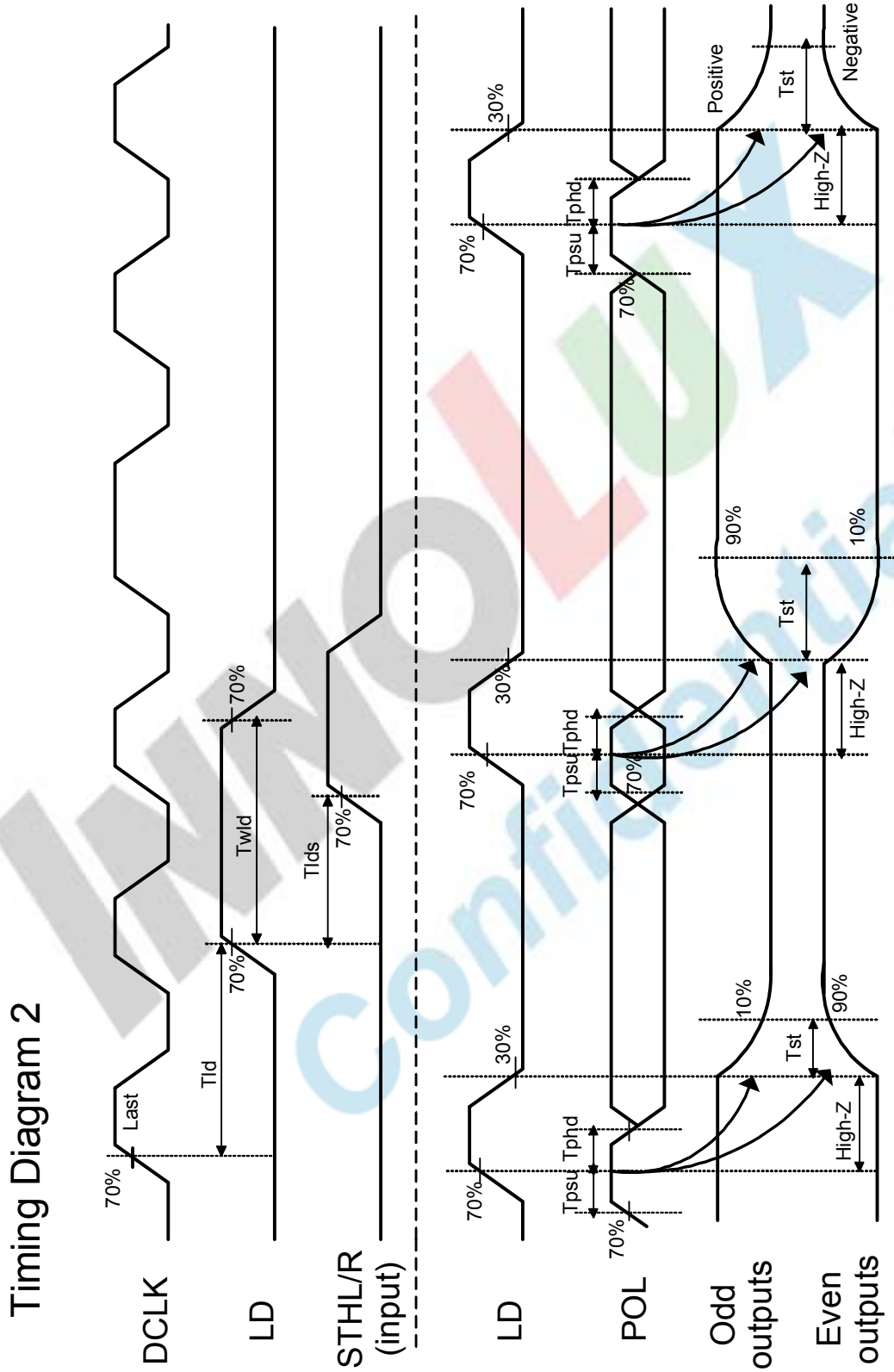


Fig.3-3 Horizontal timing 1

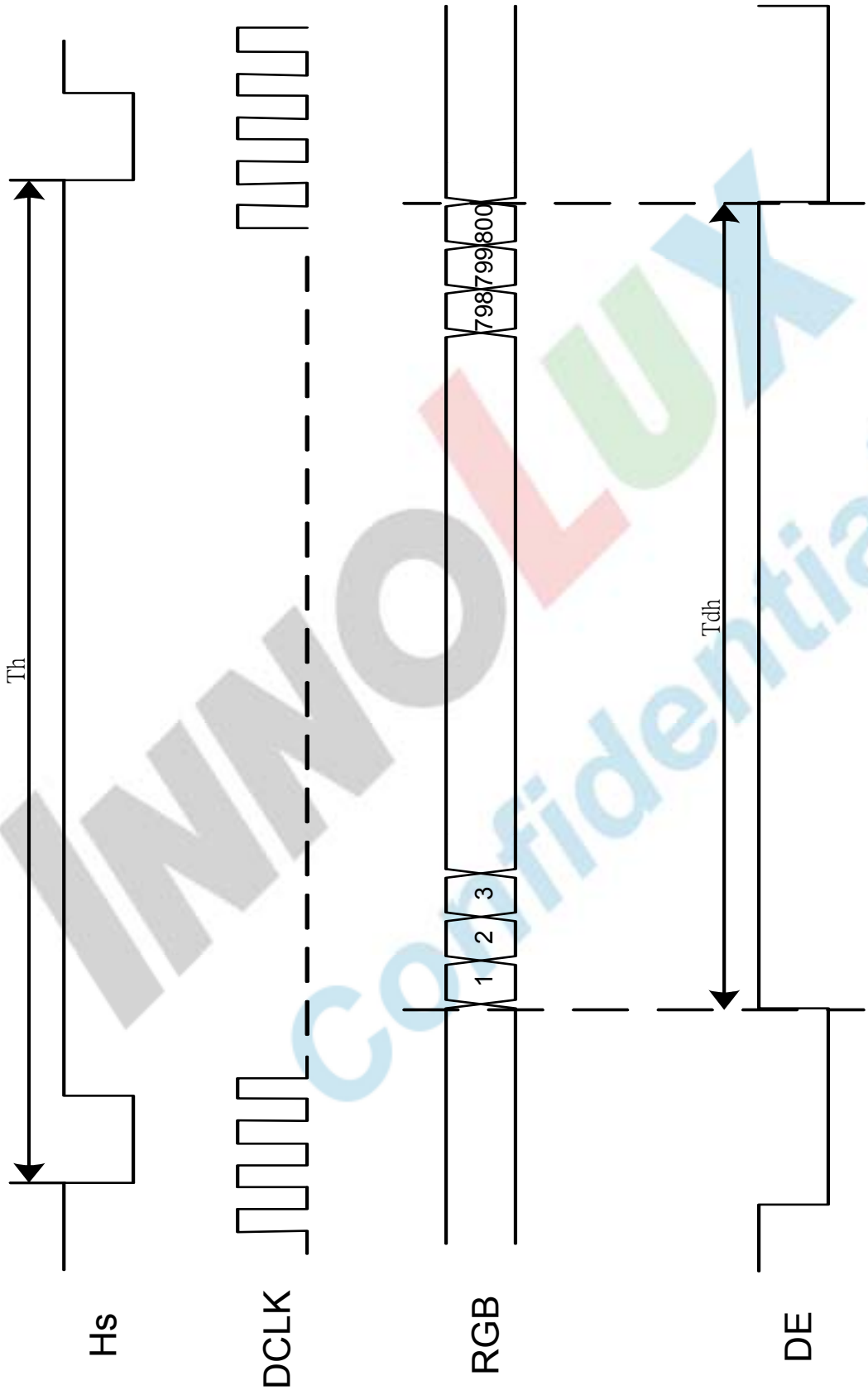


Fig.3-4 Horizontal timing 2

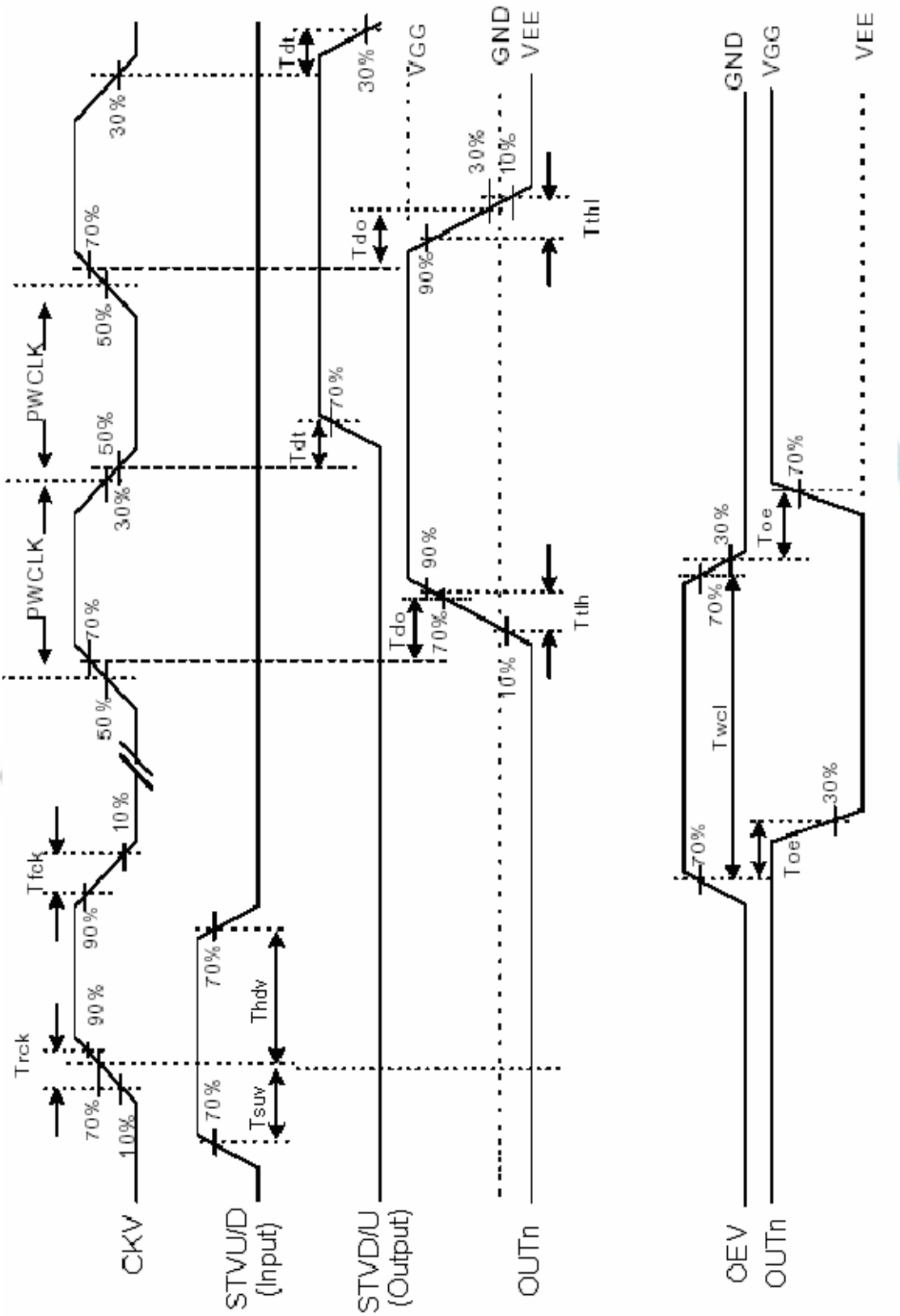


Fig.3-5 Vertical shift clock timing

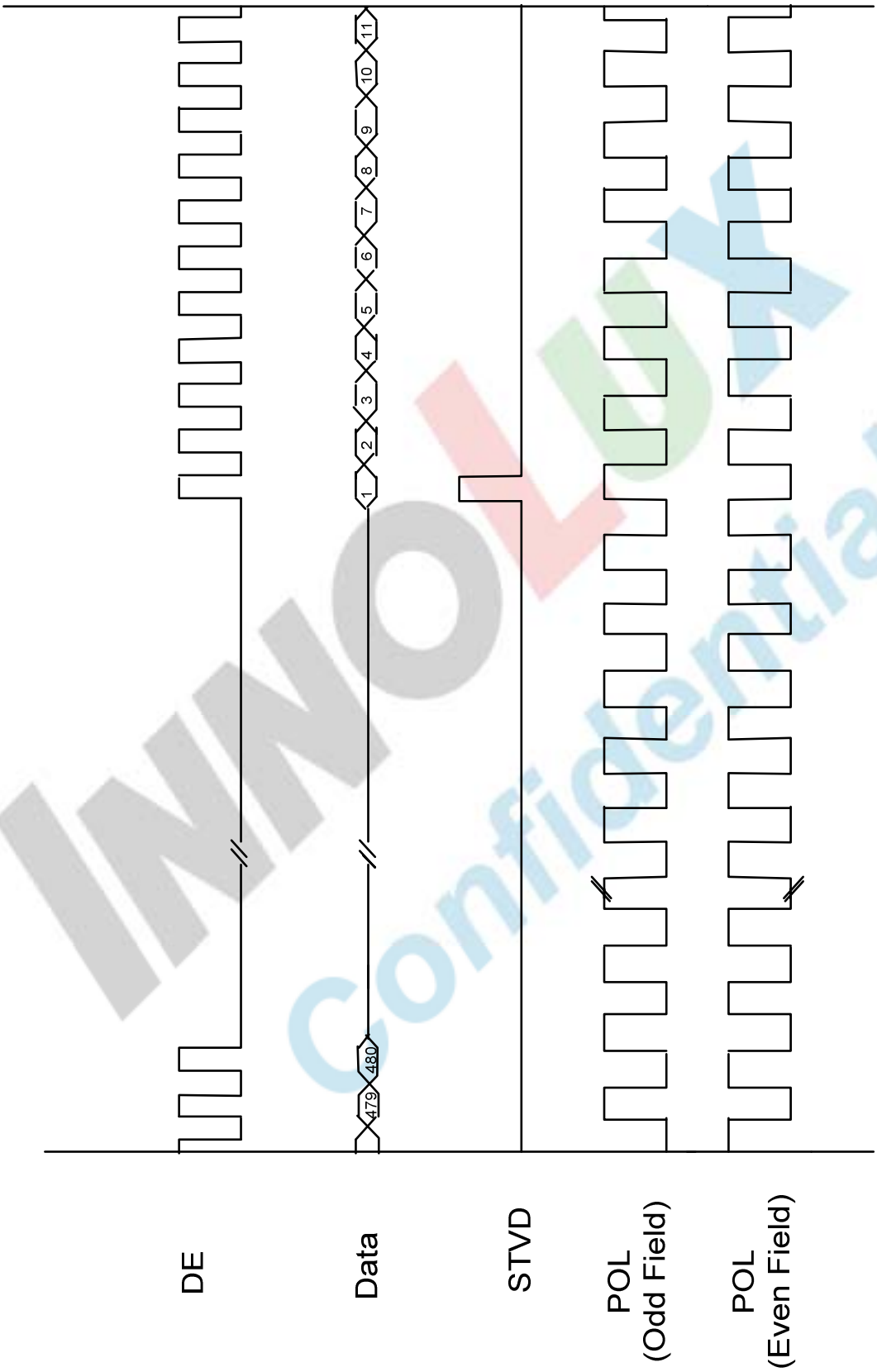


Fig.3-6 Vertical timing (from up to down)

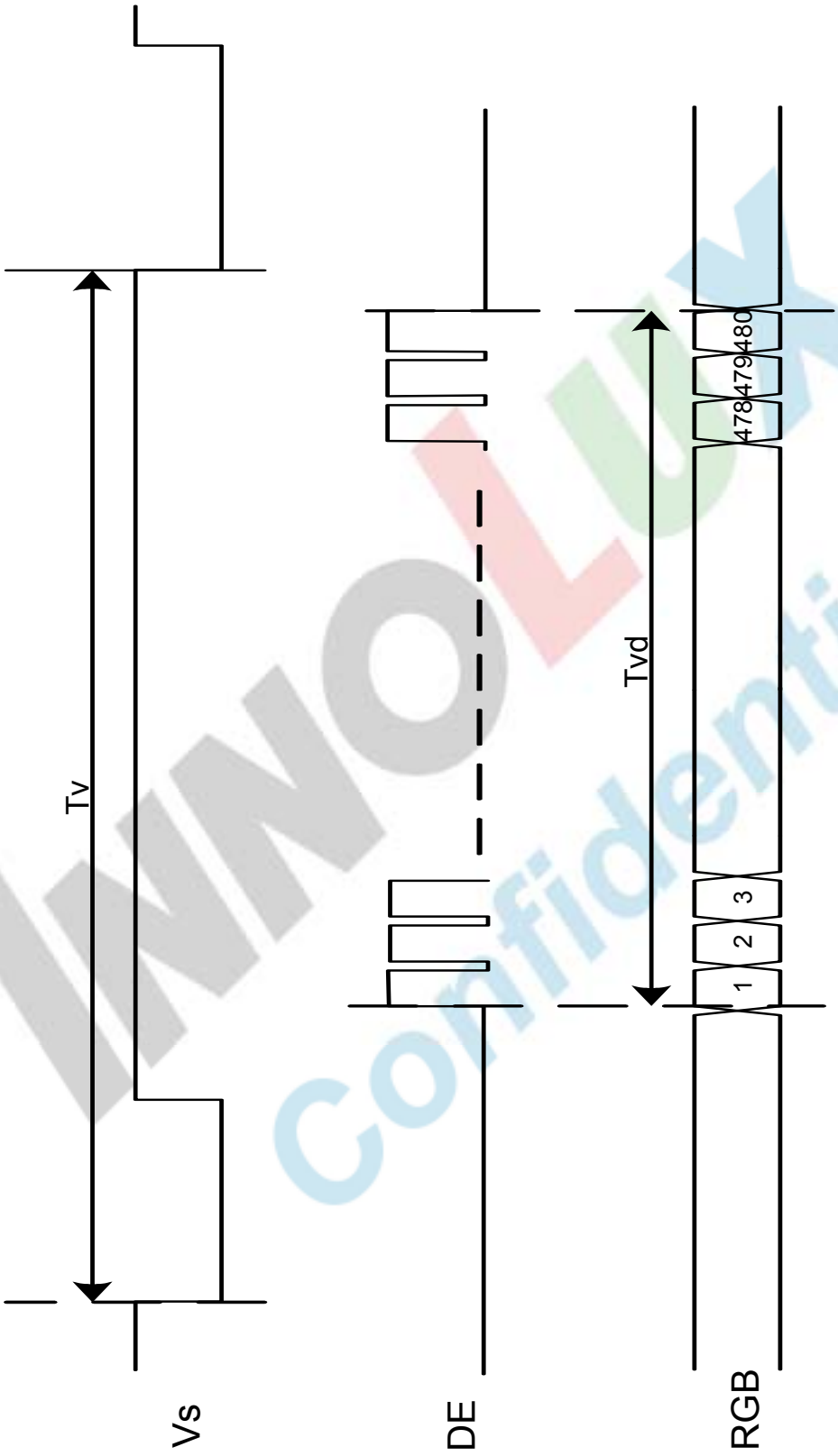


Fig.3-7 Vertical timing

4. Optical Specifications

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing angle (CR≥ 10)	θ_L	Φ=180°(9 o'clock)	60	70	-	degree	Note 1
	θ_R	Φ=0°(3 o'clock)	60	70	-		
	θ_T	Φ=90°(12 o'clock)	40	50	-		
	θ_B	Φ=270°(6 o'clock)	60	70	-		
Response time	T_{ON}	Normal θ=Φ=0°	-	10	20	msec	Note 3
	T_{OFF}		-	15	30	msec	Note 3
Contrast ratio	CR		400	500	-	-	Note 4
Color chromaticity	W_X		0.26	0.31	0.36	-	Note 2 Note 5 Note 6
	W_Y		0.28	0.33	0.38	-	
Luminance	L		160	200	-	cd/m^2	Note 6
Luminance uniformity	Y_U		70	75	-	%	Note 7

Test Conditions:

1. DV_{DD} =3.3V, I_L =180mA (Backlight current), the ambient temperature is 25℃.
2. The test systems refer to Note 2.

Note 1: Definition of viewing angle range

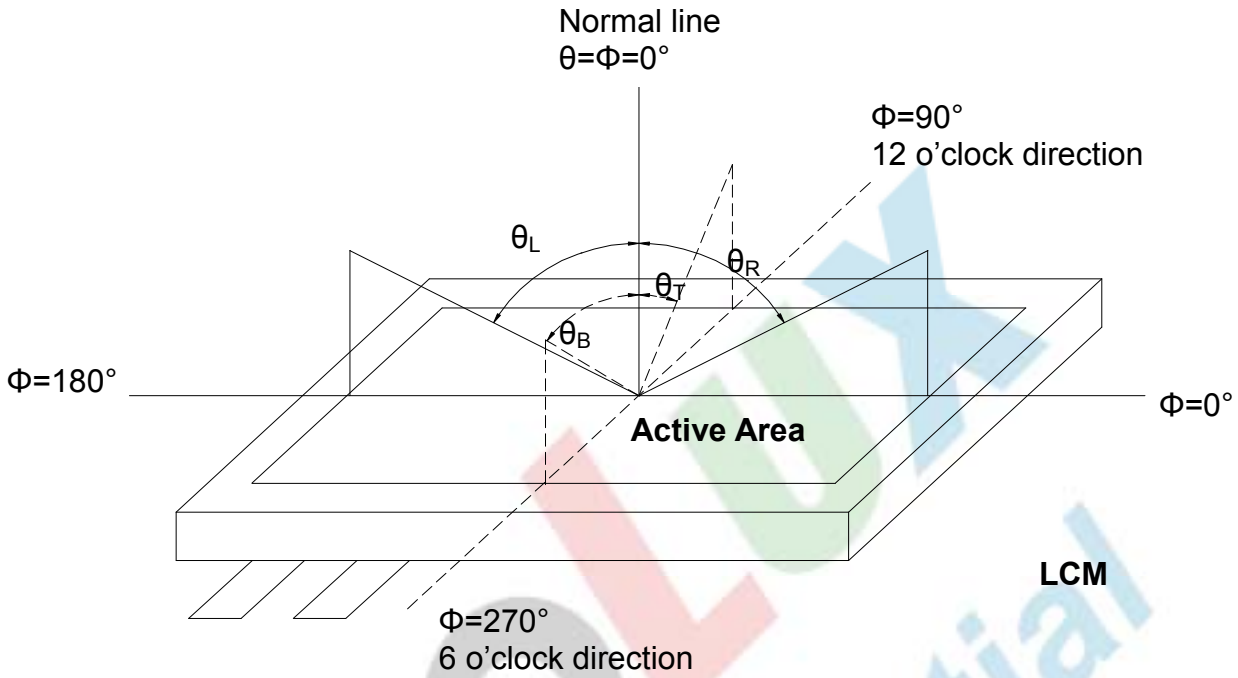


Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.
The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/Field of view: 1° /Height: 500mm.)

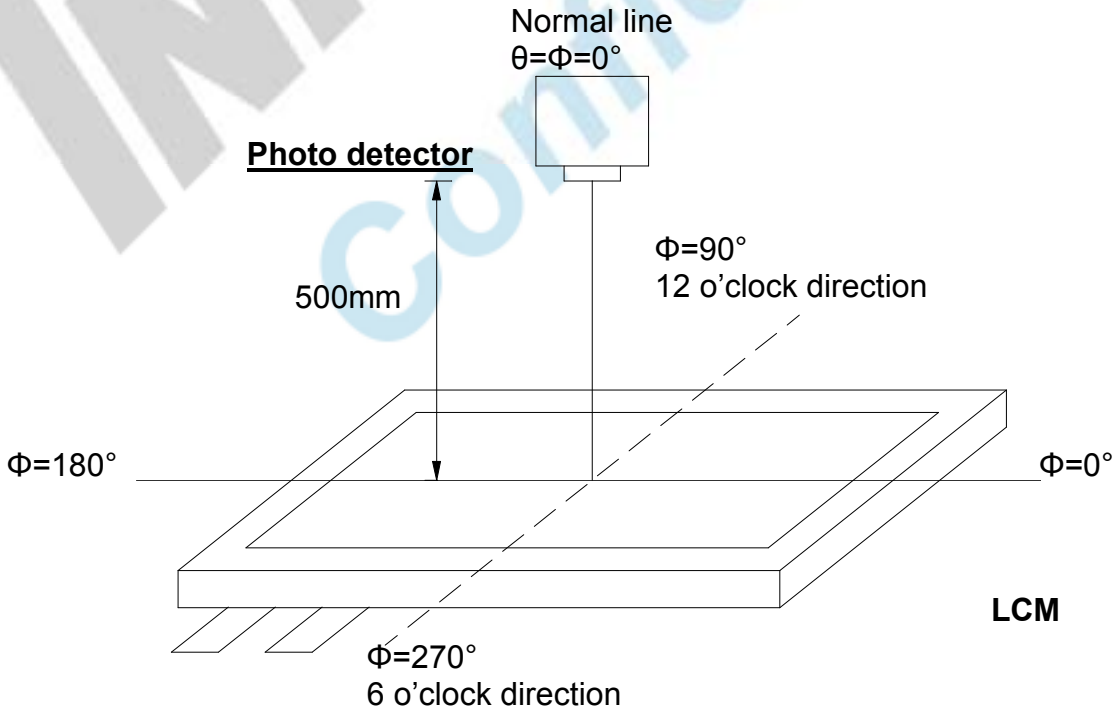


Fig. 4-2 Optical measurement system setup

Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

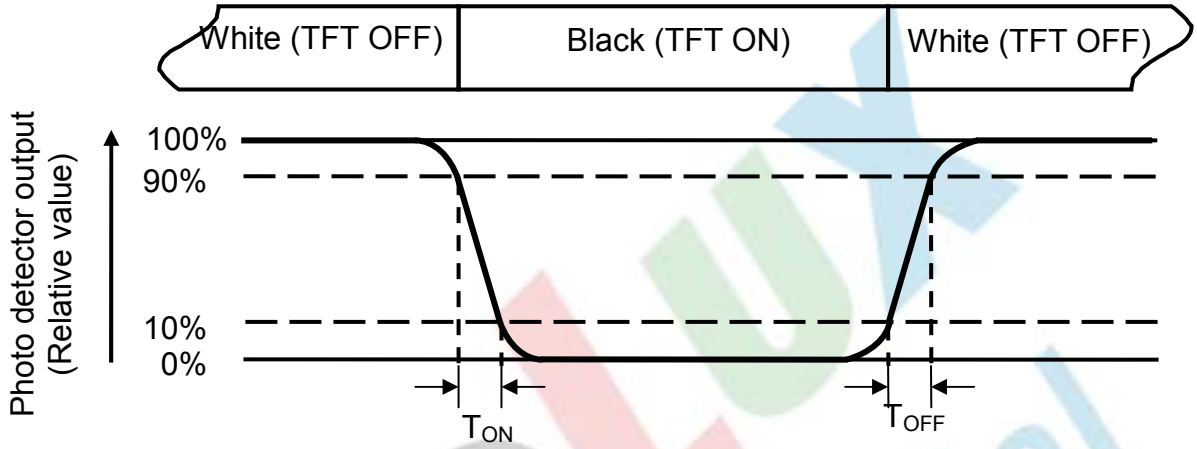


Fig. 4-3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel. The LED driving condition is I_L=180mA .

Note 7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to Fig. 4-4).Every measuring point is placed at the center of each measuring area.

$$Luminance\ \ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

L-------Active area length W----- Active area width

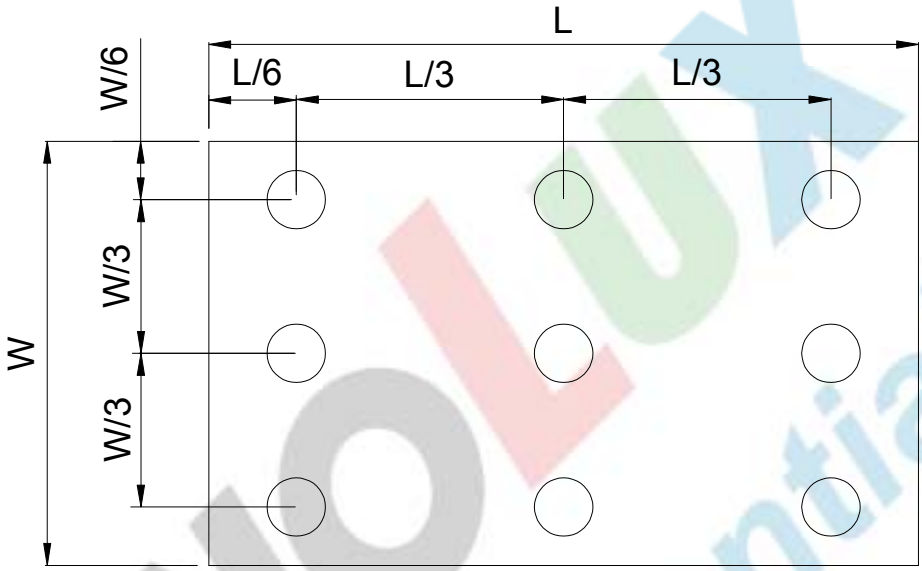


Fig. 4-4 Definition of measuring points

B_{max}: The measured maximum luminance of all measurement position.
B_{min}: The measured minimum luminance of all measurement position.

5. Reliability Test Items

(Note3)

Item	Test Conditions	Remark
High Temperature Storage	Ta = 85℃ 240 hrs	Note 1,Note 4
Low Temperature Storage	Ta = -30℃ 240hrs	Note 1,Note 4
High Temperature Operation	Ts = 85℃ 240hrs	Note 2,Note 4
Low Temperature Operation	Ta =-30℃ 240hrs	Note 1,Note 4
Operate at High Temperature and Humidity	+60℃, 90%RH max. 240 hrs	Note 4
Thermal Shock	-30℃/30 min ~ +85℃/30 min for a total 100 cycles, Start with cold temperature and end with high temperature	Note 4
Vibration Test	Frequency range:10~55Hz Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X. Y. Z. (6 hours for total)	
Mechanical Shock	100G 6ms,±X, ±Y, ±Z 3 times for each direction	
Package Vibration Test	Random Vibration : 0.015G*G/Hz from 5-200HZ, -6dB/Octave from 200-500HZ 2 hours for each direction of X. Y. Z. (6 hours for total)	
Package Drop Test	Height:60 cm 1 corner, 3 edges, 6 surfaces	
Electro Static Discharge	± 2KV, Human Body Mode, 100pF/1500Ω	

Note 1: Ta is the ambient temperature of samples.
Note 2: Ts is the temperature of panel's surface.
Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.
Note 4: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

6. General Precautions

6.1. Safety

Liquid crystal is poisonous. Do not put it in your mouth. If liquid crystal touches your skin or clothes, wash it off immediately by using soap and water.

6.2. Handling

1. The LCD panel is plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
2. The polarizer attached to the display is easily damaged. Please handle it carefully to avoid scratch or other damages.
3. To avoid contamination on the display surface, do not touch the module surface with bare hands.
4. Keep a space so that the LCD panels do not touch other components.
5. Put cover board such as acrylic board on the surface of LCD panel to protect panel from damages.
6. Transparent electrodes may be disconnected if you use the LCD panel under environmental conditions where the condensation of dew occurs.
7. Do not leave module in direct sunlight to avoid malfunction of the ICs.

6.3. Static Electricity

1. Be sure to ground module before turning on power or operating module.
2. Do not apply voltage which exceeds the absolute maximum rating value.

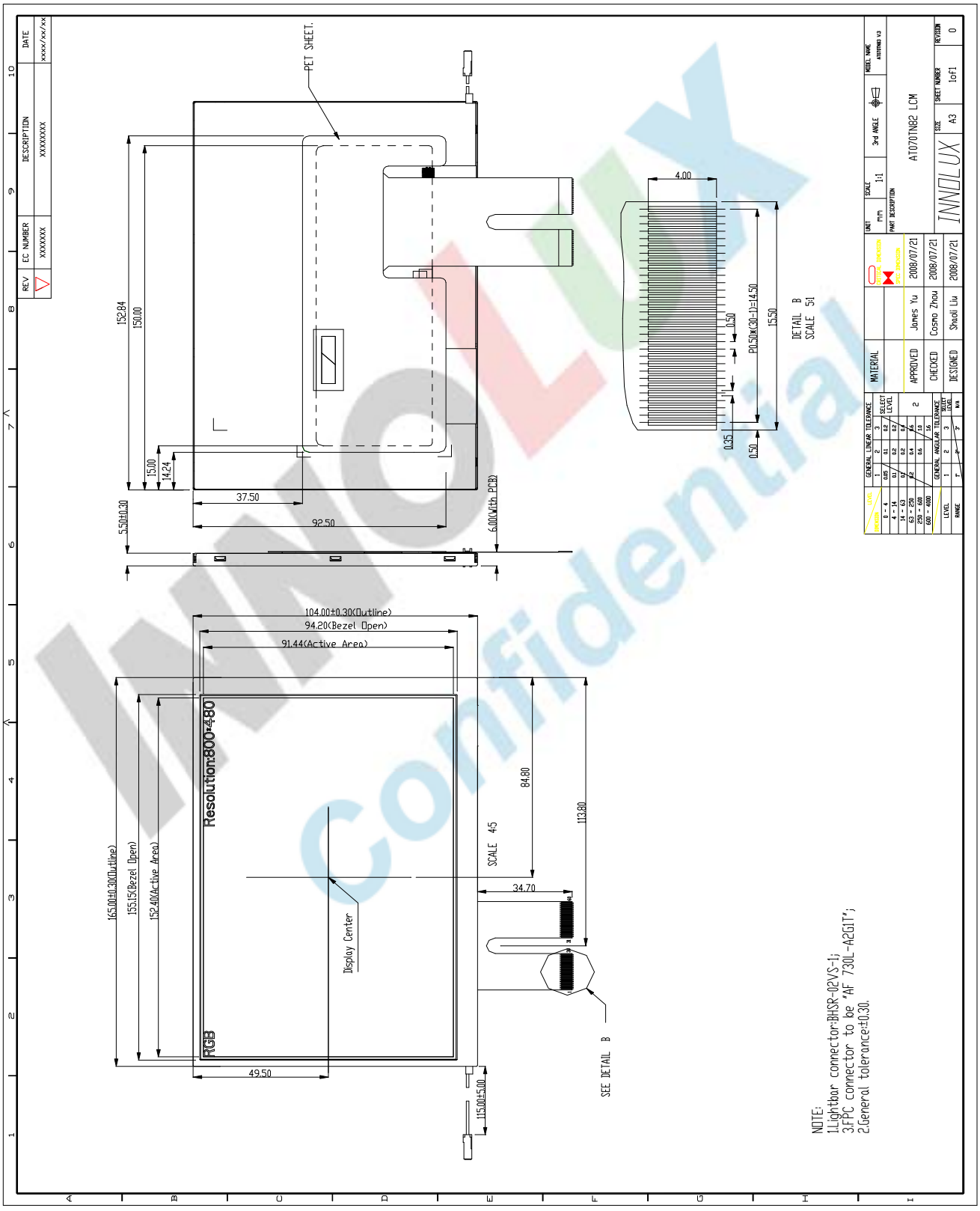
6.4. Storage

1. Store the module in a dark room where must keep at 25±10℃ and 65%RH or less.
2. Do not store the module in surroundings containing organic solvent or corrosive gas.
3. Store the module in an anti-electrostatic container or bag.

6.5. Cleaning

1. Do not wipe the polarizer with dry cloth. It might cause scratch.
2. Only use a soft sloth with IPA to wipe the polarizer, other chemicals might permanent damage to the polarizer.

7. Mechanical Drawing



8. Package Drawing

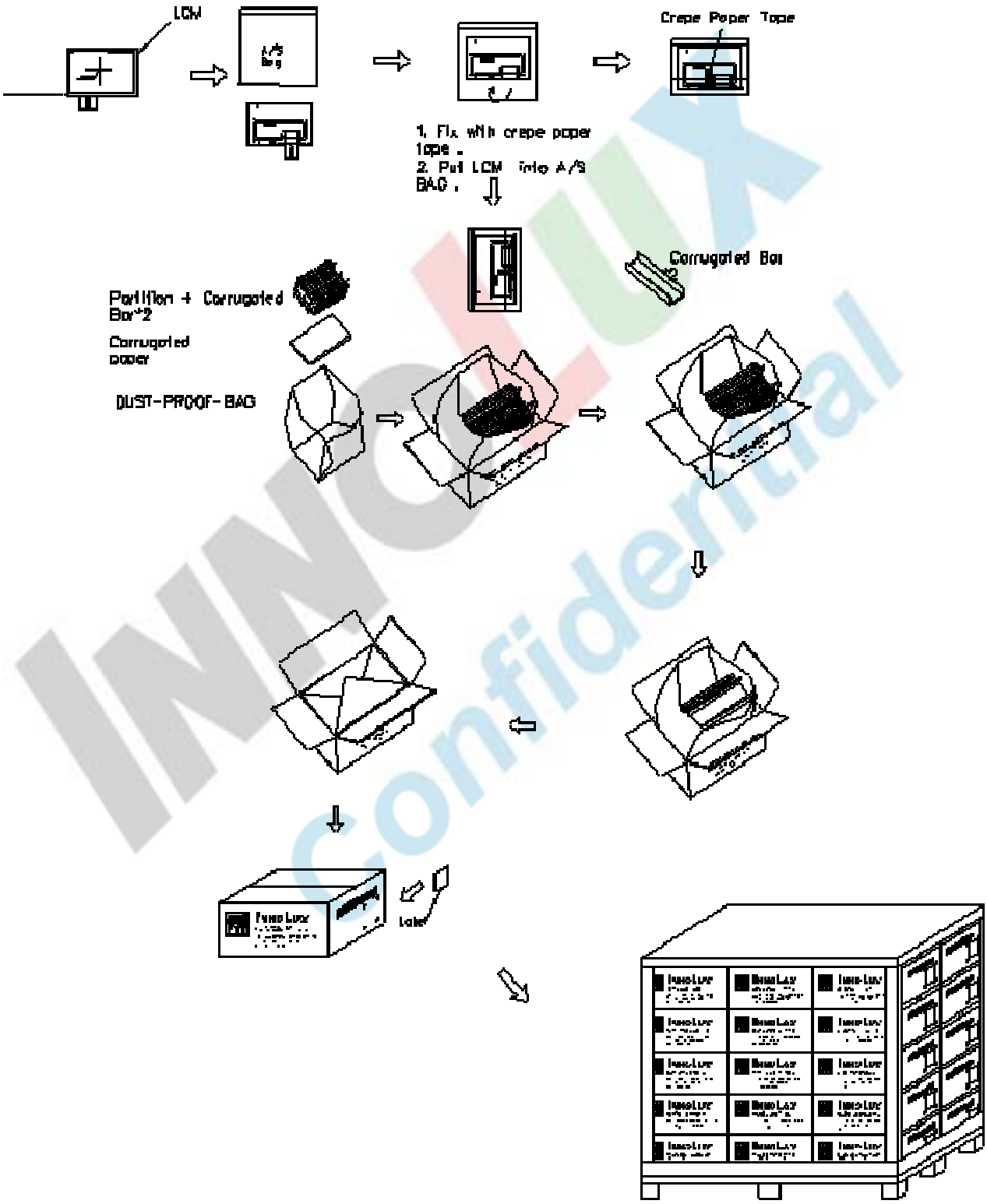
8.1. Packaging Material Table

No.	Item	Model (Material)	Dimensions(mm)	Unit Weight (kg)	Quantity	Remark
1	LCM Module	AT070TN82	165 × 104 × 5.5	TBD	50pcs	
2	Partition	BC Corrugated Paper	512 × 349 × 226	1.466	1 set	
3	Corrugated Bar	BC Corrugated Paper	512 × 162	0.046	4 set	
4	Corrugated Board	BC Corrugated Paper	510 × 343	0.130	1pcs	
5	Dust-Proof Bag	PE	700 × 530	0.048	1 pcs	
6	A/S Bag	PE	180 × 160 × 0.05	0.002	50 pcs	
7	Carton	Corrugated paper	530 × 355 × 255	1.100	1 pcs	
8	Total weight	TBD				

8.2. Packaging Quantity

Total LCM quantity in Carton: no. of Partition 2 Rows x quantity per Row 25 = 50

8.3. Packaging Drawing



AML 6210DP A/V Processor User's Guide

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www.amlogic.com

Table of Contents

Revision History

Revision Number	Revised Date	By	Changes
0.1	2008/3/3	bwester	Initial release
0.2	2008/3/3	Bwester	Fix some errors in diagram and text

1 Introduction

The AML6210DP A/V processor is a complete integrated system targeting the digital picture frame market. The device combines a super fast JPEG decoder, all digital LCD drivers/TCON signals, USB and card-reader I/Os and a 32-bit host CPU in a small 144 pin package.

The embedded 32-bits core CPU handles all system related application software. It executes AVOS, the base operating system for AML6210DP. All applications and drivers run on top of AVOS. Drivers including USB drivers, card-reader hardware driver, and video and other hardware related programming interfaces are provided by AVOS. Applications include graphical user interfaces and file system sub-system are also included. Developers can add additional applications to customize for each platform.

The core CPU interfaces to the video and audio processing hardware. It performs advanced digital audio decoding. It provides support for all existing audio formats and it also has enough flexibility to accommodate new audio standards. Popular audio formats like MPEG Layer I/II/III, LPCM, MP3, WMA, AAC and WAV can be supported.

JPEG pictures are processed by dedicated picture decoding hardware and the flexible Picture AMRISC™ engine. The hardware and microcode combination is capable of decoding JPEG pictures with no limits in picture resolution. Once decoded, the output pictures are passed to a sophisticated video sub-system that performs image analysis, enhancement and scaling functions. Contrast enhancement, hue adjustment, video scaling, video interpolation, and zoom are also supported. The high-resolution scalar supports both up-scaling and down-scaling of images and video. The scalar can also mix in multiple graphics and OSD layers for the final display. The integrated video encoder supports all digital LCD panel resolutions thru the on-chip triple panel DACs. In addition, a programmable digital LCD TCON is included for the AML6210DP to interface to digital LCD panels directly.

The AML6210DP also integrated a USB 2.0 High Speed OTG controller/PHY and card-reader controller. The card-reader controller can support SD/SDHC, MS/MS-Pro/MS-Duo/MS-Pro Duo, MMC, xD and CF cards. FAT and FAT32 file systems are supported. The USB controller can be connected to USB hard disk, FLASH drive, digital cameras and MP3 players. The AVOS drivers and applications for AML6210DP firmware includes the basic USB device driver, USB protocol stacks to support bulk and INTR transfer, Hub, Mass-Storage (MS) class and Picture Transfer Protocol (PTP). The AVOS USB firmware also supports multiple file systems and includes flexible file transfer functions between USB devices.

AML6210DP A/V processor has a set of very flexible clocking circuits that implement the adaptive AMPOWER-II power reduction algorithms. The chip works in conjunction with the AVOS software to reduce total power consumption based on processing load, type of media streams being processed and the output requirements. With AMPOWER-II, the system can reduce power consumption for portable applications and helps consumer electronics to achieve the Energy Star rating. In addition, AMPOWER-II also provides higher performance within smaller, thermally constrained environments.

2 Features

The AML6210DP chip is very flexible and most of the capabilities are under firmware control. The following list of features may or may not be included in the firmware library or binary, depending on the actual application and platform.

- **High Integration**
  - Embedded 32-bits core RISC processor for system control
  - Complete JPEG decoding logic and video scaling logic
  - Complete audio decoding and stereo audio DACs
  - Integrated digital LCD video signals and TCON
  - Integrated USB 2.0 High Speed OTG port
  - Integrated card reader controllers
  - Integrated NAND FLASH controller

- **JPEG Decoding**
  - Super fast hardware decoding of JPEG picture
  - Unlimited pixel resolution (currently test with 16M pixel pictures)
  - Supports scaling (zoom in or out), rotation and transition effects
  - Automatic image analysis and enhancement

- **Other Images/Pictures Decoding**
  - Decodes BMP, PNG, GIF, TIFF and other popular picture formats
  - Supports zoom in and out, rotation and transition effects

- **Special Trick Modes:**
  - Pause
  - Reverse playback
  - Multiple steps fast forward/backward

- **Picture Processing**
  - Automatic image analysis and enhancement
  - Variable steps picture zooming (up to 8x)
  - On-Screen-Display (OSD) capable of supporting 4/16/256 colors or True-Color
  - OSD alpha-blending over video display

- **TV Encoder / TCON**
  - Digital video output signals especially for digital LCD panels
  - Programmable tint, brightness and other TV enhancements
  - Integrated programmable timing controller (TCON) for digital LCD panels

- **Graphics**
  - Graphics can be scaled independently of the video output
  - Unified graphics memory architecture for maximum flexibility and system cost savings

- **Audio Decoding**
  - Full MPEG audio layers I, II and III
  - Capable of decoding popular audio formats including: MP3, WMA and WAV

- **Audio Post Processing and Output**
  - Integrated a 2-channel audio DACs
  - Muting, volume control, etc.

- **USB Interface**
  - Integrated OTG 2.0 High Speed controller and PHY
  - Backward compatible with USB 1.1 devices
  - USB OTG port can be configured as USB device, host or OTG port

- DMA support for data movement for BULK, INTR and ISO transfer
- USB device driver, native USB protocol stack supported in AVOS firmware
- Integrated support for Mass-storage class (MS-Class) and Picture Transfer Protocol (PTP)
- USB Hub support
- Audio and image decoding from USB attached MS-Class or PTP devices
- Connecting to PCs or Apple computers as USB MS-Class devices

➢ **Card Reader Interfaces and Controllers**
- Support MS, SD/SDHC, MMC, and xD memory card formats
- Supports reading and play back of audio and picture multimedia files
- AVOS software supports all file operations via file system on each memory card

➢ **Core CPU Sub-system**
- 32-bit core CPU dedicated for user applications
- Embedded debug interface using ICE/JTAG
- Shared MPEG SDRAM as run time data storage for minimal system cost
- Integrated interrupt controller
- Integrated general purpose timers and counters
- Integrated general purpose DMA controllers
- Supports up to 8M bytes of 8-bit FLASH chip
- Supports single SDRAM interface (m1_*). The SDRAM interface can support 8M or 16M bytes of SDRAM.

➢ **System, Peripherals and Misc. Interfaces**
- One 27 MHz crystal oscillator for A/V system
- AMPOWER-II power reduction algorithm for portable devices
- Numerous programmable GPIO pins for system control and interrupts
- Integrated i2c master controllers, remote control input circuitry, quad PWM output pins
- 1.2 volt and 3.3 volt power supplies
- 3.3 volt I/O support
- 144 pins LQFP RoHS package

3 External Interfaces

3.1 Global Configurations

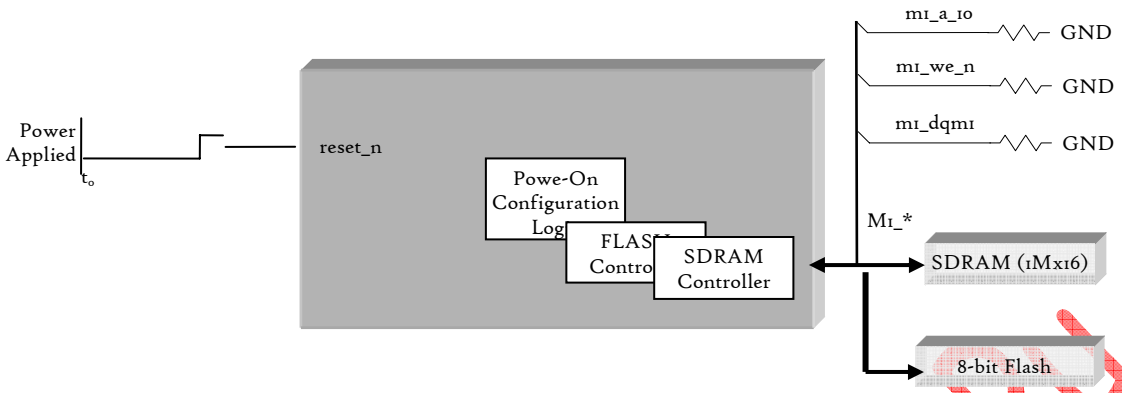
3.1.1 Power-On Configuration

The chip has a common active-low reset signal called *reset_n*. This signal puts the entire chip into a known state by resetting internal registers and state-machines to their default states. Typically this signal is held low for at least 100 msec after the power and crystal clock is stabilized. The reset process also plays a role in configuring certain functions within the chip. Using the state of the configuration pins and the rising edge of the *reset_n* signal, the user can dictate the configuration of the JTAG pins and the boot device. The configuration pins should be pulled up or down using 10K resistors to either 3.3v or ground.

PIN	Function
m1_a_10	This pin controls the **JTAG** configuration after RESET: ➢ Tie to 3.3v with 10k resistor for JTAG debugging ➢ Tie to ground with a 10k resistor to use the JTAG pins as GPIO
m1_we_n	This pin controls the **Boot Option** after RESET: ➢ Tie to 3.3v with 10k resistor if the boot device is NAND FLASH ➢ Tie to ground with a 10k resistor if the boot device is NOR FLASH
m1_dqm1	This pin controls the **FLASH Data Wide** after RESET: ➢ Tie to 3.3v with 10k resistor for 16-bit FLASH device ➢ Tie to ground with a 10k resistor for 8-bit FLASH device
m1_cas_n	This pin controls the **NAND Page Size** after RESET (only for NAND flash): ➢ Tie to 3.3v with 10k resistor for 512 bytes page size ➢ Tie to ground with a 10k resistor for 2048 bytes page size
m1_ras_n	This pin controls the **NAND Flash Size** after RESET. The pin controls the number of ALE pulses that are issued to set the ROW address. ➢ Tie to 3.3v with 10k resistor for large size NAND flash device that needs 3 ALE pulses ➢ Tie to ground with a 10k resistor for small size NAND device that needs 2 ALE pulses

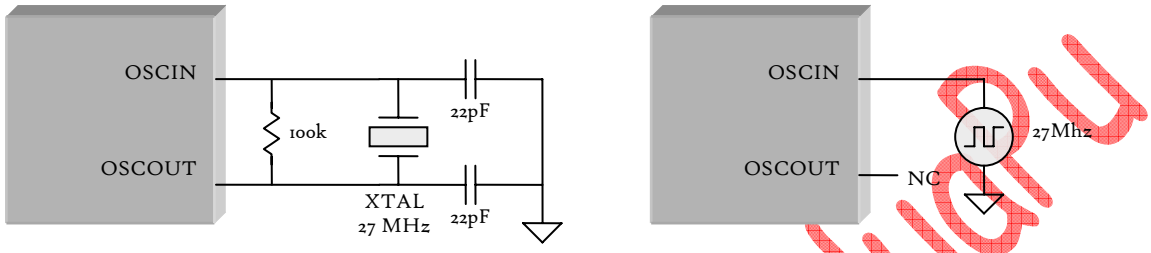
Example:

The following example illustrates a start-up configuration for a single 2M Bytes SDRAM and 8-bit FLASH memory during a production environment (i.e. no JTAG debugging). M1_a_10 is tied to GND to disable JTAG debugging; m1_we_n is tied to GND to boot from NOR FLASH; and m1_dqm1 is tied to GND for 8-bits NOR FLASH device.



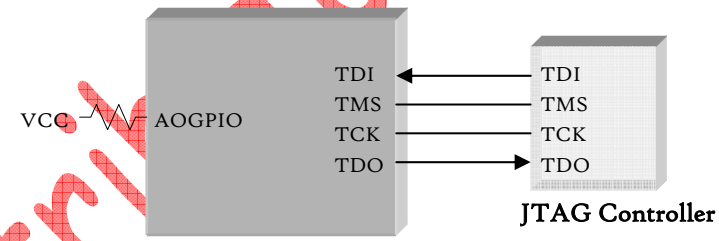
3.1.2 Clocks

The AML6210DP has multiple internal clock domains, but all the internal clock domains are derived from a single external reference: *OSC*. As illustrated below, the crystal/oscillator pin pairs (OSCIN/OSCOUT) can be connected to a crystal or driven from an external oscillator. In the typical A/V application, a 27 MHz crystal is connected to the *OSC* pins. The following diagram depicts a typical crystal circuit; the actual values of the components depend on the type of crystal used in the application.



3.1.3 JTAG for Software Development

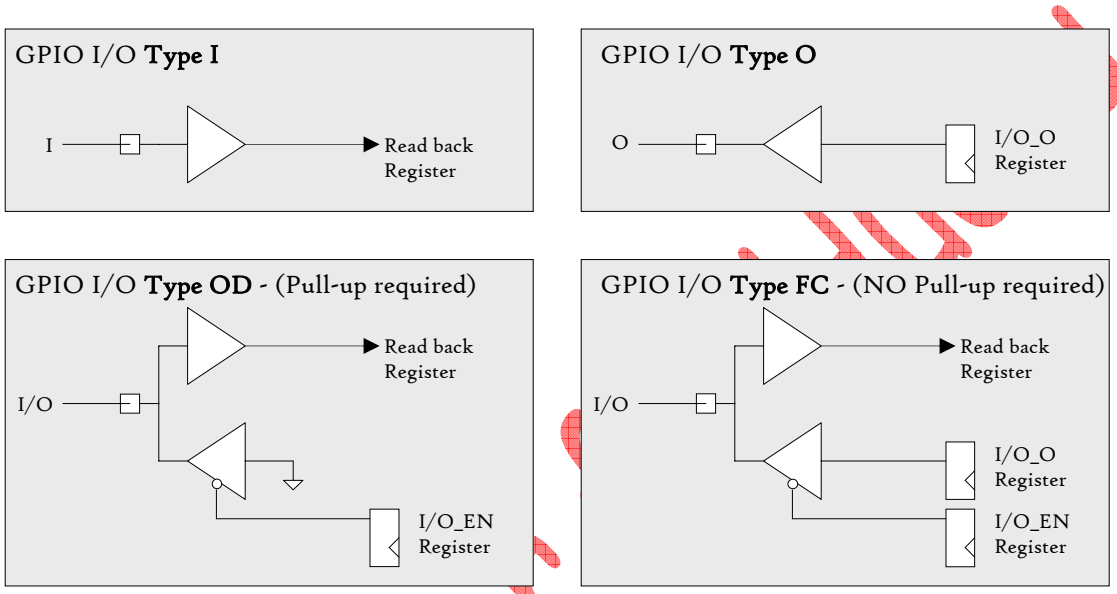
The embedded core processor can be controlled through its JTAG port using the embedded ICE interface. The embedded ICE interface allows the developer to download code/data to the SDRAM memory, probe registers on the AML6210DP chip, execute and debug the RISC code using a user friendly development environment. The JTAG interface is enabled by tying MI_A_10 high high as illustrated below.



3.1.4 GPIOs

Configurable hardware controllers (e.g. i2c, card-reader, etc.) and DMAs are integrated into the AML6210DP device to speed up the common operations and relieve the core RISC for user-level applications. Since hardware controllers and state-machines cannot cover all possible external devices or system-level signals, numerous general-purpose I/O pins are available on the chip for purpose like Portable Media Player keypads. Each GPIO pin can be independently configured to be an input or an output. As indicated in the diagram, there are various I/O types.

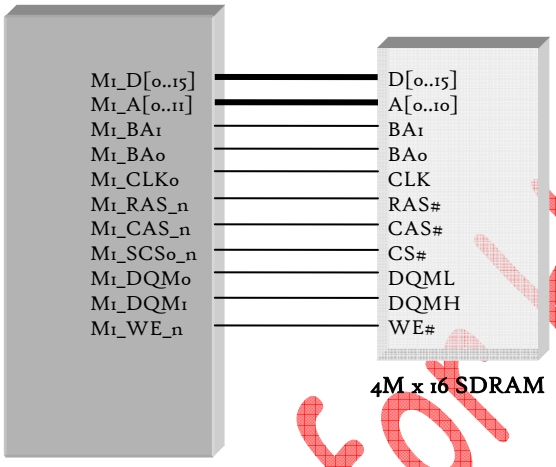
GPIO PAD TYPES



3.2 *Memory Interfaces*

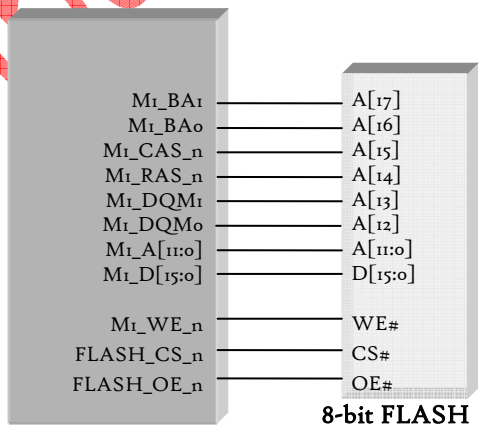
3.2.1 SDRAM Interfaces

The AML6210DP device uses external SDRAM for data storage and code execution. The SDRAM1 interface is labeled as *m1_** interface. The SDRAM interface can access up to 16M bytes of memory. Depending on the application, 166MHz 4Mx16 or 8Mx16 SDRAM chips can be used. The following example depicts a system with 8M bytes of SDRAM on m1_* interface.



3.2.2 FLASH Interface

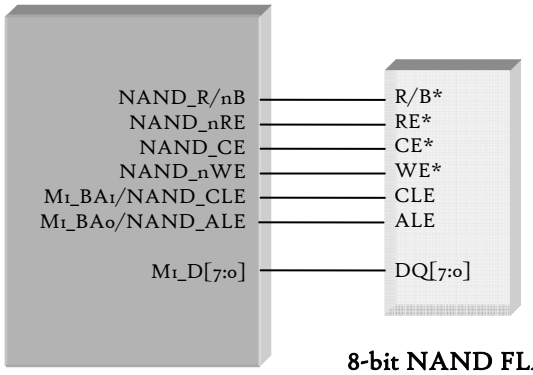
The FLASH interface can accommodate an 8-bits FLASH device. Due to the limited number of I/O pins, the FLASH interface is shared with the SDRAM (m1_*) interface. Up to 8M bytes of FLASH is accessible with the 8-bits wide FLASH interface design. The FLASH should be connected as indicated in the following diagram:



3.2.3 NAND FLASH Interface

The NAND FLASH interface can accommodate an 8-bits or 16-bits NAND FLASH device. Due to the limited number of I/O pins, the FLASH interface is shared with the SDRAM (m1_*) interface. NAND FLASH has a

very large capacity that ranges from 32MB to more than 1GB. The NAND FLASH should be connected as indicated in the following diagram:

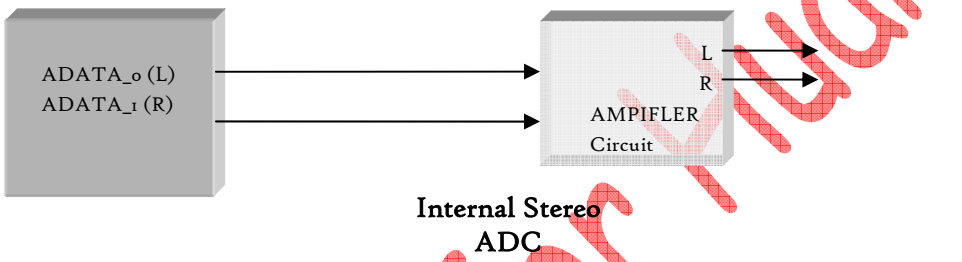


8-bit NAND FLASH

3.3 Audio Interfaces

A pair of audio DACs is provided in the AML6210DP device. The audio DACs are designed for connecting to small speaker inside the photo frame or ear buds for external listening. A simple external amplifier is needed. Please see the following sample circuit diagram.

Internally, the delta-sigma algorithm is used to improve the performance and ensure high SNR output. The implementation includes a multi-tap interpolation filter which increases the sample rate of the audio channels to the modulator rate. Then the audio stream is passed through a sigma-delta modulator that generates the serial PWM data stream. An internal analog filter is then used for out-of-band noise filtering and analog signal reconstruction. External amplifier is needed to provide the necessary current to drive the speakers or head phones.



Internal Stereo ADC

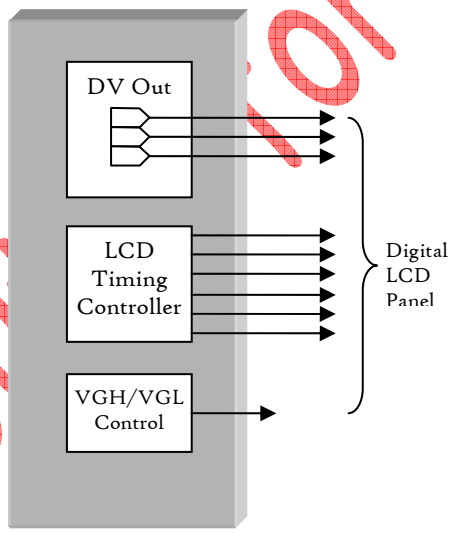
3.4 *Display Output Interfaces*

3.4.1 Digital Output

The AML6210DP integrated internal LCD video scalar and encoder and high-resolution triple panel DACs (PDAC) for direct connection to digital LCD panels. The LCD scale and encoder convert the images to the LCD resolution and prepare the image to be displayed. Then special LCD specific dithering logic and gamma correction algorithm is applied before the data is sent to the digital output.

3.4.2 LCD Timing Controller

The AML6210DP AV processor has a built-in LCD timing controller (TCON) that works in conjunction with the digital output to provide the best performance on a digital LCD panel. The TCON and digital output drive the digital LCD panel directly without any additional logic. AML6210DP's TCON is programmable and can be used in any small to medium size digital LCD panels. The LCD TCON also includes a dedicated VGH/VGL pulse generator for the LCD panel voltage generator. Together with some simple passive components, VGH/VGL can be generated.



3.5 *Peripherals*

3.5.1 Card-Reader Interface

The AML6210DP have an integrated hardware controller for SD/MS/MMC/xD card-reader operations. The hardware controller is capable of executing the low-level card interface protocols, computing the CRC or checksum, and transferring data to/from SDRAM. The hardware provides interface for the necessary signals (e.g. SD_CLK, SD_CMD, SD_Do-3 for SD cards) but signals like card detect and write-protect are provided using GPIO only.

3.5.2 USB Interface

AM6210DP AV processor has integrated one high speed USB 2.0 OTG controller and PHY into the chip. The output USB signal (DP/DM) can drive the external USB controller (e.g. Hub, FLASH drive, camera, PC, Mac, etc.) directly. The OTG controller can acts as a high speed USB Host or USB Device or a try OTG controller.

4 Operating Conditions

4.1 DC Characteristics

Table 4-1 DC Characteristics

V_{DD} = 3.3 +/- 0.3V, T_A = 0 to 65°C

Symbol	Parameters	Condition	Min	Typ	Max	Unit
V_{IH}	High Level Input		2.0		3.3	V
V_{IL}	Low Level Input		-0.3		0.8	V
VT+	Schmitt trigger, positive going Threshold			1.5		V
VT-	Schmitt trigger, negative going threshold			0.93		
Voh	High-level output voltage	Ioh = -2.0mA to 24mA	2.4			V
Vol	Low-level output voltage	Iol = 2.0 mA to 24mA			0.4	V
I_{IH}	High-level input current	Vin = V_{DD}		10nA	1	uA
I_{IL}	Low-level input current			10nA	1	
Ioz	Tri-state output leakage current			10nA	1	
P_D	Power Dissipation	Vin = V_{DD}			0.8	W

4.2 Absolute Maximum Ratings

The table below gives the absolute maximum ratings. Exposure to stresses beyond those listed in this table may result in permanent device damage, unreliability or both.

Table 4-2 Absolute Maximum Ratings

Characteristic	Value	Unit
1.2V Core Supply Voltage	1.3	V
3.3V Pads Supply Voltage	3.6	V
Input voltage, V_I	-0.5 ~ 4.6	V
Output voltage, V_O	-0.5 ~ 4.6	V
Operating Temperature	65	℃

4.3 Recommended Operating Conditions

Table 4-3 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max	Unit
$V_{DD(CORE)}$	1.2V Core Supply Voltage	1.10	1.2	1.3	V
$V_{DD(PADS)}$	3.3V Pads Supply Voltage	3.0	3.3	3.6	V
T_J	Junction Temperature	0		125	℃

5 Pin-out

The AML6210DP A/V processor pin-out is described in the following table.

Abbreviations:

- I == Input digital pin, O == Output digital pin, I/O == Input/Output pin
- AI == Analog input pin, AO == Analog output pin, AIO == Analog input/output pin
- P == Power pin, AP == Analog power pin, NC == No connection

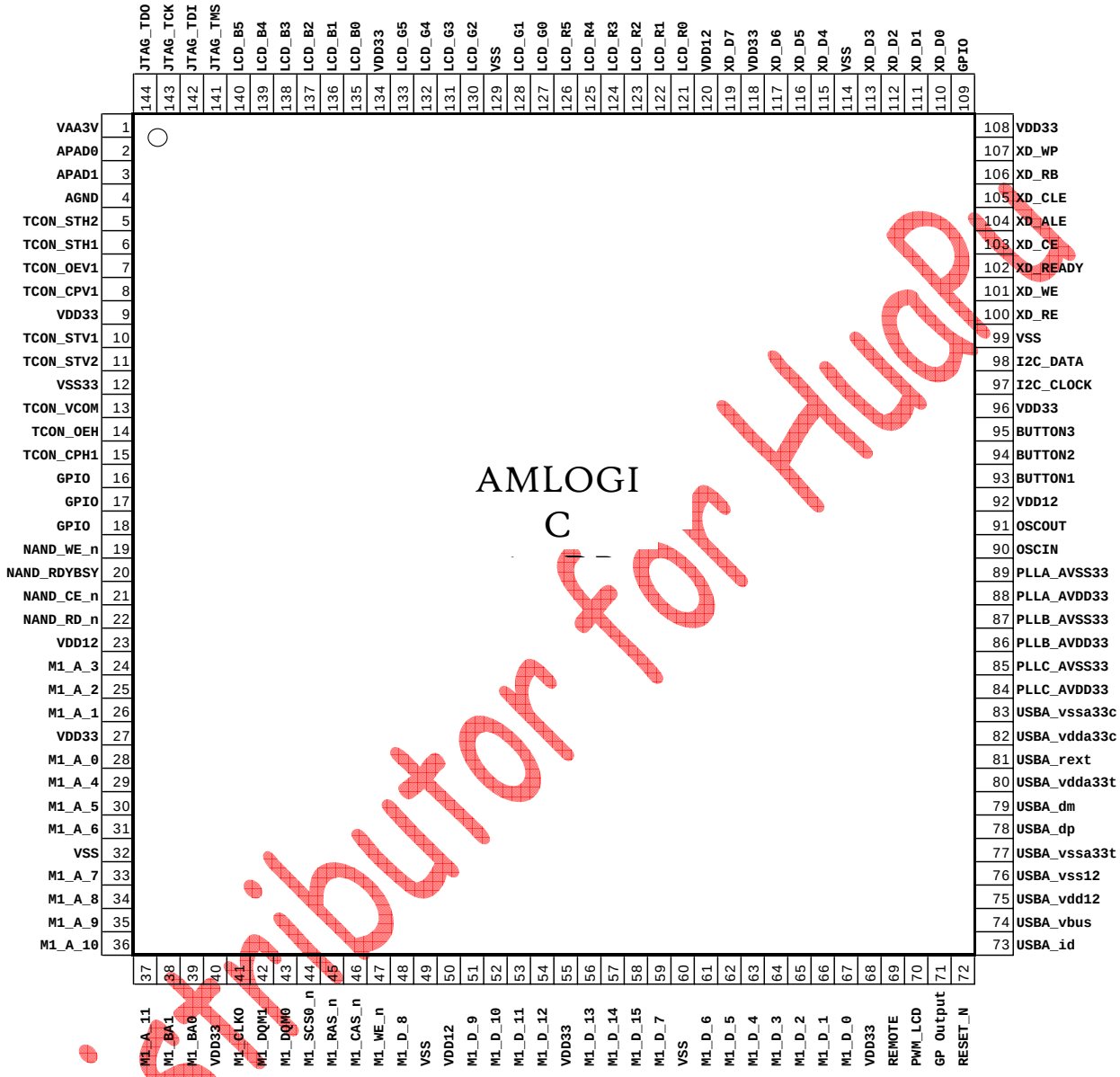
Pin #	Pin Name	Description	Alternate Usage / Comments	Type
1	VAA3V	Analog power	3.3V analog power	AP
2	APAD_0	Audio output	Audio output - LEFT	AP
3	APAD_1	Audio output	Audio output - RIGHT	AO
4	AGND	Analog ground	Analog ground	AP
5	TCON_STH2	LCD Panel signal	LCD panel clock pulse	I/O
6	TCON_STH1	LCD Panel signal	LCD panel clock pulse	I/O
7	TCON_OEV1	LCD Panel signal	LCD panel clock pulse	I/O
8	TCON_CPV1	LCD Panel signal	LCD panel clock pulse	I/O
9	VDD33	Digital I/O Power	Digital I/O 3.3V Power	P
10	TCON_STV1	LCD Panel signal	LCD panel clock pulse	I/O
11	TCON_STV2	LCD Panel signal	LCD panel clock pulse	I/O
12	VSS33	Digital Ground	Digital Ground	P
13	TCON_VCOM	LCD Panel signal	LCD panel clock pulse	I/O
14	TCON_OEH	LCD Panel signal	LCD panel clock pulse	I/O
15	TCON_CPH1	LCD Panel signal	LCD panel clock pulse	I/O
16	GPIO // XD_INS	GPIO	GPIO for card reader	I/O
17	GPIO // SD_INS	GPIO	GPIO for card reader	I/O
18	GPIO // MS_INS	GPIO	GPIO for card reader	I/O
19	NAND_WE_n	NAND Interface	NAND Interface WE	I/O
20	NAND_RDYBSY	NAND Interface	NAND Interface RDYBSY	I/O
21	NAND_CE_n	NAND Interface	NAND Interface CE	I/O
22	NAND_RD_n	NAND Interface	NAND Interface RD	I/O
23	VDD12	Digital Core Power	Digital core 1.2V power	P
24	M1_A_3	M1_A_3	SDRAM1 and/or FLASH	I/O
25	M1_A_2	M1_A_2	SDRAM1 and/or FLASH	I/O
26	M1_A_1	M1_A_1	SDRAM1 and/or FLASH	I/O
27	VDD33	Digital I/O Power	Digital I/O 3.3V power	P
28	M1_A_0	M1_A_0	SDRAM1 and/or FLASH	I/O
29	M1_A_4	M1_A_4	SDRAM1 and/or FLASH	I/O
30	M1_A_5	M1_A_5	SDRAM1 and/or FLASH	I/O
31	M1_A_6	M1_A_6	SDRAM1 and/or FLASH	I/O
32	VSS	Digital Ground	Digital ground	P
33	M1_A_7	M1_A_7	SDRAM1 and/or FLASH	I/O
34	M1_A_8	M1_A_8	SDRAM1 and/or FLASH	I/O
35	M1_A_9	M1_A_9	SDRAM1 and/or FLASH	I/O
36	M1_A_10	M1_A_10	SDRAM1 and/or FLASH	I/O

Pin	Pin name	Description	Comments / Alternate usage	Type
37	M1_A_11	M1_A_11	SDRAM1 and/or FLASH	O
38	M1_BA1	M1_BA1	SDRAM1 and/or FLASH	O
39	M1_BA0	M1_BA0	SDRAM1 and/or FLASH	O
40	VDD33	I/O Power 3.3V	Digital I/O power 3.3V	P
41	M1_CLK0	M1_CLK0	SDRAM1 and/or FLASH	O
42	M1_DQM1	M1_DQM1	SDRAM1 and/or FLASH	O
43	M1_DQM0	M1_DQM0	SDRAM1 and/or FLASH	O
44	M1_SCS0_n	M1_SCS0_n	SDRAM1 and/or FLASH	O
45	M1_RAS_n	M1_RAS_n	SDRAM1 and/or FLASH	O
46	M1_CAS_n	M1_CAS_n	SDRAM1 and/or FLASH	O
47	M1_WE_n	M1_WE_n	SDRAM1 and/or FLASH	O
48	M1_D_8	M1_D_8	SDRAM1 and/or FLASH	I/O
49	VSS	VSS	Digital ground	P
50	VDD12	Digital Core 1.2V	Digital core power 1.2V	P
51	M1_D_9	M1_D_9	SDRAM1 and/or FLASH	I/O
52	M1_D_10	M1_D_10	SDRAM1 and/or FLASH	I/O
53	M1_D_11	M1_D_11	SDRAM1 and/or FLASH	I/O
54	M1_D_12	M1_D_12	SDRAM1 and/or FLASH	I/O
55	VDD33	I/O Power 3.3V	Digital I/O power 3.3V	P
56	M1_D_13	M1_D_13	SDRAM1 and/or FLASH	I/O
57	M1_D_14	M1_D_14	SDRAM1 and/or FLASH	I/O
58	M1_D_15	M1_D_15	SDRAM1 and/or FLASH	I/O
59	M1_D_7	M1_D_7	SDRAM1 and/or FLASH	I/O
60	VSS	VSS	Digital ground	P
61	M1_D_6	M1_D_6	SDRAM1 and/or FLASH	I/O
62	M1_D_5	M1_D_5	SDRAM1 and/or FLASH	I/O
63	M1_D_4	M1_D_4	SDRAM1 and/or FLASH	I/O
64	M1_D_3	M1_D_3	SDRAM1 and/or FLASH	I/O
65	M1_D_2	M1_D_2	SDRAM1 and/or FLASH	I/O
66	M1_D_1	M1_D_1	SDRAM1 and/or FLASH	I/O
67	M1_D_0	M1_D_0	SDRAM1 and/or FLASH	I/O
68	VDD33	I/O Power 3.3V	Digital I/O power 3.3V	P
69	REMOTE	Remote	Remote Control	I
70	PWM_LCD	LCD PWM	PWM for the LCD ?	I/O
71	GP Output // LCD_PWR_EN	GPO	GPO for LCD_power control	O
72	RESET_N	Reset	Master Reset	I

Pin	Pin name	Description	Comments / Alternate usage	Type
73	USBA_id	USBA identifier	USB Mini-receptacle Identifier between mini-A/mini-B plug	AI
74	USBA_vbus	USBA mini VBUS	USB power supply pin **(5 volt)**. An off-chip charge pump is used to provide power to the VBUS pin.	AP
75	USBA_vdd12	USBA Digital 1.2V Power	Digital 1.2V power for USB-A	AP
76	USBA_vss12	USBA Digital Ground	Digital ground for USB-A	AP
77	USBA_vssa33t	USBA ground	Analog ground for USB-A transceiver	AP
78	USBA_dp	USBA D+	D+ analog signal from the USB cable	A
79	USBA_dm	USSA D-	D- analog signal from the USB cable	A
80	USBA_vdda33t	USBA 3.3V power	Analog 3.3V power for USB-A transceiver	AP
81	USBA_rext	USBA Ext Ref resistor	External resistor that controls the bias current for USB	AP
82	USBA_vdda33c	USBA 3.3V power	Analog 3.3V power for USB-A core	AP
83	USBA_vssa33c	USBA ground	Analog ground for USB-A core	AP
84	PLLC_AVDD33	PLL VDD	PLL power	AP
85	PLLC_AVSS33	PLL Ground	PLL ground	AP
86	PLLB_AVDD33	PLL VDD	PLL power	AP
87	PLLB_AVSS33	PLL Ground	PLL ground	AP
88	PLLA_AVDD33	PLL VDD	PLL power	AP
89	PLLA_AVSS33	PLL Ground	PLL ground	AP
90	OSCIN	OSC Input	27MHz crystal oscillator input	I
91	OSCOUT	OSC Output	27MHz crystal oscillator output	O
92	VDD12	Digital Core Power	Digital core 1.2V power	P
93	BUTTON_1	BUTTON_1	BUTTON or GPIO or MISC	I/O
94	BUTTON_2	BUTTON_2	BUTTON or GPIO or MISC	I/O
95	BUTTON_3	BUTTON_3	BUTTON or GPIO or MISC	I/O
96	VDD33	VDD	Digital Power 3.3V	P
97	I2C_CLOCK	GPIO	GPIO	I/O
98	I2C_DATA	GPIO	GPIO	I/O
99	VSS	VSS	Digital Ground	P
100	XD_RE	Card Reader I/O	Card Reader I/F or GPIO	I/O
101	XD_WE	Card Reader I/O	Card Reader I/F or GPIO	I/O
102	XD_READY	Card Reader I/O	Card Reader I/F or GPIO	I/O
103	XD_CE	Card Reader I/O	Card Reader I/F or GPIO	I/O
104	XD_ALE	Card Reader I/O	Card Reader I/F or GPIO	I/O
105	XD_CLE	Card Reader I/O	Card Reader I/F or GPIO	I/O
106	XD_RB	Card Reader I/O	Card Reader I/F or GPIO	I/O
107	XD_WP	Card Reader I/O	Card Reader I/F or GPIO	I/O
108	VDD33	Digital I/O Power	Digital I/O 3.3V power	P

109	GPIO	GPIO	General Purpose I/O or CARD_ENABLE	I/O
110	XD_D0	Card Reader I/O	Card Reader I/F or GPIO	I/O
111	XD_D1	Card Reader I/O	Card Reader I/F or GPIO	I/O
112	XD_D2 // SD_CMD	Card Reader I/O	Card Reader I/F or GPIO	I/O
113	XD_D3 // SD_CLK	Card Reader I/O	Card Reader I/F or GPIO	I/O
114	VSS	VSS	Digital Ground	P
115	XD_D4 // SD_D0	Card Reader I/O	Card Reader I/F or GPIO	I/O
116	XD_D5 // SD_D1	Card Reader I/O	Card Reader I/F or GPIO	I/O
117	XD_D6 // SD_D2	Card Reader I/O	Card Reader I/F or GPIO	I/O
118	VDD33	Digital I/O Power	Digital I/O 3.3V power	P
119	XD_D7 // SD_D3	Card Reader I/O	Card Reader I/F or GPIO	I/O
120	VDD12	VDD	Digital Power 1.2V	P
121	LCD_R0	LCD Video Out	LCD Video Signal Output	O
122	LCD_R1	LCD Video Out	LCD Video Signal Output	O
123	LCD_R2	LCD Video Out	LCD Video Signal Output	O
124	LCD_R3	LCD Video Out	LCD Video Signal Output	O
125	LCD_R4	LCD Video Out	LCD Video Signal Output	O
126	LCD_R5	LCD Video Out	LCD Video Signal Output	O
127	LCD_G0	LCD Video Out	LCD Video Signal Output	O
128	LCD_G1	LCD Video Out	LCD Video Signal Output	O
129	VSS	VSS	Digital Ground	P
130	LCD_G2	LCD Video Out	LCD Video Signal Output	O
131	LCD_G3	LCD Video Out	LCD Video Signal Output	O
132	LCD_G4	LCD Video Out	LCD Video Signal Output	O
133	LCD_G5	LCD Video Out	LCD Video Signal Output	O
134	VDD33	VDD	Digital Power 3.3V	P
135	LCD_B0	LCD Video Out	LCD Video Signal Output	O
136	LCD_B1	LCD Video Out	LCD Video Signal Output	O
137	LCD_B2	LCD Video Out	LCD Video Signal Output	O
138	LCD_B3	LCD Video Out	LCD Video Signal Output	O
139	LCD_B4	LCD Video Out	LCD Video Signal Output	O
140	LCD_B5	LCD Video Out	LCD Video Signal Output	O
141	JTAG_TMS	JTAG TMS	JTAG	I/O
142	JTAG_TDI	JTAG TDI	JTAG	I/O
143	JTAG_TCK	JTAG TCK	JTAG	I/O
144	JTAG_TDO	JTAG TDO	JTAG	I/O

5.1 Package pin-out diagram



5.2 Multiple function pins

Multiple usage pins are used to converse pin consumption for different features. The AML6210DP devices can be used in many different applications but each application will not utilize all the on chip features. As a result, some of the features share the same pin. Most of the multiple usage pins can be a GPIO pin also.

The following tables illustrate the applications of the multiple usage pins.

5.2.1 Card Reader interface multi-function pins

PIN#	PACKAGE PIN NAME	XD	SD	MS	GPIO
100	XD_RE	XD_RE			AT_GPIO0
101	XD_WE	XD_WE			AT_GPIO1
102	XD_READY	XD_READY			AT_GPIO2
103	XD_CE	XD_CE			AT_GPIO3
104	XD_ALE	XD_ALE			AT_GPIO6
103	XD_CLE				AT_GPIO7
110	XD_D0	XD_D0			AT_GPIO8
111	XD_D1	XD_D1			AT_GPIO9
112	XD_D2	XD_D2	SD_CMD	MS_STB	AT_GPIO10
113	XD_D3	XD_D3	SD_CLK	MS_CLK	AT_GPIO11
115	XD_D4	XD_D4	SD_D0	MS_D0	AT_GPIO12
116	XD_D5	XD_D5	SD_D1	MS_D1	AT_GPIO13
117	XD_D6	XD_D6	SD_D2	MS_D2	AT_GPIO14
119	XD_D7	XD_D7	SD_D3	MS_D3	AT_GPIO15

5.2.2 TCON Multi-Function Pins

Pin#	Package Pin Name	LCD TCON	GPIO
5	TCON_STH2	TCON_STH2	LCD_GPIO_29
6	TCON_STH1	TCON_STH1	LCD_GPIO_28
7	TCON_OEV1	TCON_OEV1	LCD_GPIO_24
8	TCON_CPV1	TCON_CPV1	LCD_GPIO_25
10	TCON_STV1	TCON_STV1	LCD_GPIO_26
11	TCON_STV2	TCON_STV2	LCD_GPIO_27
13	TCON_VCOM	TCON_VCOM	LCD_GPIO_31
14	TCON_OEH	TCON_OEH	LCD_GPIO_30
15	TCON_CPH1	TCON_CPH1/2/3	LCD_GPIO_23

5.2.3 JTAG interface multi-function pins

Pin#	Package Pin Name	JTAG	MISC	GPIO
141	JTAG_TMS	JTAG_TMS	I2C_MSTR_CLK	JTAG_GPIO_1
142	JTAG_TDI	JTAG_TDI	I2C_MSTR_DATA	JTAG_GPIO_2
143	JTAG_TCK	JTAG_TCK	UART_RX	JTAG_GPIO_0
144	JTAG_TDO	JTAG_TDO	UART_TX	JTAG_GPIO_3

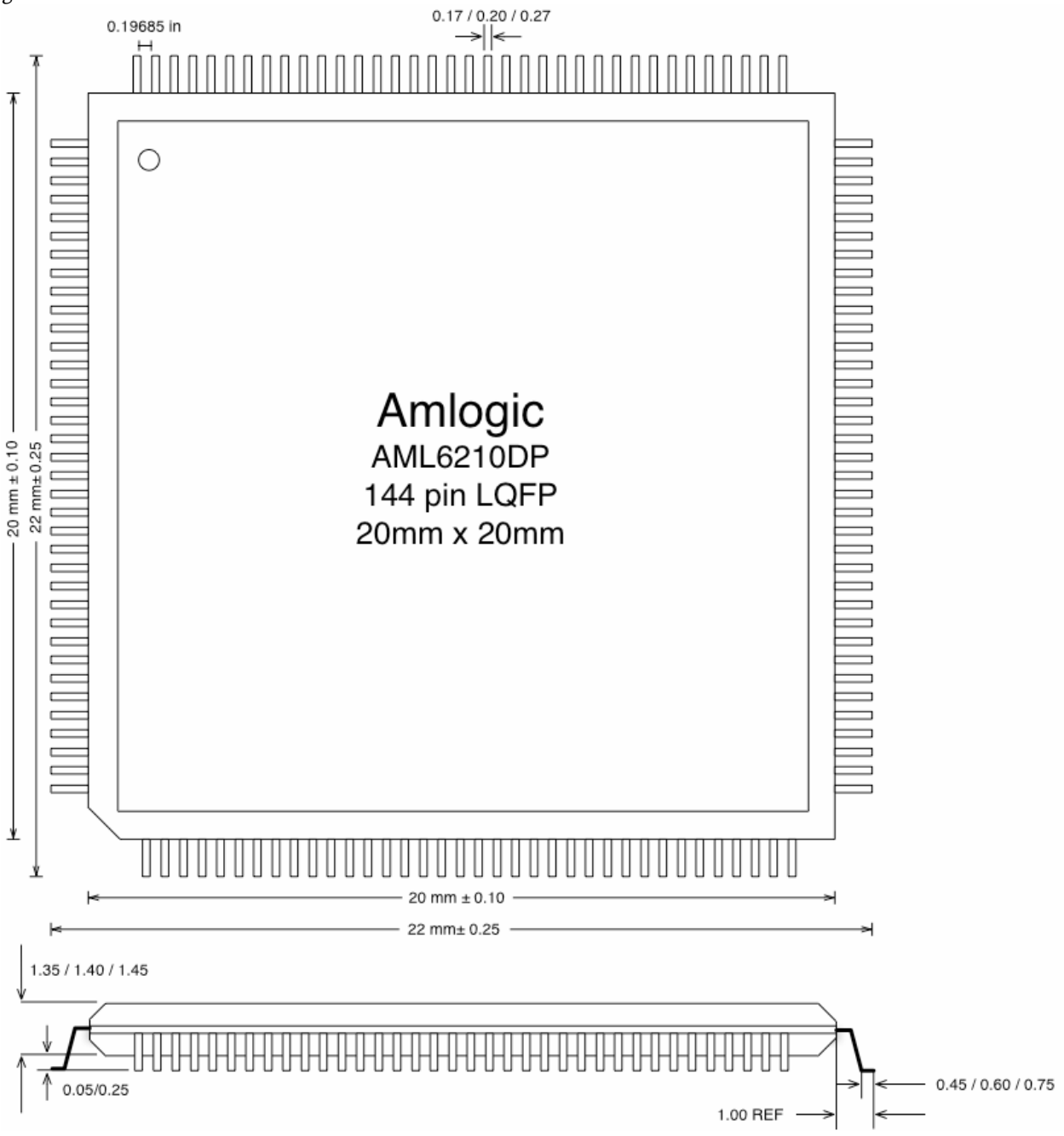
5.2.4 FLASH and m1_* interface multi-function pins

Pin#	Package Pin Name	SDRAM Memory Interface Usage (16bits wide only)	NAND FLASH Usage (8-bits wide or 16-bits wide)	NOR FLASH Usage (8-bits wide, maximum of 8Mbytes)	MISC
111	NAND_WE_n		NAND_WE_n		EGPIO_8
112	NAND_RDYBSY		NAND_RDY_BSY		EGPIO_9
113	NAND_CE_n		NAND_CE_n	FLASH_CS_n	
114	NAND_RD_n		NAND_RD_n	FLASH_OE_n	
116	M1_A_3	M1_A_3		FLASH_A_3	

117	M1_A_2	M1_A_2		FLASH_A_2	
118	M1_A_1	M1_A_1		FLASH_A_1	
120	M1_A_0	M1_A_0		FLASH_A_0	
121	M1_A_4	M1_A_4		FLASH_A_4	
122	M1_A_5	M1_A_5		FLASH_A_5	
123	M1_A_6	M1_A_6		FLASH_A_6	
125	M1_A_7	M1_A_7		FLASH_A_7	
126	M1_A_8	M1_A_8		FLASH_A_8	
127	M1_A_9	M1_A_9		FLASH_A_9	
128	M1_A_10	M1_A_10		FLASH_A_10	
1	M1_A_11	M1_A_11		FLASH_A_11	
2	M1_BA1	M1_BA1			
3	M1_BA0	M1_BA0			
5	M1_CLK0	M1_CLK0			
6	M1_DQM1	M1_DQM1		FLASH_A_21	
7	M1_DQM0	M1_DQM0		FLASH_A_20	
8	M1_SCS0_n	M1_SCS0_n			
9	M1_RAS_n	M1_RAS_n		FLASH_A_22	
10	M1_CAS_n	M1_CAS_n			
11	M1_WE_n	M1_WE_n		FLASH_WE_n	
12	M1_D_8	M1_D_8	NAND_8	FLASH_A_12	
15	M1_D_9	M1_D_9	NAND_9	FLASH_A_13	
16	M1_D_10	M1_D_10	NAND_10	FLASH_A_14	
17	M1_D_11	M1_D_11	NAND_11	FLASH_A_15	
18	M1_D_12	M1_D_12	NAND_12	FLASH_A_16	
20	M1_D_13	M1_D_13	NAND_13	FLASH_A_17	
21	M1_D_14	M1_D_14	NAND_14	FLASH_A_18	
22	M1_D_15	M1_D_15	NAND_15	FLASH_A_19	
23	M1_D_7	M1_D_7	NAND_7	FLASH_D_7	
25	M1_D_6	M1_D_6	NAND_6	FLASH_D_6	
26	M1_D_5	M1_D_5	NAND_5	FLASH_D_5	
27	M1_D_4	M1_D_4	NAND_4	FLASH_D_4	
28	M1_D_3	M1_D_3	NAND_3	FLASH_D_3	
29	M1_D_2	M1_D_2	NAND_2	FLASH_D_2	
30	M1_D_1	M1_D_1	NAND_1	FLASH_D_1	
31	M1_D_0	M1_D_0	NAND_0	FLASH_D_0	

6 Mechanical Specifications

The AML6210DP A/V processor is packaged using a 144 pins LQFP package. The mechanical dimensions are given in millimeters as below:



2Gb NAND FLASH
HY27UF(08/16)2G2B

Document Title
2Gbit (256Mx8bit) NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft.	Jul. 03. 2007	Preliminary
0.1	1) Add ULGA Package. - Figures & texts are added. 2) Change tRCBSY to tRBSY 3) Change figure 13	Sep. 11. 2007	Preliminary
0.2	1) Delete Preliminary	Jan. 09. 2008	

FEATURES SUMMARY

HIGH DENSITY NAND FLASH MEMORIES
- Cost effective solutions for mass storage applications

MULTIPLANE ARCHITECTURE
- Array is split into two independent planes. Parallel Operations on both planes are available, halving Program and erase time.

NAND INTERFACE
- x8/x16 bus width.
- Address/ Data Multiplexing
- Pinout compatiblity for all densities

SUPPLY VOLTAGE
- 3.3V device : Vcc = 2.7 V ~3.6 V

MEMORY CELL ARRAY
- x8 : (2K + 64) bytes x 64 pages x 2048 blocks
- x16 : (1K + 32) words x 64 pages x 2048 blocks

PAGE SIZE
- (2K + 64 spare) Bytes
- (1K + 32 spare) Words

BLOCK SIZE
- (128K + 4Kspare) Bytes
- (64K + 2Kspare) Words

PAGE READ / PROGRAM
- Random access : 25us (max.)
- Sequential access : 25ns (min.)
- Page program time : 200us (typ.)
- Multi-page program time (2 pages) : 200us (typ.)

COPY BACK PROGRAM
- Automatic block download without latency time

FAST BLOCK ERASE
- Block erase time: 1.5ms (typ.)
- Multi-block erase time (2 blocks) : 1.5ms (typ.)

CACHE READ
- Internal (2048 + 64) Byte buffer to improve the read throughtput.

STATUS REGISTER
- Normal Status Register (Read/Program/Erase)
- Extended Status Register (EDC)

ELECTRONIC SIGNATURE
- 1st cycle : Manufacturer Code
- 2nd cycle : Device Code
- 3rd cycle : Internal chip number, Cell Type, Number of Simultaneously Programmed Pages.
- 4th cycle : Page size, Block size, Organization, Spare size
- 5th cycle : Multiplane information

CHIP ENABLE DON'T CARE
- Simple interface with microcontroller

HARDWARE DATA PROTECTION
- Program/Erase locked during Power transitions.

DATA RETENTION
- 100,000 Program/Erase cycles (with 1bit/528byte ECC)
- 10 years Data Retention

PACKAGE
- HY27UF(08/16)2G2B-T(P)
  : 48-Pin TSOP1 (12 x 20 x 1.2 mm)
  - HY27UF(08/16)2G2B-T (Lead)
  - HY27UF(08/16)2G2B-TP (Lead Free)

- HY27UF082G2B-F(P)
  : 63-Ball FBGA (9 x 11 x 1.0 mm)
  - HY27UF082G2B-F (Lead)
  - HY27UF082G2B-FP (Lead Free)

- HY27UF082G2B-UP
  : 52-ULGA (12 x 17 x 0.65 mm)
  - HY27UF082G2B-UP (Lead Free)

1.SUMMARY DESCRIPTION

Hynix NAND HY27UF(08/16)2G2B Series have 256Mx8bit with spare 8Mx8 bit capacity. The device is offered in 3.3V Vcc Power Supply, and with x8 and x16 I/O interface Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.
The device contains 2048 blocks, composed by 64 pages. A program operation allows to write the 2112-byte page in typical 200us and an erase operation can be performed in typical 1.5ms on a 128K-byte block.

Data in the page can be read out at 25ns cycle time per byte(x8). The I/O pins serve as the ports for address and data input/output as well as command input.
This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint. Commands, Data and Addresses are synchronously introduced using $\overline{CE}$, $\overline{WE}$, $\overline{RE}$, ALE and CLE input pin. The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the $\overline{WP}$ input. The output pin R/$\overline{B}$ (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/$\overline{B}$ pins can be connected all together to provide a global status signal.

The copy back function allows the optimization of defective blocks management. When a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. Copy back operation automatically executes embedded error detection operation: 1 bit error every 528byte (x8) or 1bit error out of every 264-word (x16) can be detected. Due to this feature, it is no more nor necessary nor recommended to use external 2-bit ECC to detect copy back operation errors. Data read out after copy back read (both for single and multiplane cases) is allowed.

Even the write-intensive systems can take advantage of the HY27UF(08/16)2G2B Series extended reliability of 100K program/erase cycles by supporting ECC (Error Correcting Code) with real time mapping-out algorithm. The chip supports $\overline{CE}$ don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the $\overline{CE}$ transitions do not stop the read operation.
This device includes also extra features like OTP/Unique ID area, Read ID2 extension.

The HY27UF(08/16)2G2B Series are available in 48-TSOP1 12 x 20 mm, 63-FBGA 9 x 11mm, 52-ULGA 12 x 17 mm.

1.1 Product List

PART NUMBER	ORGANIZATION	Vcc RANGE	PACKAGE
HY27UF082G2B	x8	2.7V ~ 3.6V	48-TSOP1, 63-FBGA, 52-ULGA
HY27UF162G2B	x16		48-TSOP1

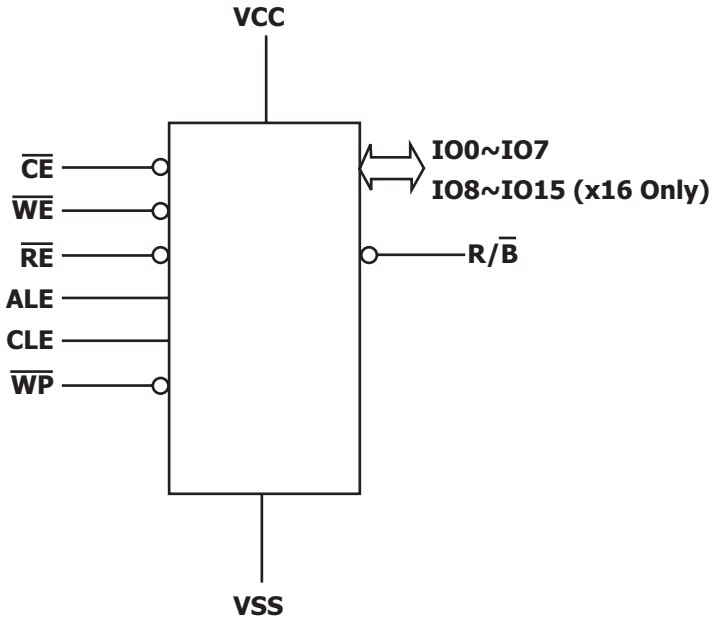


Figure1: Logic Diagram

IO15 - IO8	Data Input / Outputs (x16 only)
IO7 - IO0	Data Input / Outputs
CLE	Command latch enable
ALE	Address latch enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready / Busy
Vcc	Power Supply
Vss	Ground
NC	No Connection

Table 1: Signal Names

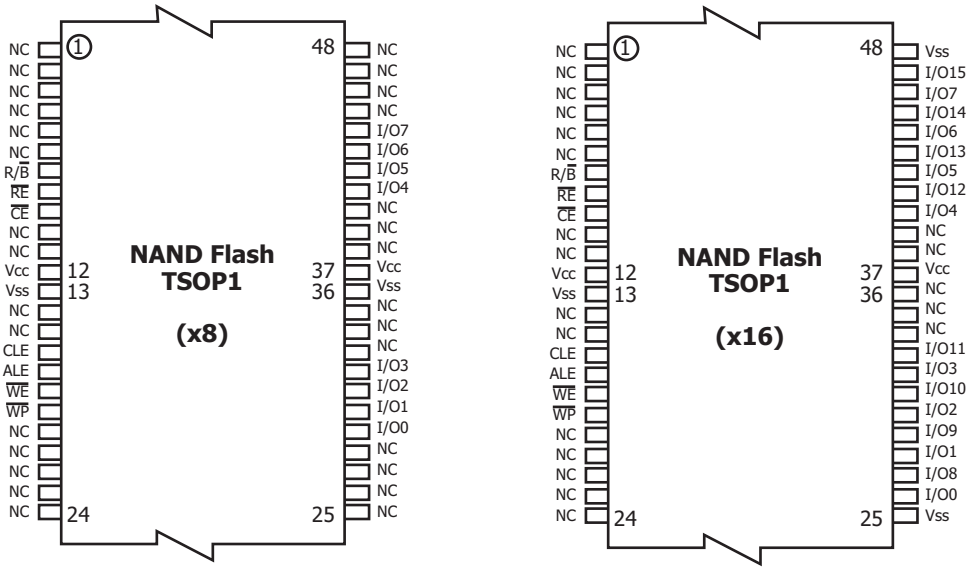


Figure 2: 48TSOP1 Contact, x8 and x16 Device

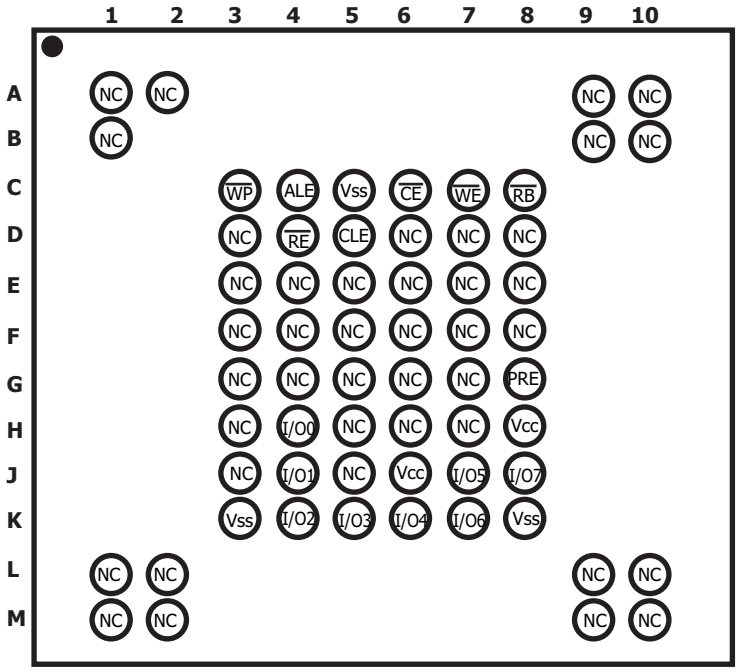


Figure 3: 63FBGA Contactions, x8 Device (Top view through package)

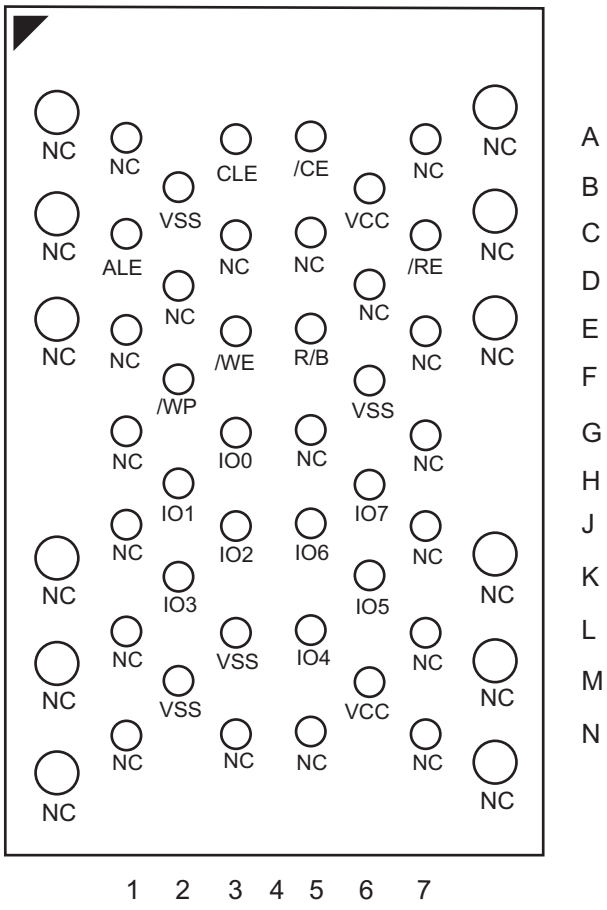


Figure 4. 52-ULGA Contactions, x8 Device (Top view through package)

1.2 PIN DESCRIPTION

Pin Name	Description
IO0-IO7 IO8-IO15(1)	**DATA INPUTS/OUTPUTS** The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable ($\overline{WE}$). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable ($\overline{WE}$).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable ($\overline{WE}$).
$\overline{CE}$	**CHIP ENABLE** This input controls the selection of the device.
$\overline{WE}$	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of $\overline{WE}$.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
R/$\overline{B}$	**READY BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
Vcc	**SUPPLY VOLTAGE** The Vcc supplies the power for all the operations (Read, Write, Erase).
Vss	GROUND
NC	NO CONNECTION

Table 2: Pin Description

NOTE:

1. For x16 version only
2. A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.
3. An internal voltage detector disables all functions whenever VCC is below 1.8V (3.3V version) to protect the device from any involuntary program/erase during power transitions.

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	L(1)	L(1)	L(1)	L(1)
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27
5th Cycle	A28	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)

Table 3: Address Cycle Map(x8)

NOTE:
1. L must be set to Low.

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7	I/O8-IO15
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	L(1)
2nd Cycle	A8	A9	A10	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18	L(1)
4th Cycle	A19	A20	A21	A22	A23	A24	A25	A26	L(1)
5th Cycle	A27	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)

Table 4: Address Cycle Map(x16)

NOTE:
1. L must be set to Low.

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
READ1	00h	30h	-	-	
READ FOR COPY-BACK	00h	35h	-	-	
READ ID	90h	-	-	-	
RESET	FFh	-	-	-	Yes
PAGE PROGRAM	80h	10h	-	-	
COPY BACK PGM	85h	10h	-	-	
MULTI PLANE PROGRAM	80h	11h	81h	10h	
MULTI PLANE COPYBACK PROGRAM	85h	11h	81h	10h	
BLOCK ERASE	60h	D0h	-	-	
MULTI PLANE BLOCK ERASE	60h	60h	D0h	-	
READ STATUS REGISTER	70h	-	-	-	Yes
RANDOM DATA INPUT	85h	-	-	-	
RANDOM DATA OUTPUT	05h	E0h	-	-	
READ CACHE (RANDOM)	00h	31h	-	-	
READ CACHE (SEQUENTIAL)	31h	-	-	-	
READ CACHE END	3Fh	-	-	-	
READ EDC STATUS REGISTER	7Bh	-	-	-	

Table 5: Command Set

Note:
1. READ EDC STATUS REGISTER is only available on Copy Back operation.

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input(5 cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input(5 cycles)
L	L	L	Rising	H	H	Data Input	
L	L	L(1)	H	Falling	X	Sequential Read and Data Output	
L	L	L	H	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc	Stand By	

Table 6: Mode Selection

NOTE:

1. With the $\overline{CE}$ high during latency time does not stop the read operation

2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.
Typically glitches less than 3ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 6 and Table 13 for details of the timings requirements. Command codes are always applied on IO7:0 regardless of the bus configuration. (x8 or x16)

2.2 Address Input

Address Input bus operation allows the insertion of the memory address. Five cycles are required to input the addresses for the 4Gbit devices. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modifying operation (write/erase) the Write Protect pin must be high. See Figure 7 and Table 13 for details of the timings requirements. Addresses are always applied on IO7:0 regardless of the bus configuration (x8 or x16).

2.3 Data Input

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serial and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure 8 and Table 13 for details of the timings requirements.

2.4 Data Output

Data Output bus operation allows to read data from the memory array and to check the status register content, the EDC register content and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See Figure 9,10,12,13,14 and Table 13 for details of the timings requirements.

2.5 Write Protect

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modifying operation does not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6 Standby

In Standby mode the device is deselected, outputs are disabled and Power Consumption is reduced.

3. DEVICE OPERATION

3.1 Page Read

This operation is operated by writing 00h and 30h to the command register along with five address cycles.
Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 2112 bytes (x8) or 1056 words (x16) of data within the selected page are transferred to the data registers in less than 25us(tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns cycle time by sequentially pulsing $\overline{RE}$. The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address.
The device may output random data in a page instead of the sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

3.2 Page Program

The device is programmed by page. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 8 times. The addressing should be done on each pages in a block. A page program cycle consists of a serial data loading period in which up to 2112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The bytes other than those to be programmed do not need to be loaded. The device supports random data input in a page.
The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s.
The command register remains in Read Status command mode until another valid command is written to the command register. Figure 16 details the sequence.

3.3 Multi Plane Program

Device supports multiple plane program: it is possible to program in parallel 2 pages, one per each plane.

A multiple plane program cycle consists of a double serial data loading period in which up to 4224bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (A<18>=0). The data of 1st page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY). Once it has become ready again, 81h command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane (A<18>=1). The data of 2nd page other than those to be programmed do not need to be loaded. Program Confirm command (10h) makes parallel programming of both pages start. User can check operation status by R/$\overline{B}$ pin or read status register command, as if it were a normal page program; status register command is also available during Dummy Busy time (tDBSY). In case of fail in 1st or 2nd page program, fail bit of status register will be set: Device supports pass/fail status of each plane. Figure 21 details the sequence.

3.4 Block Erase

The Erase operation is done on a block basis. Block address loading is accomplished in there cycles initiated by an Erase Setup command (60h). Only address A18 to A28 is valid while A12 to A17 is ignored (x8). The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase verify.

Once the erase process starts, the Read Status Register command may be entered to read the status register.

The system controller can detect the completion of an erase by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

Figure 20 details the sequence.

3.5 Multi Plane Erase

Multiple plane erase, allows parallel erase of two blocks, one per each memory plane.

Block erase setup command (60h) must be repeated two times, each time followed by 1st block and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation start. Multiplane erase does not need any Dummy Busy Time between 1st and 2nd block address insertion. Address limitation required for multiple plane program applies also to multiple plane erase, as well as operation progress can be checked like for multiple plane program. Figure 22 details the sequence

3.6 Copy-back Program

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data reloading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 2112byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register.
When the Copy-Back Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 18 & Figure 18). The command register remains in Read Status command mode until another valid command is written to the command register. During copy-back program, data modification is possible using random data input command (85h) as shown in Figure19.

Copy-back program operation is allowed only within same plane.

3.7 Multi-Plane Copy-Back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is greatly improved. The benefit is especially obvious when a portion of a block needs to be updated and the rest of the block also need to be copied to the newly assigned free block.

The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112byte data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling $\overline{RE}$ (See Figure 23), or Copy Back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 23.

Most NAND devices require 2 bit external ECC only due to copy back operation while 1 bit ECC can be enough for all other operation. Reason is that during read for copy back + copy back program sequence a bit error due to charge loss is not checked by external error detection/correction scheme. On the contrary, 2Gbit NAND includes automatic Error Detection Code during copy back operation: thanks to this, 2 bit external ECC is no more required, with significant advantage for customers that can always use single bit ECC. More details on EDC operation are available in section 3.8.

3.8 EDC Operation

Error Detection Code check automatically starts immediately after device becomes busy for a copy back program operation (both single and multiple plane). In the x8 version EDC allows detection of 1 single bit error every 528 bytes, where each 528byte group is composed by 512 bytes of main array and 16 bytes of spare area (see Table 20,21). So described 528byte area is called “EDC unit”. In the x16 version EDC allows detection of 1 single bit error every 264 words, where each 264 word group is composed by 256 words of main array and 8 words of spare area (see Table 20,21). So described 264 word area is called “ EDC unit”.

To Properly use EDC, some limitations apply:
- Random data input can be used only once in copy back program or page program or multiple page program, unless user inputs data for a whole EDC unit (or more whole EDC units).
- Any page program operation must be done on whole page basis, or on whole EDC unit (s).

EDC result can be checked only during copy back program through 7Bh (specific Read EDC register command, Table 22)

3.9 Read Status Register

The device contains a Status Register which may be read to find out whether, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 14 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random data output, the read command (00h) should be given before starting read cycles.

3.10 Read EDC Status Register

The operation is available only in copy back program and it allows the detection of errors occurred during read for copy back. In case of multiple plane copy back, it is not possible to know which of the two read operation caused the error. After writing 7Bh command to the command register, a read cycle outputs the content of the EDC Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last.
Operation is same read status register command. Refer to below Table 22 for specific EDC Register definitions.

3.11 Read ID.

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code (ADh), and the device code and 3rd, 4th, 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 24 shows the operation sequence, while tables 15 explain the byte meaning.

3.12 Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table 14 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin goes low for tRST after the Reset command is written. Refer to Figure 27.

3.13 Cache Read

Cache read operation allows automatic download of consecutive pages. Immediately after 1st latency end, while user can start reading out data, device internally starts reading following page.

Start address of 1st page is at page start (A<10:0>=00h), after 1st latency time (tr) , automatic data download will be uninterrupted. In fact latency time is 25us, while download of a page require at least 100us for x8 device. (50us for x16device).

The Cache Read function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Cache Read function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Cache Read function. Issuing an additional Cache Read function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[6]is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array.

The host shall not issue a sequential Read Cache (31h) command after the last page of the device is read.

Refer to Figure 15.

Cache Read operation must be done only block by block if system needs to avoid reading also reading from invalid blocks.

4. OTHER FEATURES

4.1 Data Protection & Power On/Off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2.0V(3.3V device). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences as shown in Figure 28. The two-step command sequence for program/erase provides additional software protection.

4.2 Ready/Busy.

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/$\overline{B}$ pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied.

Because pull-up resistor value is related to tR(R/$\overline{B}$) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (Fig 28). Its value can be determined by the following guidance.

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	NVB	2008	-	2048	Blocks

Table 7 : Valid Blocks Numbers

NOTE:
1. The 1st block is guaranteed to be a valid block at the time of shipment.

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (Commercial Temperature Range)	0 to 70	℃
	Ambient Operating Temperature (Industrial Temperature Range)	-40 to 85	℃
T_{BIAS}	Temperature Under Bias	-50 to 125	℃
T_{STG}	Storage Temperature	-65 to 150	V
$VIO^{(2)}$	Input or Output Voltage	-0.6 to 4.6	V
Vcc	Supply Voltage	-0.6 to 4.6	V

Table 8: Absolute maximum ratings

NOTE:

1. Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the Hynix SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

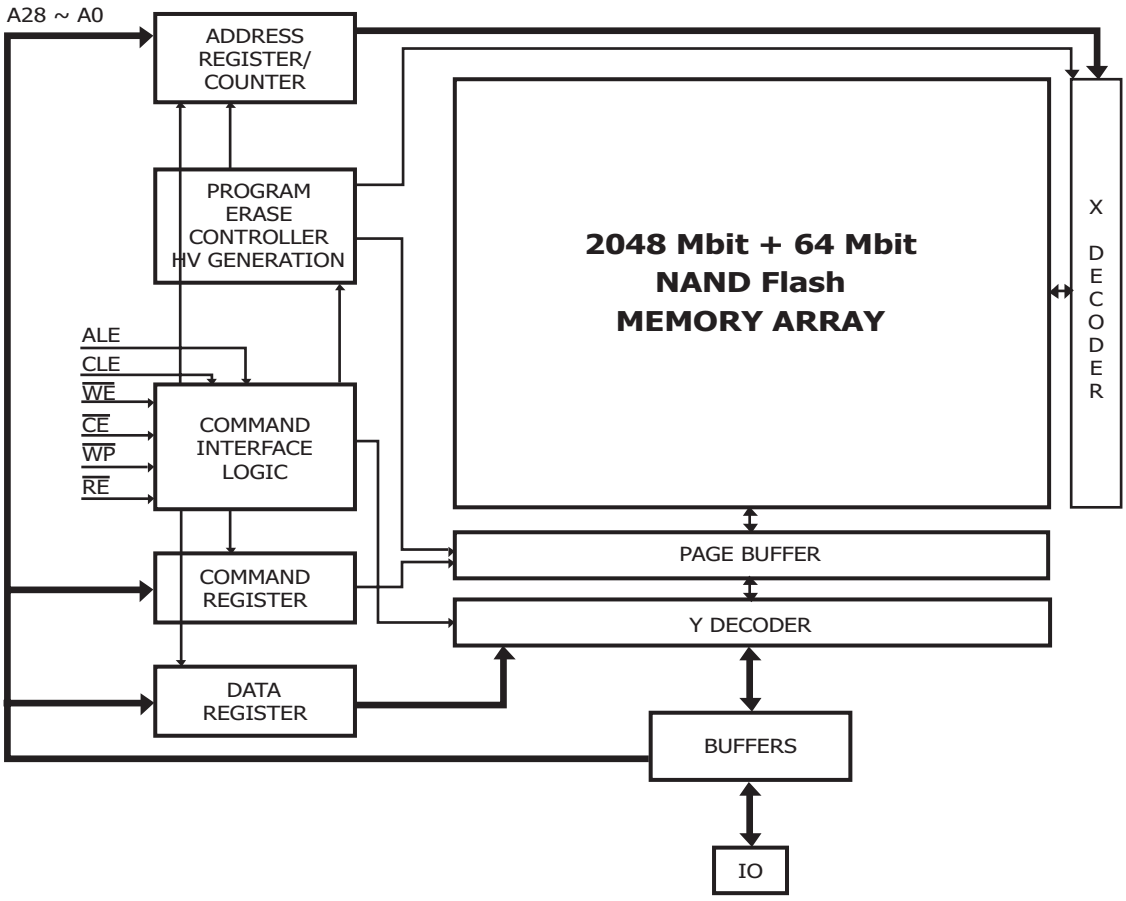


Figure 5: Block Diagram

Parameter		Symbol	Test Conditions	3.3Volt			Unit
				Min	Typ	Max	
Operating Current	Sequential Read	I_{CC1}	tRC=25ns, $\overline{CE}$=VIL, IOUT=0mA	-	15	30	mA
	Program	I_{CC2}	-	-	15	30	mA
	Erase	I_{CC3}	-	-	15	30	mA
Stand-by Current (TTL)		I_{CC4}	$\overline{CE}$=VIH, $\overline{WP}$=0V/Vcc	-		1	mA
Stand-by Current (CMOS)		I_{CC5}	$\overline{CE}$=Vcc-0.2, $\overline{WP}$=0V/Vcc	-	10	50	uA
Input Leakage Current		I_{LI}	VIN=0 to Vcc (max)	-	-	± 10	uA
Output Leakage Current		I_{LO}	VOUT =0 to Vcc (max)	-	-	± 10	uA
Input High Voltage		V_{IH}	-	0.8xVcc	-	Vcc+0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.2xVcc	V
Output High Voltage Level		V_{OH}	IOH=-400uA	2.4	-	-	V
Output Low Voltage Level		V_{OL}	IOL=2.1mA	-	-	0.4	V
Output Low Current (R/$\overline{B}$)		I_{OL} (R/$\overline{B}$)	VOL=0.4V	8	10	-	mA

Table 9: DC and Operating Characteristics

Parameter	Value
	3.3Volt
Input Pulse Levels	0V to VCC
Input Rise and Fall Times	5ns
Input and Output Timing Levels	VCC/2
Output Load (2.7V - 3.6V)	1 TTL GATE and CL=50pF

Table 10: AC Conditions

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

Table 11: Pin Capacitance (TA=25C, F=1.0MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Program Time / Multi-Plane Program Time	t_{PROG}	-	200	700	us
Dummy Busy Time for Two Plane Program	t_{DBSY}	-	0.5	1	us
Number of partial Program Cycles in the same page	NOP	-	-	8	Cycles
Block Erase Time / Multi-Plane Block Erase Time	t_{BERS}	-	1.5	2	ms
Read Cache Busy Time	t_{RBSY}	-	3	tR	us

Table 12: Program / Erase Characteristics

Parameter	Symbol	3.3V		Unit
		Min	Max	
CLE Setup time	t_{CLS}	12		ns
CLE Hold time	t_{CLH}	5		ns
$\overline{CE}$ setup time	t_{CS}	20		ns
$\overline{CE}$ hold time	t_{CH}	5		ns
$\overline{WE}$ pulse width	t_{WP}	12		ns
ALE setup time	t_{ALS}	12		ns
ALE hold time	t_{ALH}	5		ns
Data setup time	t_{DS}	12		ns
Data hold time	t_{DH}	5		ns
Write Cycle time	t_{WC}	25		ns
$\overline{WE}$ High hold time	t_{WH}	10		ns
Data Transfer from Cell to register	t_R		25	us
ALE to $\overline{RE}$ Delay	t_{AR}	10		ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10		ns
Ready to $\overline{RE}$ Low	t_{RR}	20		ns
$\overline{RE}$ Pulse Width	t_{RP}	12		ns
$\overline{WE}$ High to Busy	t_{WB}		100	ns
Read Cycle Time	t_{RC}	25		ns
$\overline{RE}$ Access Time	t_{REA}		20	ns
$\overline{RE}$ High to Output High Z	t_{RHZ}		100	ns
$\overline{CE}$ High to Output High Z	t_{CHZ}		50	ns
$\overline{CE}$ High to Output hold	t_{COH}	15		ns
$\overline{RE}$ High to Output Hold	t_{RHOH}	15		ns
$\overline{RE}$ Low to Output Hold	t_{RLOH}	5		ns
$\overline{RE}$ High Hold Time	t_{REH}	10		ns
Output High Z to $\overline{RE}$ low	t_{IR}	0		ns
$\overline{CE}$ Low to $\overline{RE}$ Low	t_{CR}	10		ns
Address to data loading time	t_{ADL}	70		ns
$\overline{WE}$ High to $\overline{RE}$ low	t_{WHR}	60		ns
$\overline{RE}$ High to $\overline{WE}$ low	t_{RHW}	100		ns
Device Resetting Time (Read / Program / Erase)	t_{RST}		5/10/500(1)	us
Write Protection time	t_{WW}(2)	100		ns

Table 13: AC Timing Characteristics

NOTE:

1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us
2. Program / Erase Enable Operation : $\overline{WP}$ high to $\overline{WE}$ High.
   Program / Erase Disable Operation : $\overline{WP}$ Low to $\overline{WE}$ High.

IO	Page Program	Block Erase	Read	Cache Read	CODING
0	Pass / Fail	Pass / Fail	NA	NA	Pass: '0' Fail: '1'
1	NA	NA	NA	NA	-
2	NA	NA	NA	NA	-
3	NA	NA	NA	NA	-
4	NA	NA	NA	NA	-
5	Ready / Busy	Ready / Busy	Ready / Busy	P/E/R Controller Bit	Active: '0' Idle:'1'
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready/Busy	Busy: '0' Ready:'1'
7	Write Protect	Write Protect	Write Protect	NA	Protected: '0' Not Protected: '1'

Table 14 : Status Register Coding

DEVICE IDENTIFIER CYCLE	DESCRIPTION
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell Type, etc.
4th	Page Size, Block Size, Spare Size, Organization
5th	Multiplane information

Table 15: Device Identifier Coding

Part Number	Voltage	Bus Width	1st cycle (Manufacture Code)	2nd cycle (Device Code)	3rd cycle	4th cycle	5th cycle
HY27UF082G2B	3.3V	x8	ADh	DAh	10h	95h	44h
HY27UF162G2B	3.3V	x16	ADh	CAh	10h	D5h	44h

Table 16: Read ID Data Table

	Description	IO7	IO6	IO5 IO4	IO3 IO2	IO1 IO0
Die / Package	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleave program Between multiple chips	Not Supported		0 1			
Write Cache	Not Supported	0 1				

Table 17: 3rd Byte of Device Idendifier Description

	Description	IO7	IO6	IO5-4	IO3	IO2	IO1-0
Page Size (Without Spare Area)	1KB 2KB 4KB 8KB						0 0 0 1 1 0 1 1
Spare Area Size (Byte / 512Byte)	8 16					0 1	
Serial Access Time	50ns 30ns 25ns Reserved	0 0 1 1			0 1 0 1		
Block Size (Without Spare Area)	64K 128K 256K 512KB			0 0 0 1 1 0 1 1			
Organization	X8 X16		0 1				

Table 18: 4th Byte of Device Identifier Description

	Description	IO7	IO6 IO5 IO4	IO3 IO2	IO1	IO0
Plane Number	1 2 4 8			0 0 0 1 1 0 1 1		
Plane Size (w/o redundant Area)	64Mb 128Mb 256Mb 512Mb 1Gb 2Gb 4Gb 8Gb		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1			
Reserved		0			0	0

Table 19: 5rd Byte of Device Idendifier Description

Main Field (2,048 Byte)				Spare Field (64 Byte)			
"A" area (1st sector)	"B" area (2nd sector)	"C" area (3rd sector)	"D" area (4th sector)	"E" area (1st sector)	"F" area (2nd sector)	"G" area (3rd sector)	"H" area (4th sector)
512 Byte	512 Byte	512 Byte	512 Byte	16 Byte	16 Byte	16 Byte	16 Byte

Sector	Main Field (Column 0~2, 047)		Spare Field (Column 2,048~2,111)	
	Area Name	Column Address	Area Name	Column Address
1st 528 Byte Sector	"A"	0 ~ 511	"E"	2,048 ~ 2,063
2nd 528 Byte Sector	"B"	512 ~ 1,023	"F"	2,064 ~ 2,079
3rd 528 Byte Sector	"C"	1,024 ~ 1,535	"G"	2,080 ~ 2,095
4th 528 Byte Sector	"D"	1,536 ~ 2,047	"H"	2,096 ~ 2,111

Table 20: Page organization in EDC units (x8)

Main Field (2,048 Byte)				Spare Field (64 Byte)			
"A" area (1st sector)	"B" area (2nd sector)	"C" area (3rd sector)	"D" area (4th sector)	"E" area (1st sector)	"F" area (2nd sector)	"G" area (3rd sector)	"H" area (4th sector)
256 Words	256 Words	256 Words	256 Words	8 Words	8 Words	8 Words	8 Words

Sector	Main Field (Column 0~1, 1023)		Spare Field (Column 1,024~1,055)	
	Area Name	Column Address	Area Name	Column Address
1st 264 Words Sector	"A"	0 ~ 255	"E"	1,024 ~ 1,031
2nd 264 Words Sector	"B"	256 ~ 511	"F"	1,032 ~ 1,039
3rd 264 Words Sector	"C"	512 ~ 767	"G"	1,040 ~ 1,047
4th 264 Words Sector	"D"	768 ~ 1,023	"H"	1,048 ~ 1,055

Table 21: Page organization in EDC units (x16)

IO	Copy back Program	CODING
0	Pass/Fail	Pass: '0' Fail: '1'
1	EDC status	NO error: '0'
2	EDC Validity	Invalid: '0' Valid: '1'
3	NA	-
4	NA	-
5	Ready/Busy	Busy: '0' Ready: '1'
6	Ready/Busy	Busy: '0' Ready: '1'
7	Write Protect	Protected: '0' Not Protected: '1'

Table 22: EDC Register Coding

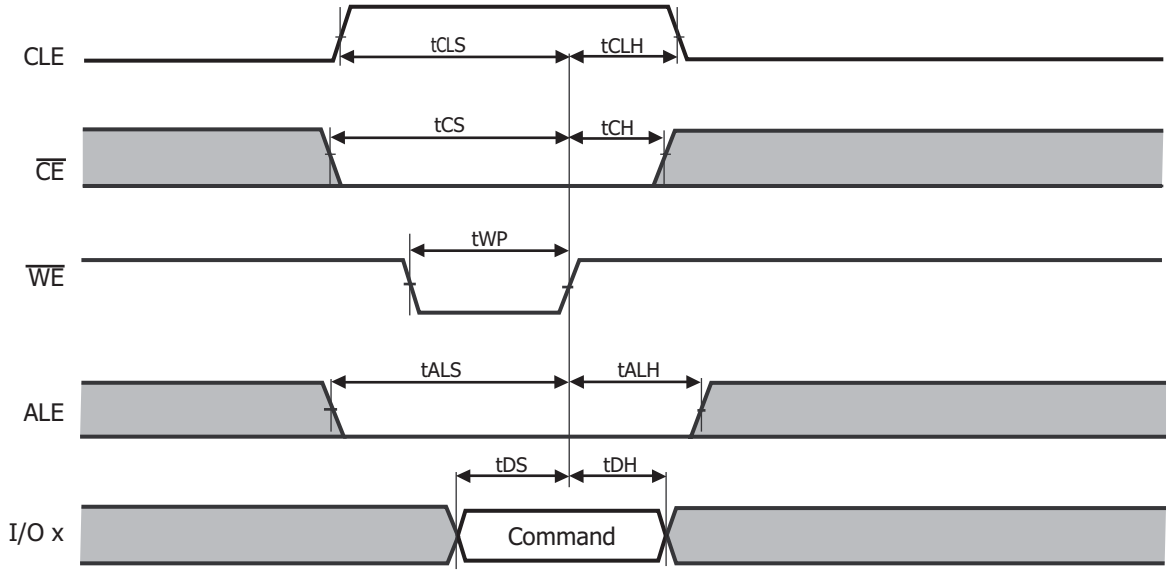


Figure 6: Command Latch Cycle

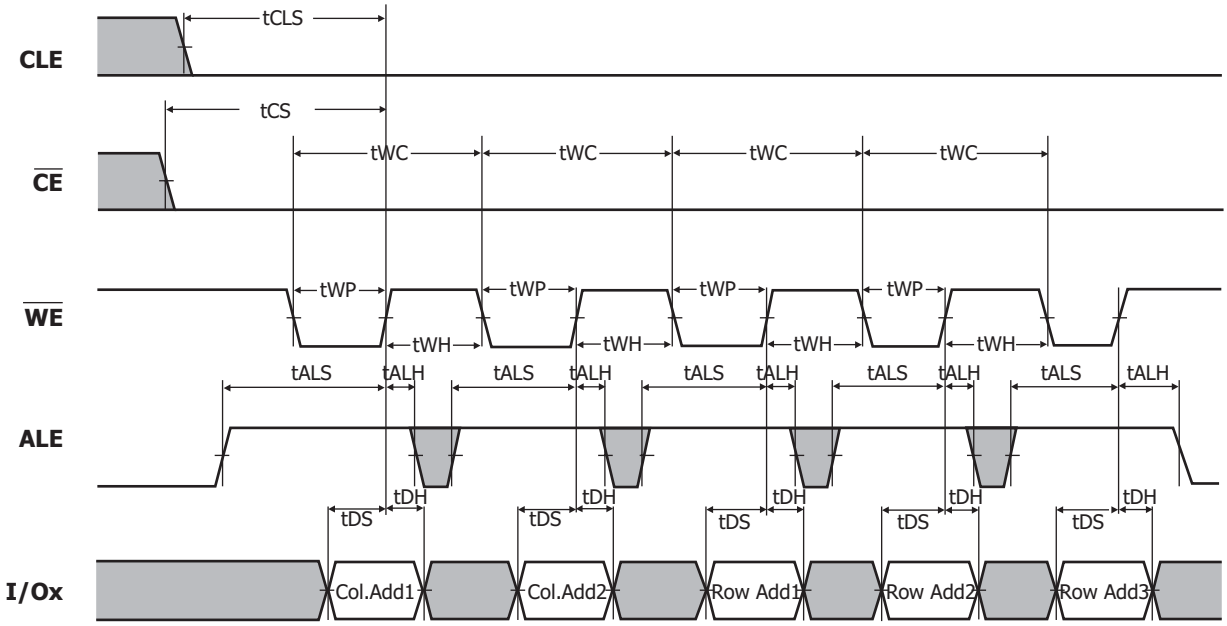
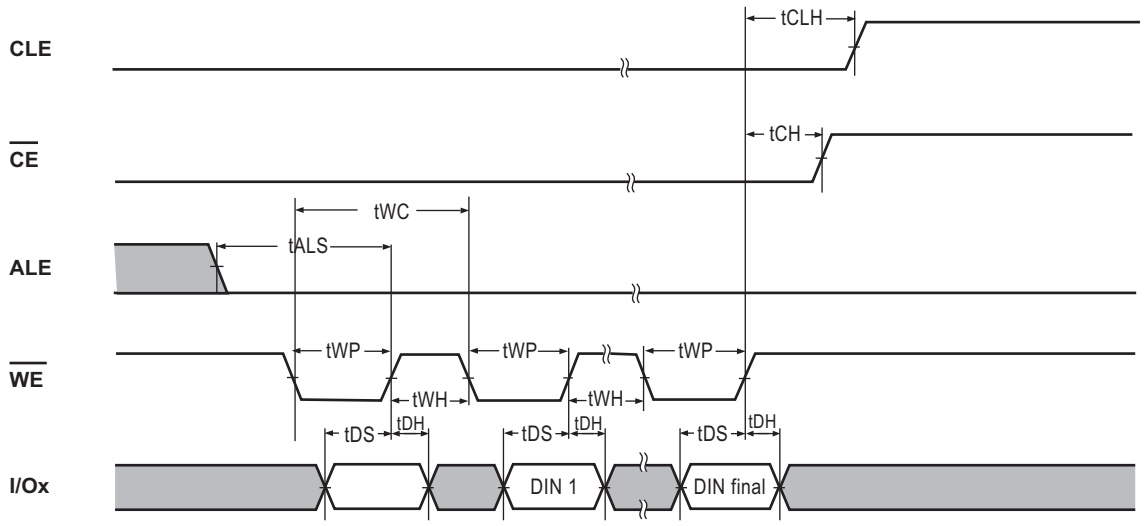
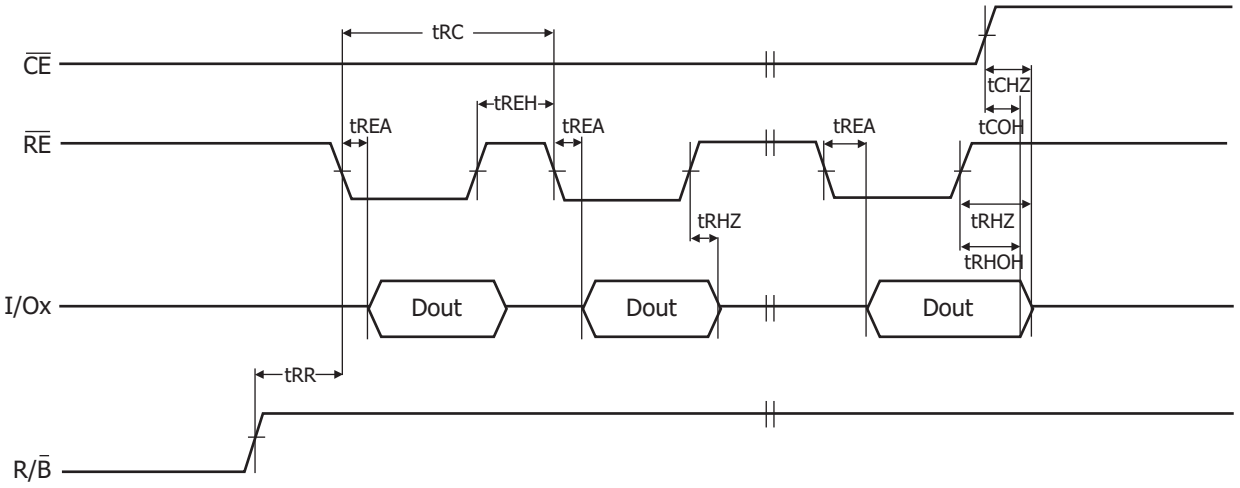


Figure 7: Address Latch Cycle



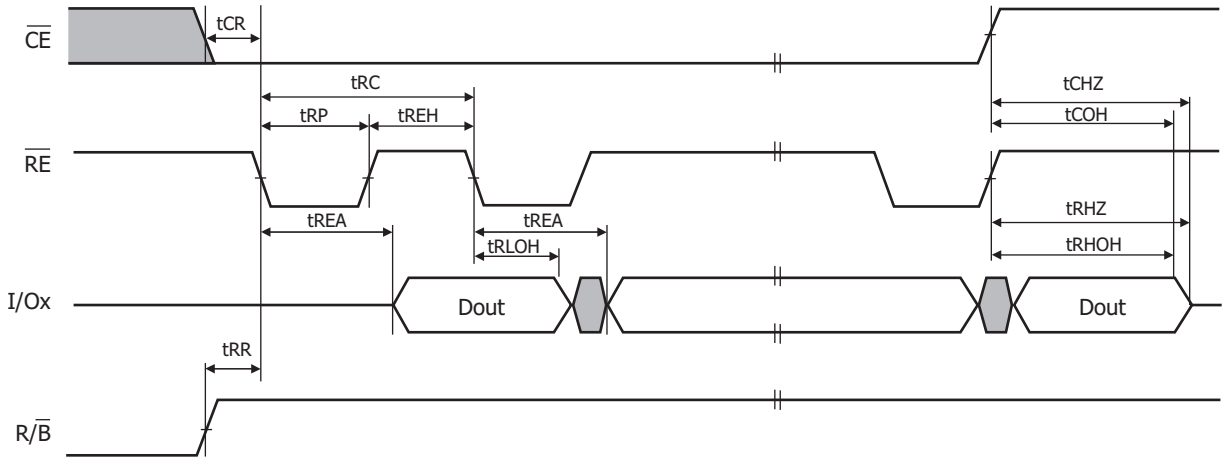
Notes: DIN final means 2,112Bytes (x8)

Figure 8: Input Data Latch Cycle



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 9: Sequential Out Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 10: Sequential Out Cycle after Read (EDO Type CLE=L, $\overline{WE}$=H, ALE=L)

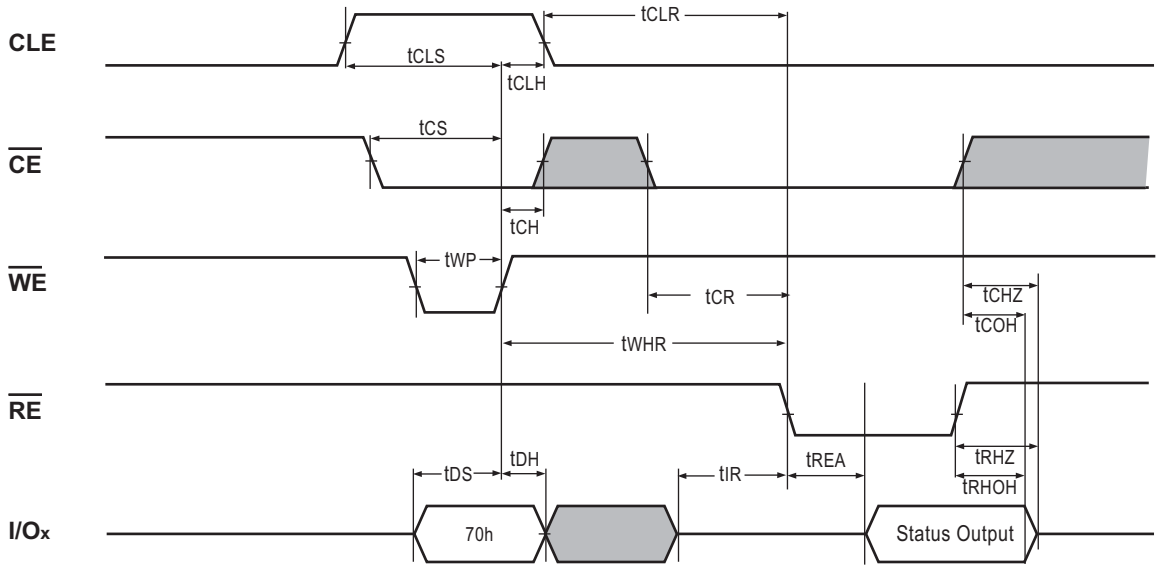


Figure 11: Status Read Cycle

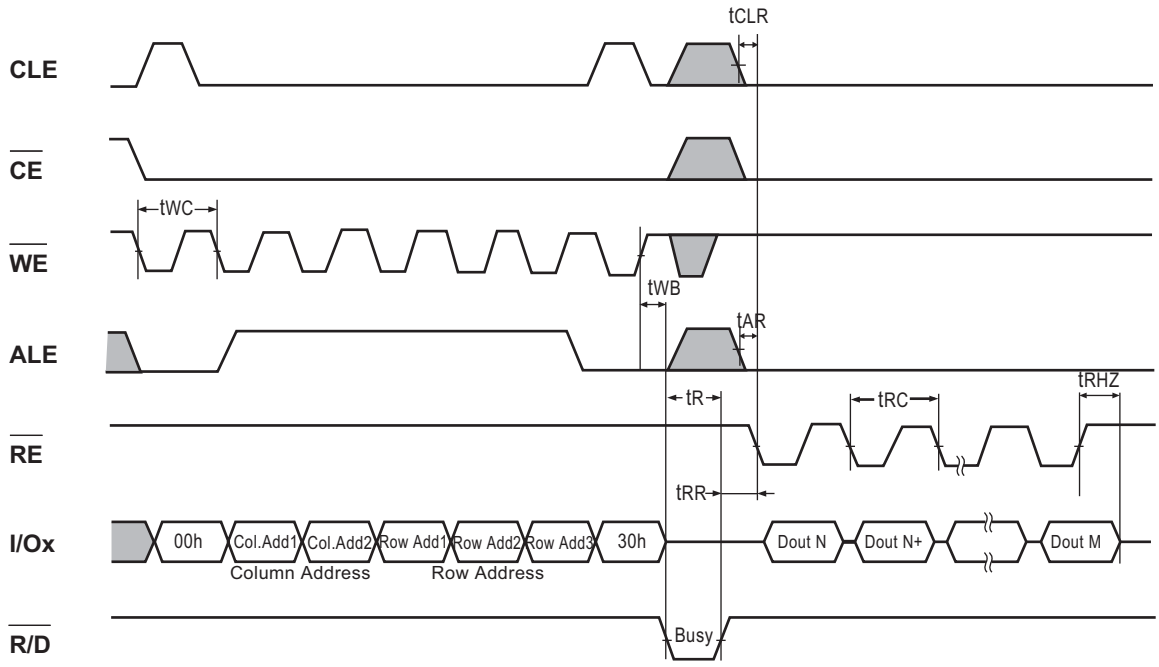


Figure 12: Read1 Operation (Read One Page)

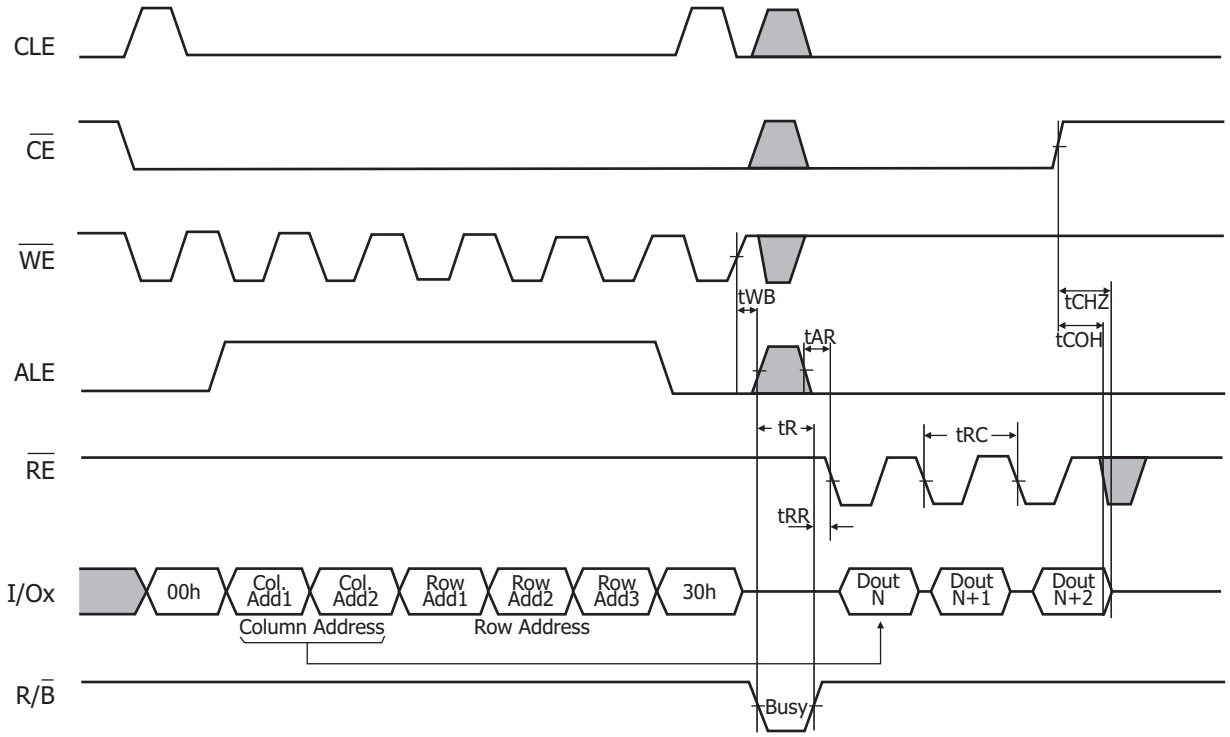


Figure 13: Read1 Operation intercepted by $\overline{CE}$

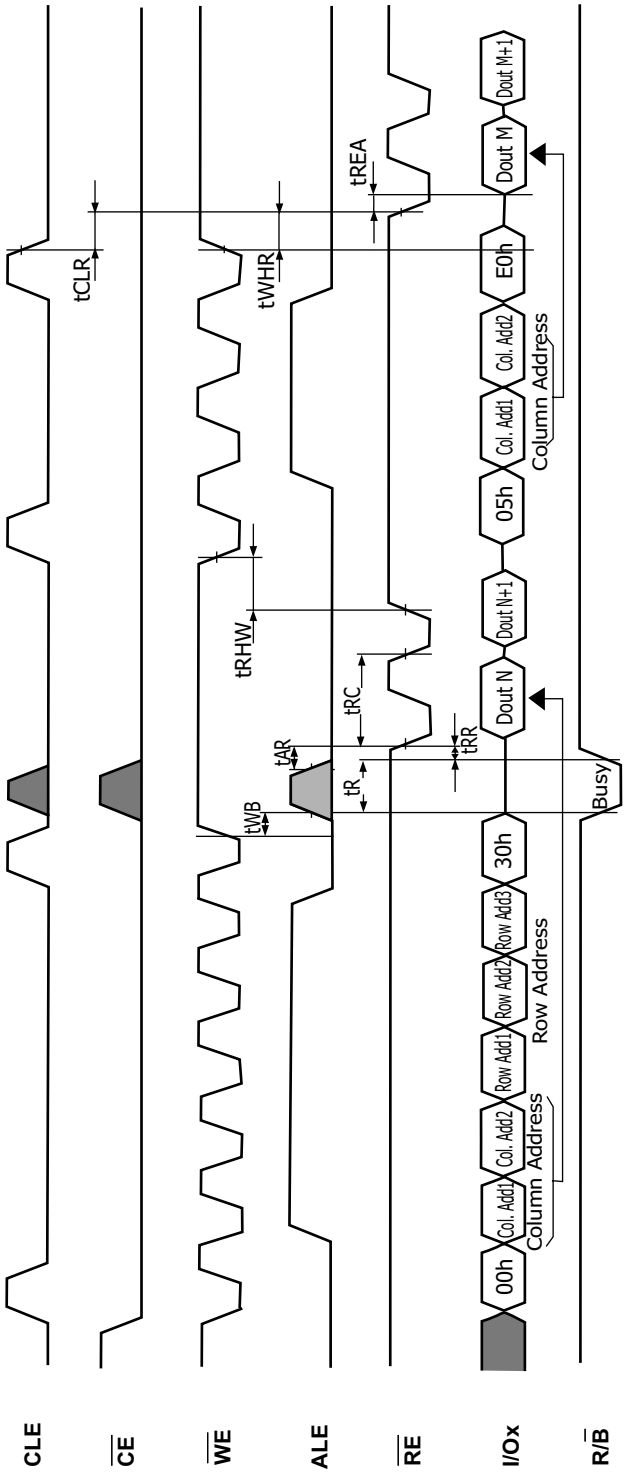


Figure 14 : Random Data output

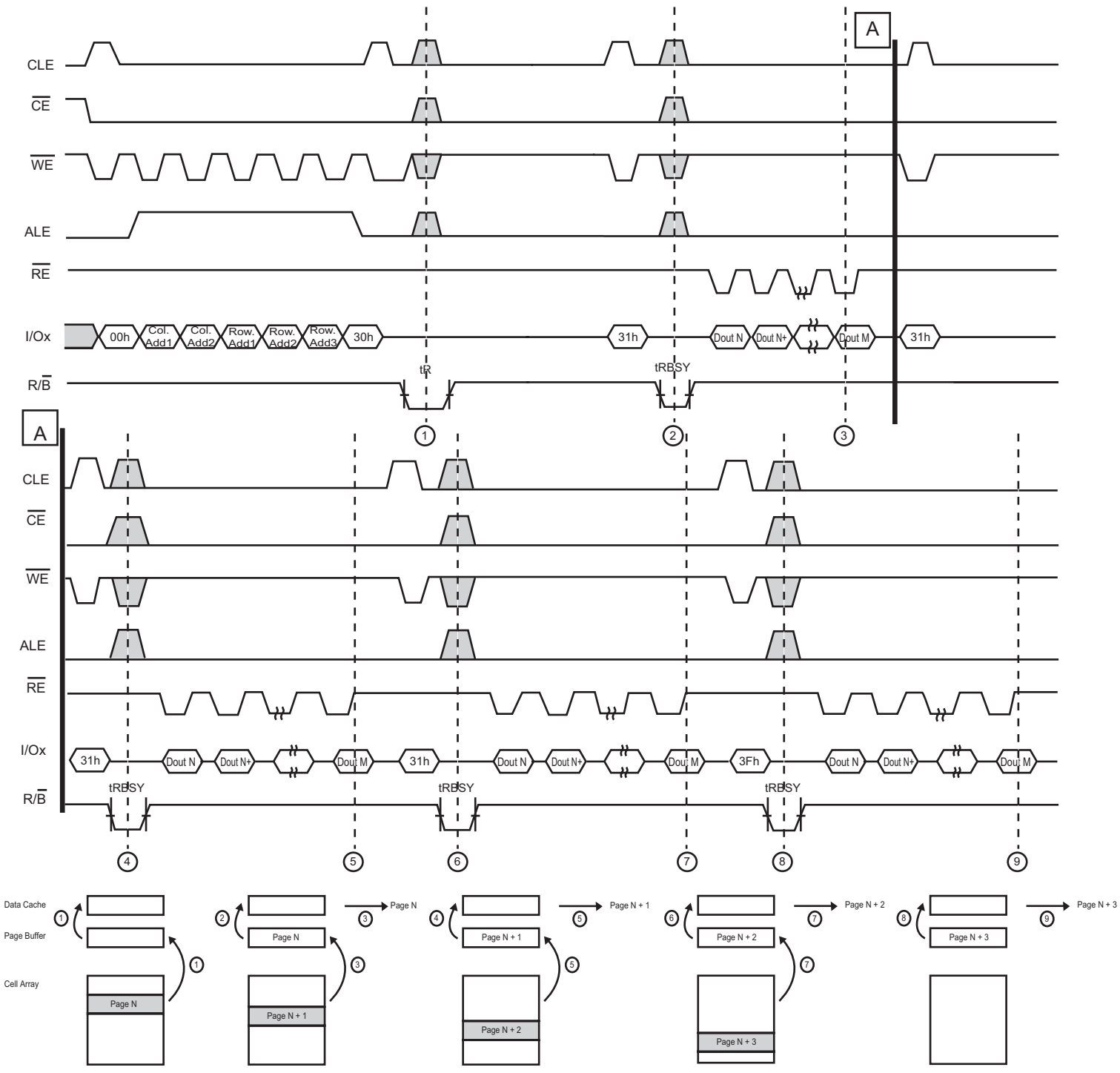
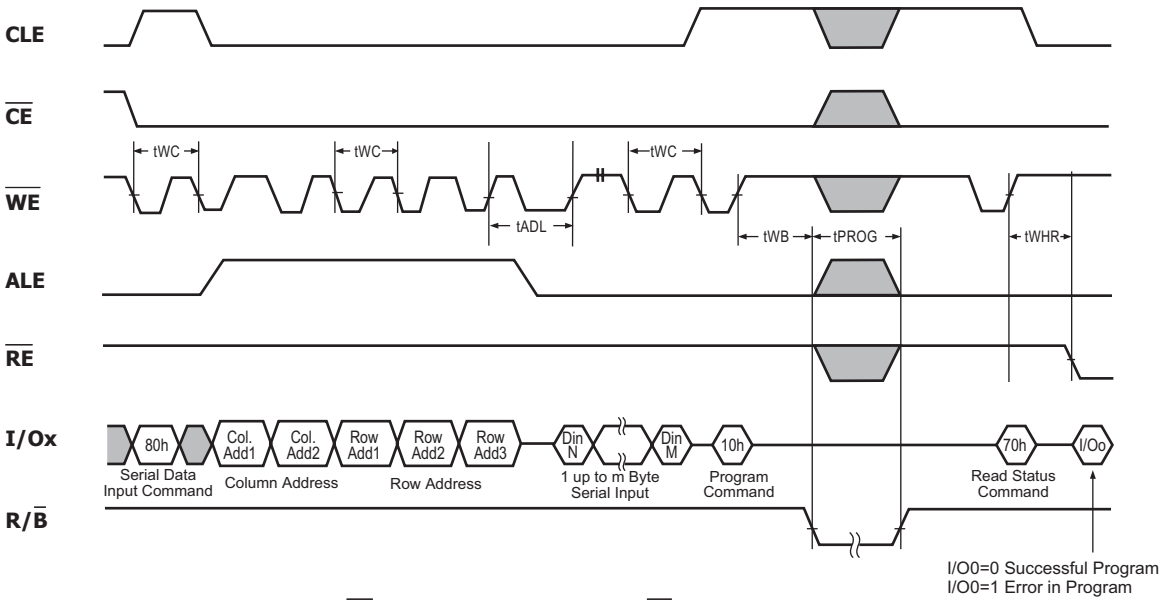


Figure 15: Read Operation with Read Cache



NOTES : tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

Figure 16: Page Program Operation

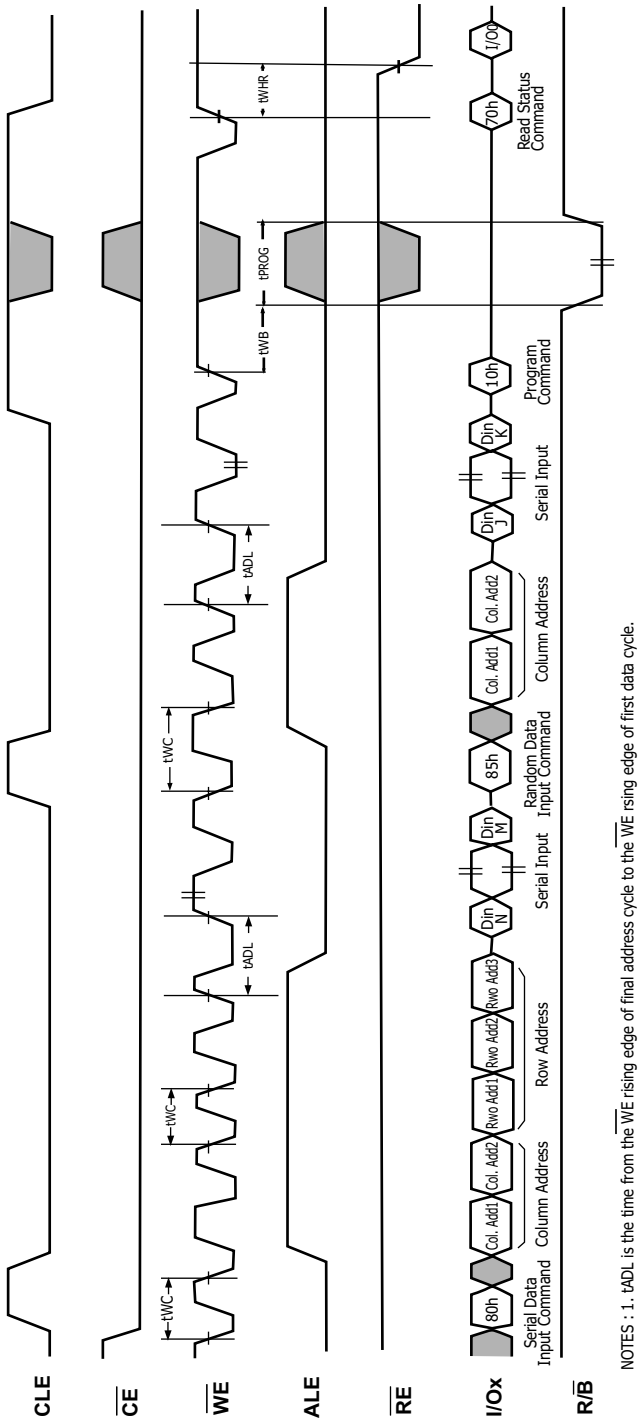


Figure 17: Random Data In

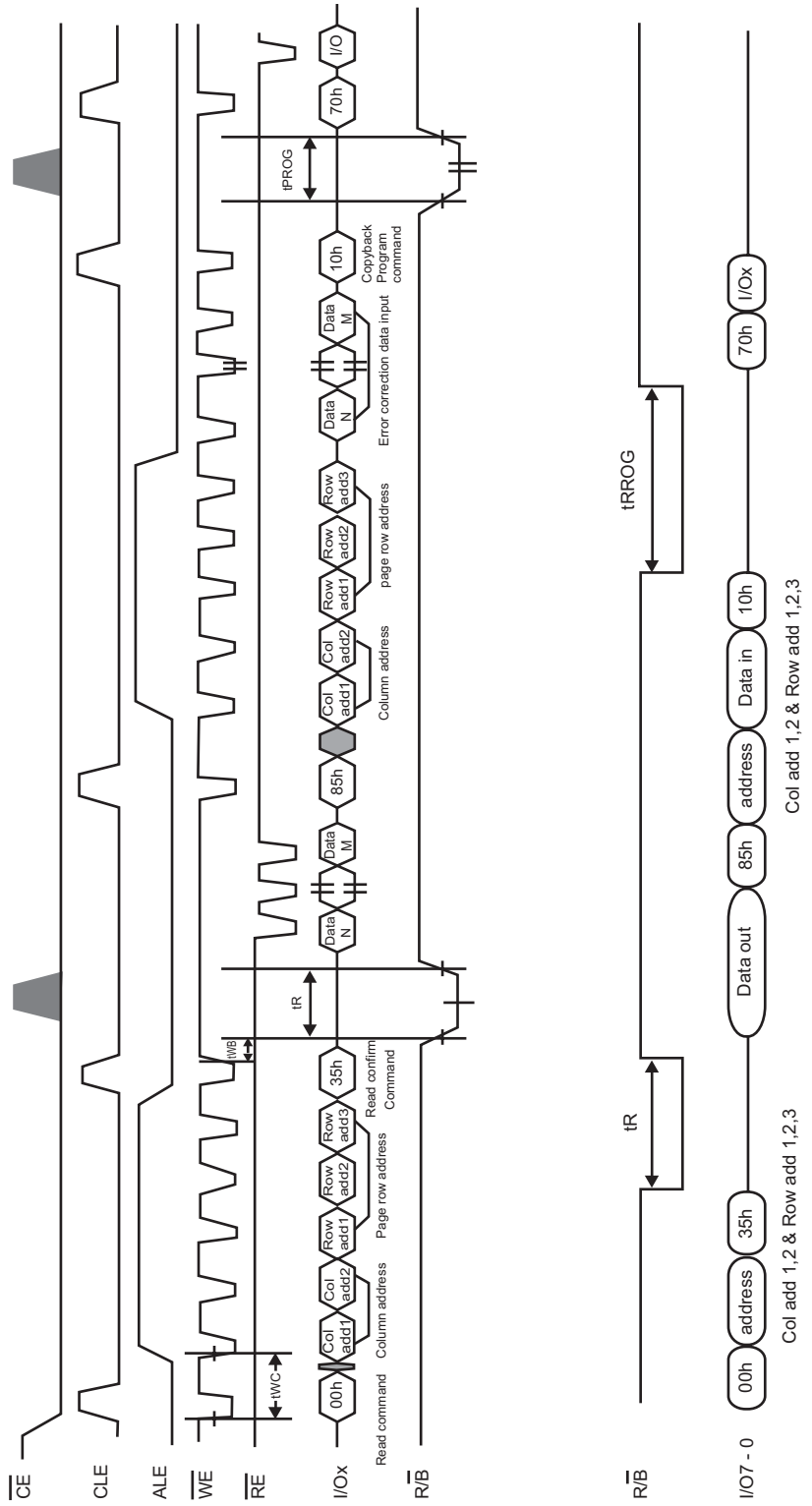


Figure 18: Copy Back Program Operation

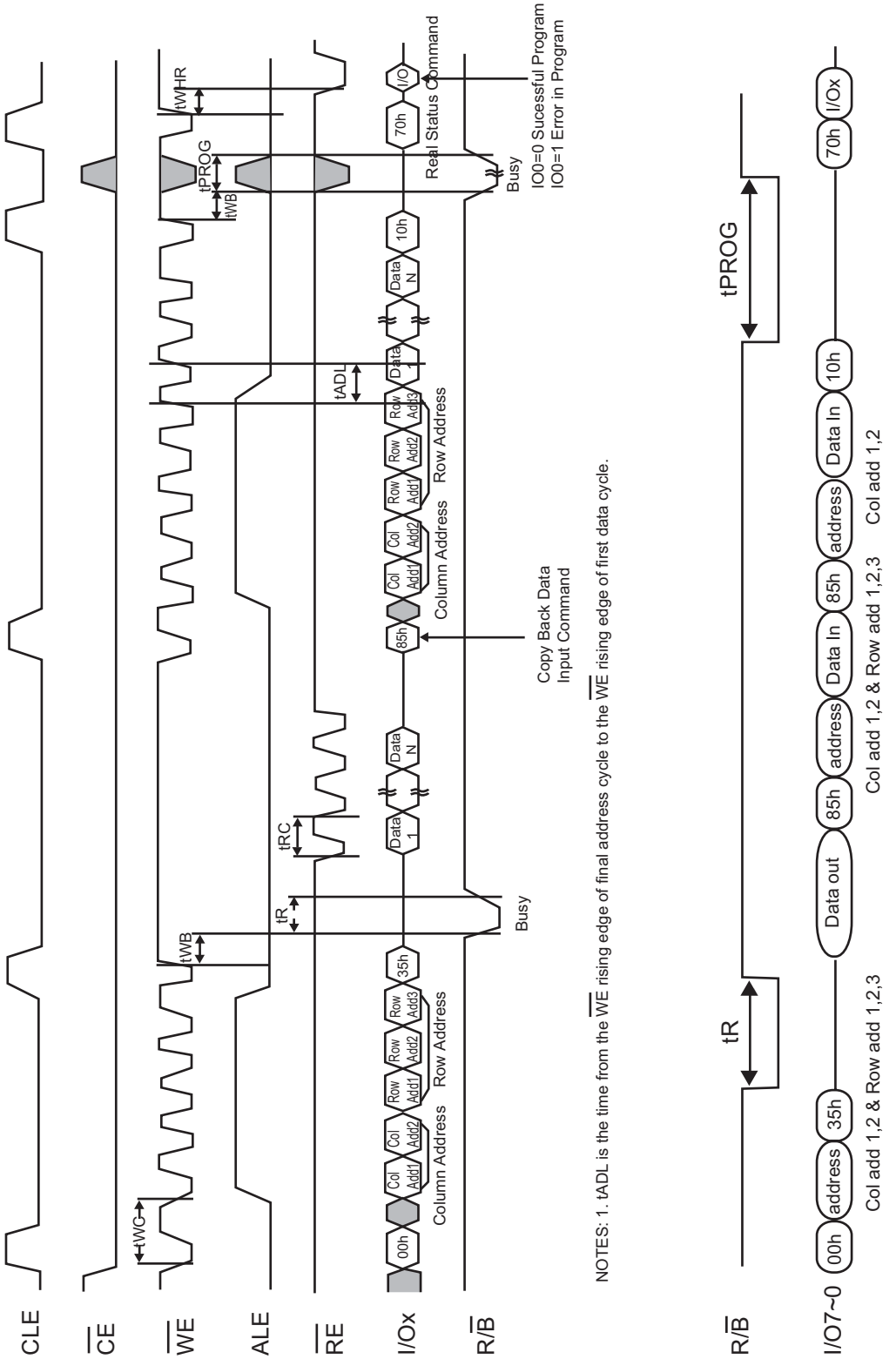


Figure 19: Copy Back Program Operation with Random Data Input

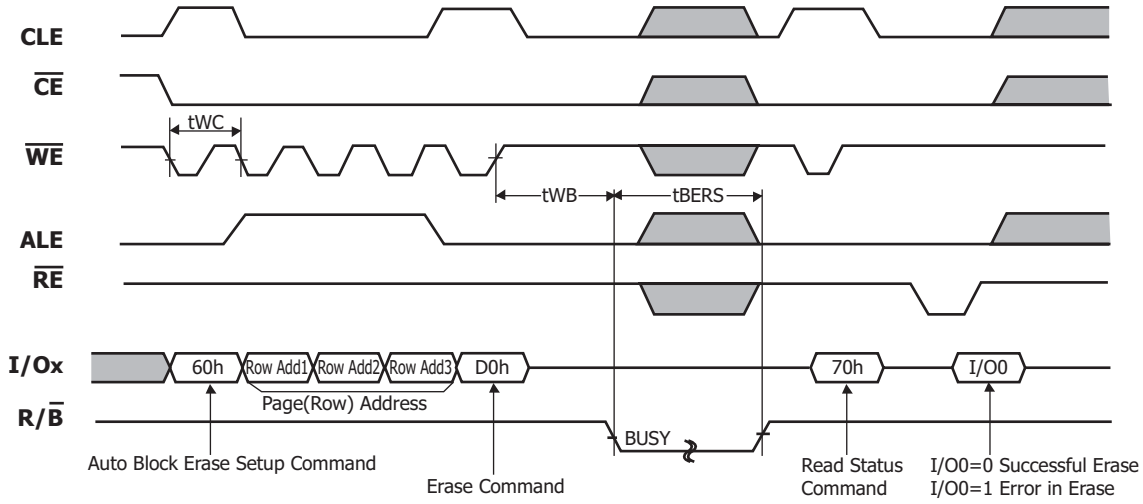


Figure 20: Block Erase Operation (Erase One Block)

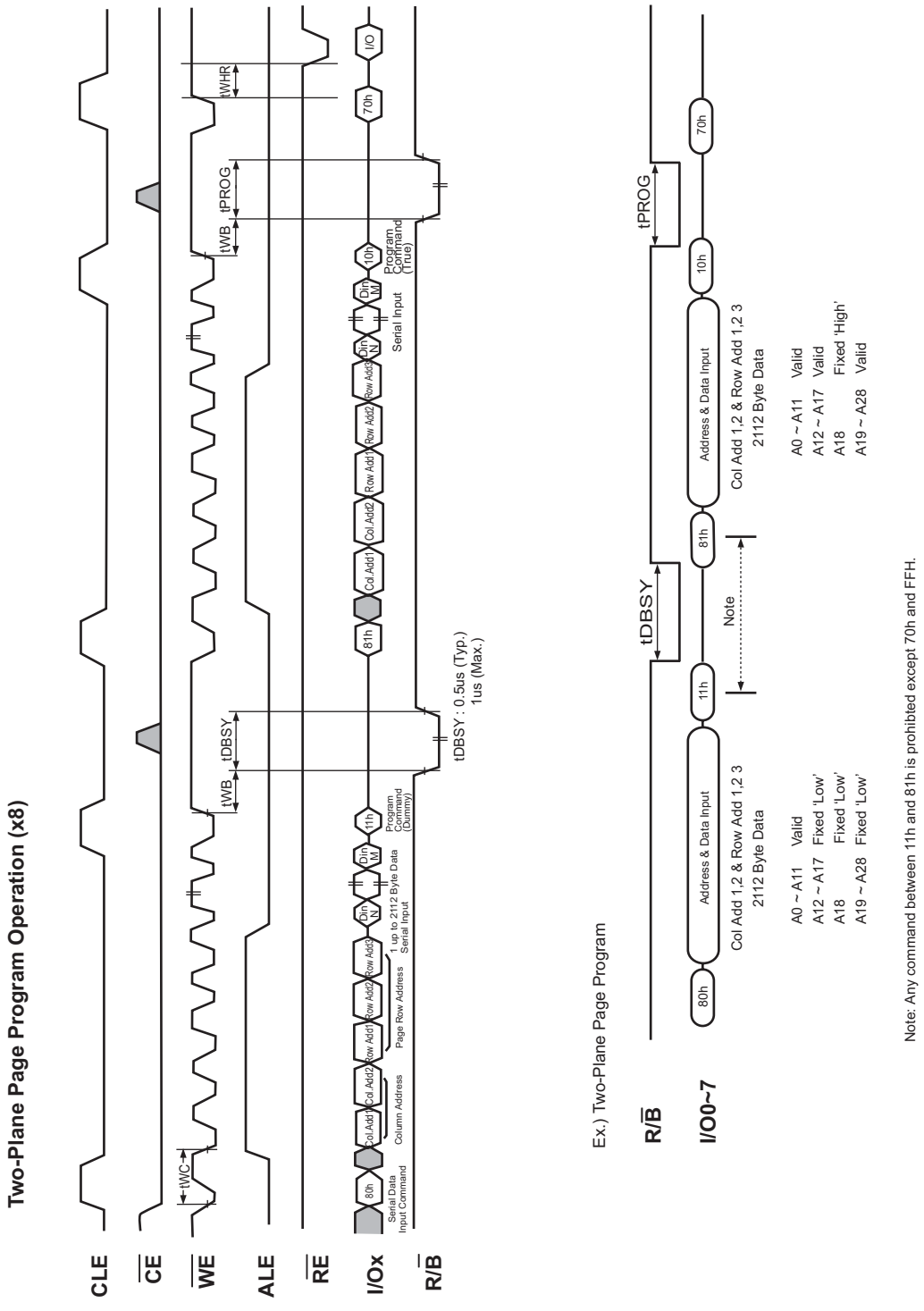
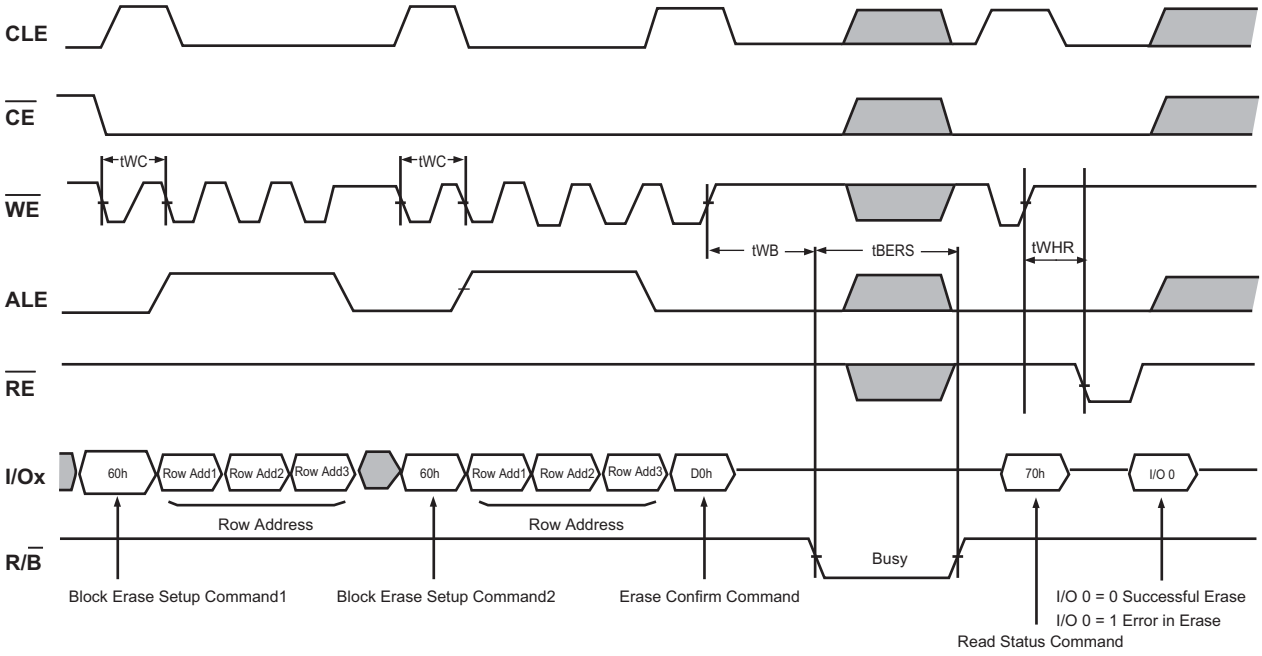


Figure 21: Multiple plane page program



Ex.) Address Restriction for Two-Plane Block Erase Operation

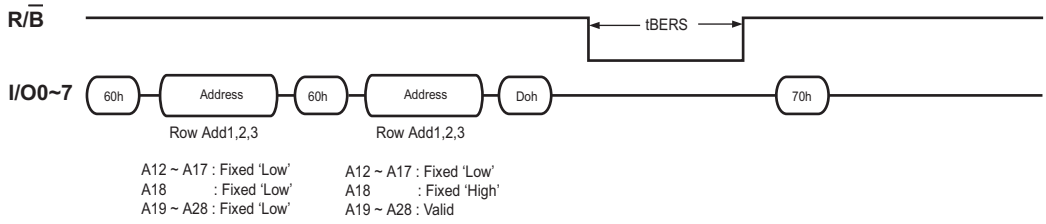


Figure 22: Multiple plane erase operation

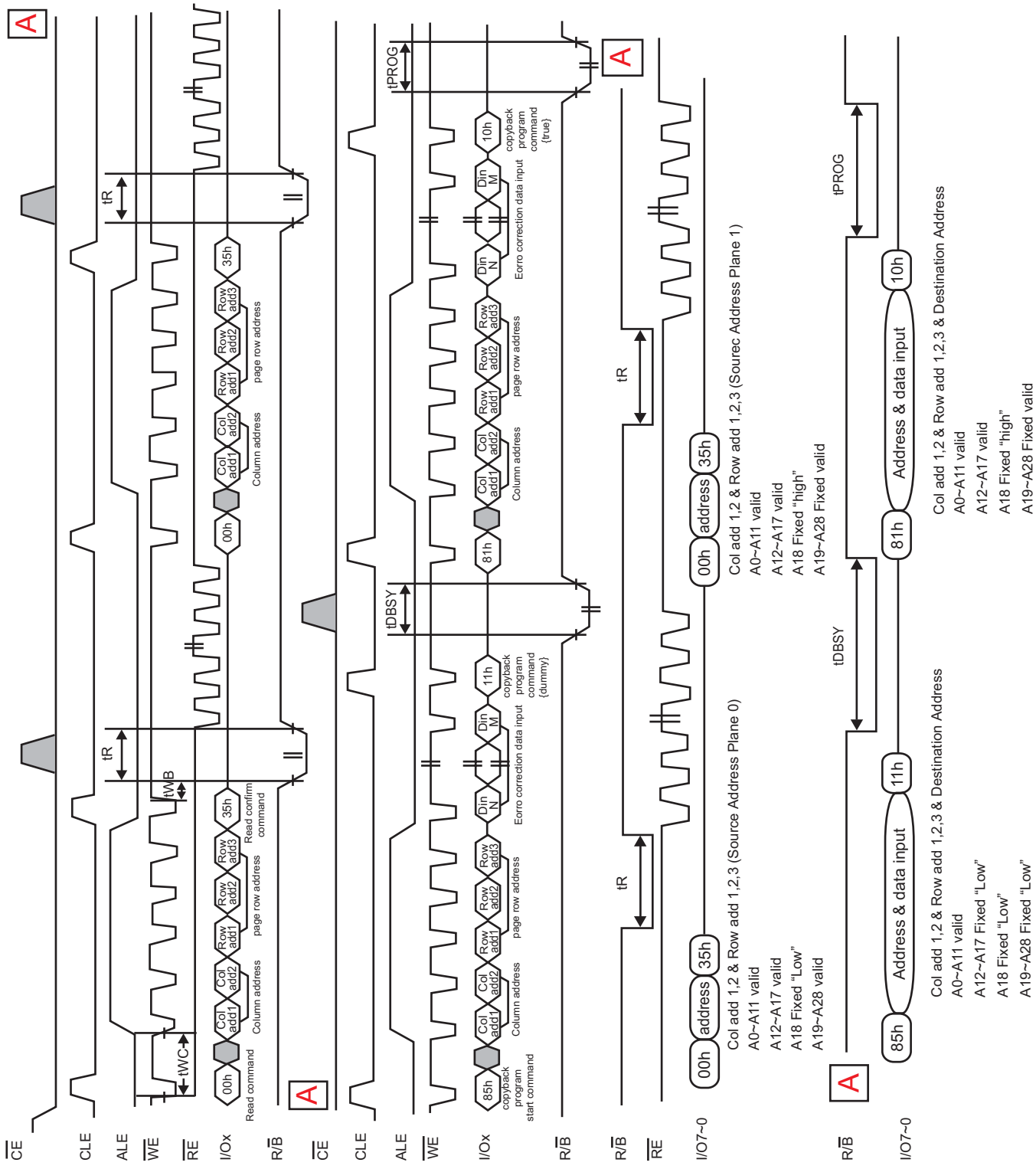


Figure 23: Multi plane copyback program Operation

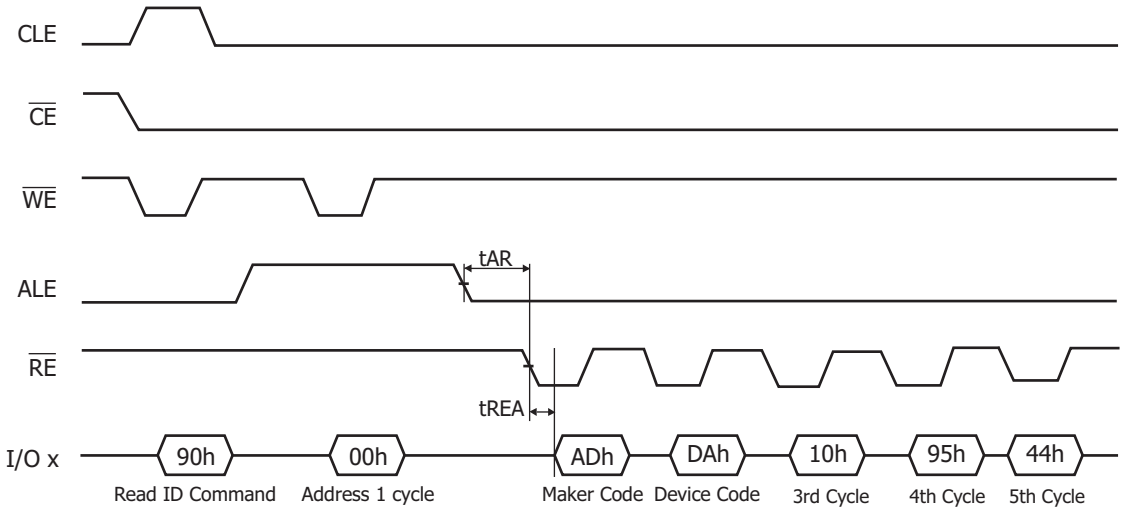


Figure 24: Read ID Operation

System Interface Using $\overline{CE}$ don't care

To simplify system interface, $\overline{CE}$ signal is ignored during data loading or sequential data-reading as shown below. So, it is possible to connect NAND Flash to a microprocessor. The only function that was removed from standard NAND Flash to make $\overline{CE}$ don't care read operation was disabling of the automatic sequential read function.

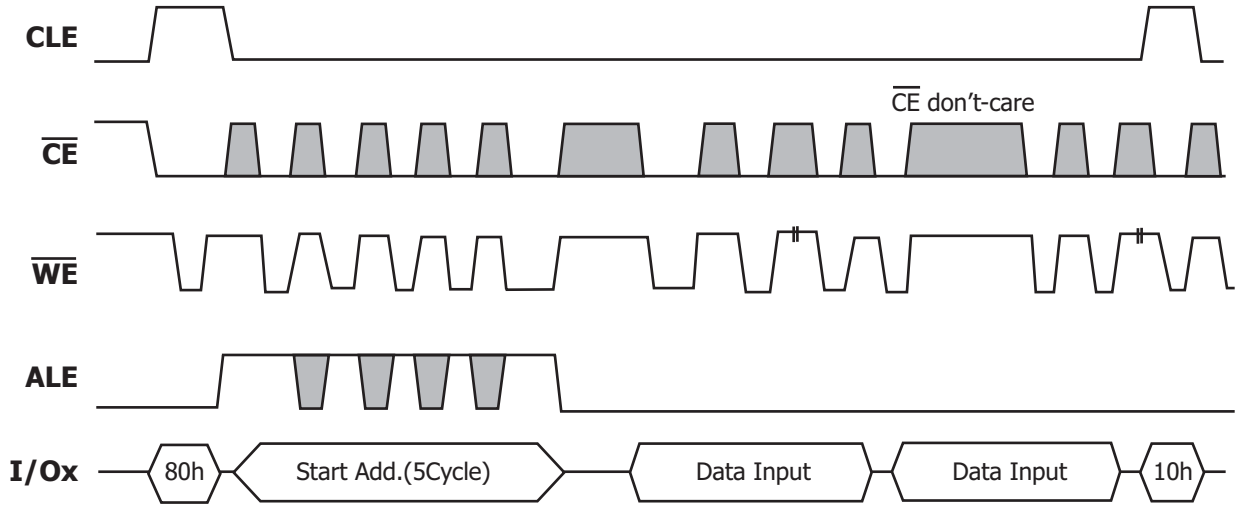


Figure 25: Program Operation with $\overline{CE}$ don't-care.

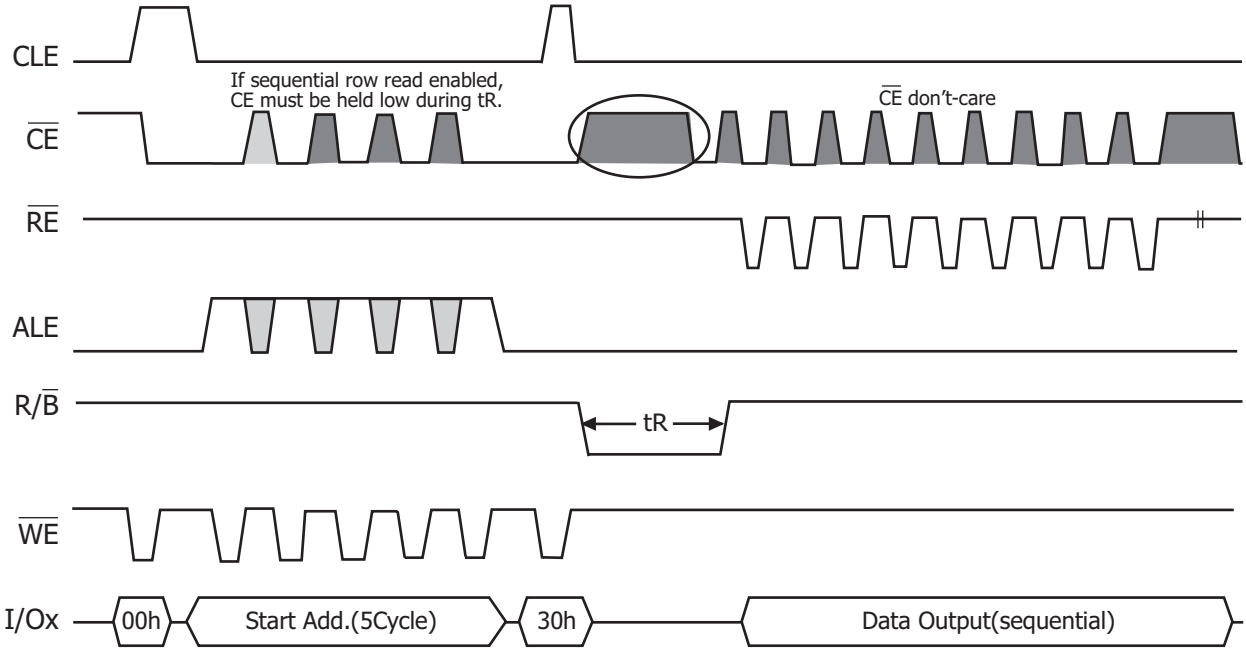


Figure 26: Read Operation with $\overline{CE}$ don't-care.

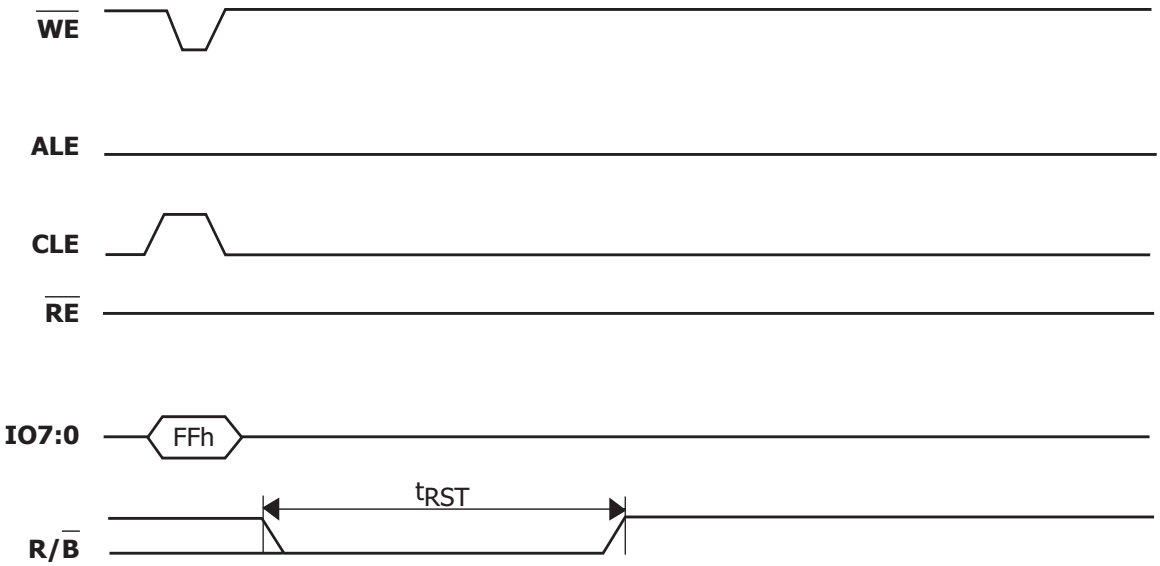


Figure 27: Reset Operation

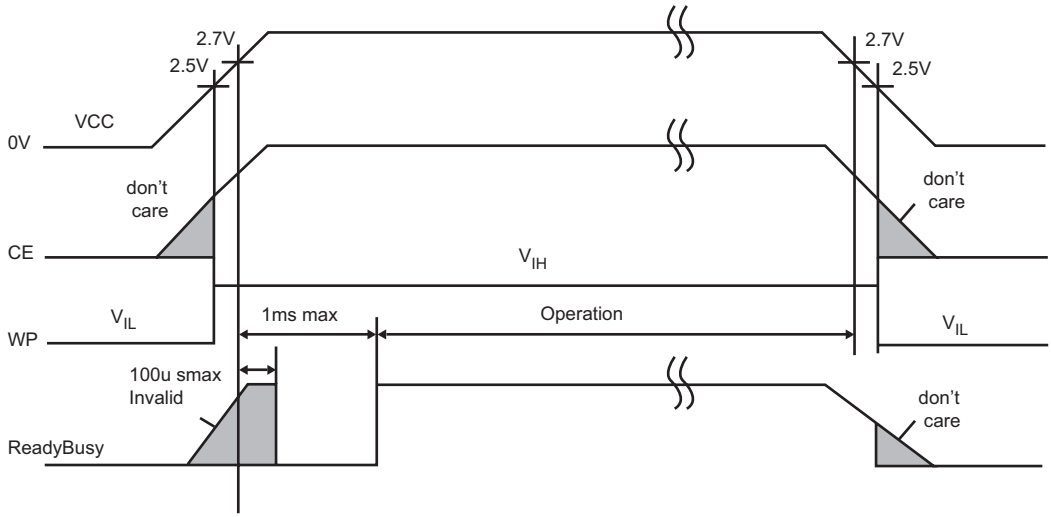


Figure 28: Power On and Data Protection Timing

VTH = 2.5 Volt for 3.3 Volt Supply devices

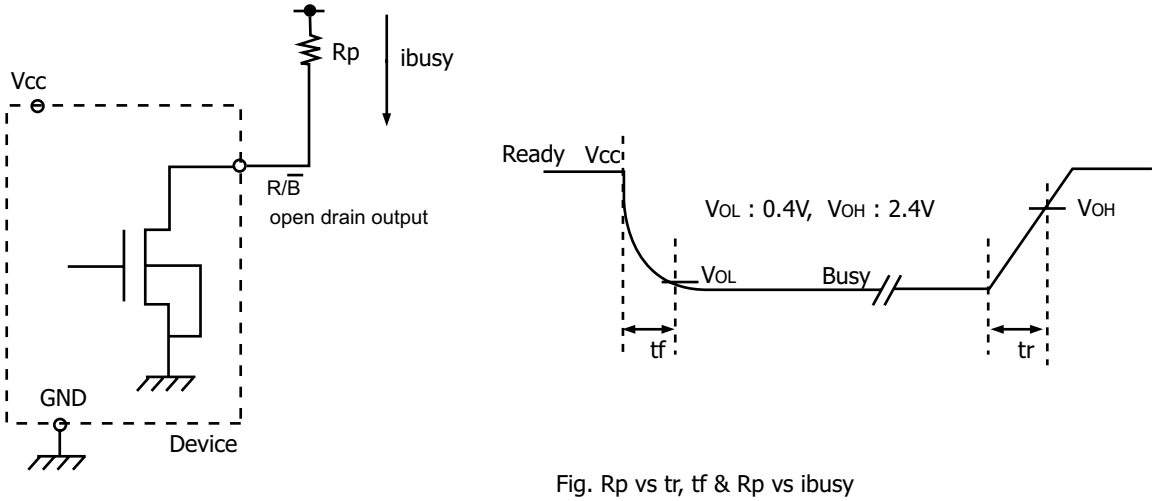
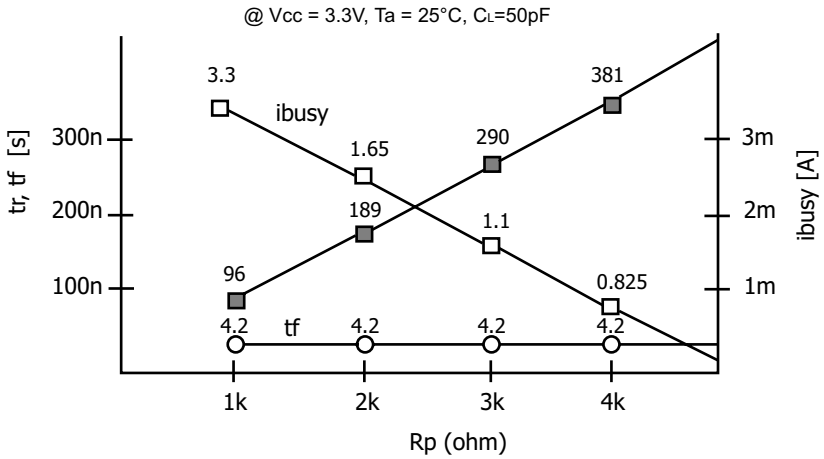


Fig. Rp vs tr, tf & Rp vs ibusy



Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currents of all devices tied to the R/B pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 29: Ready/Busy Pin electrical specifications

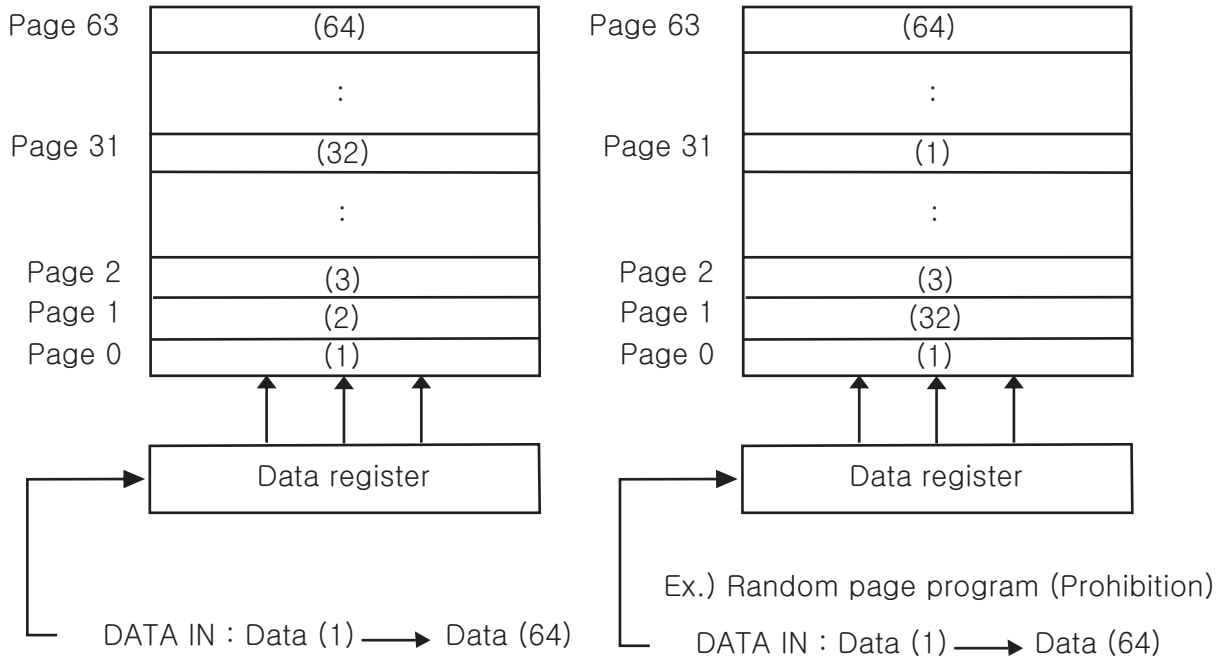


Figure 30: page programming within a block

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the 1st or 2nd th page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 31. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

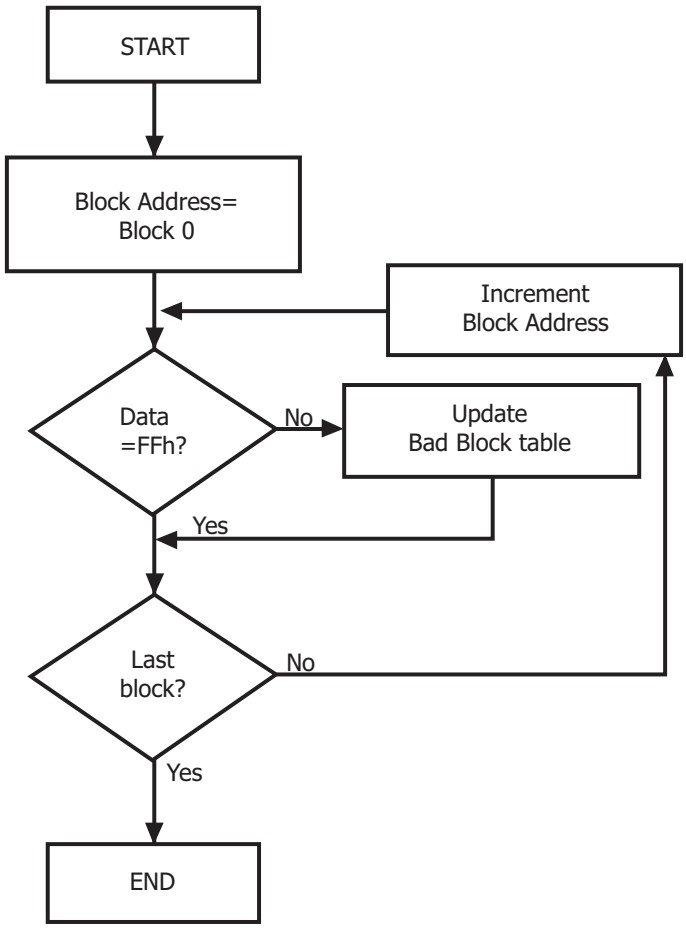


Figure 31: Bad Block Management Flowchart

Bad Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.
Unlike the case of odd page which carries a possibility of affecting previous page, the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.
Refer to Table 23 and Figure 32 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC (with 1bit/528byte)

Table 23: Block Failure

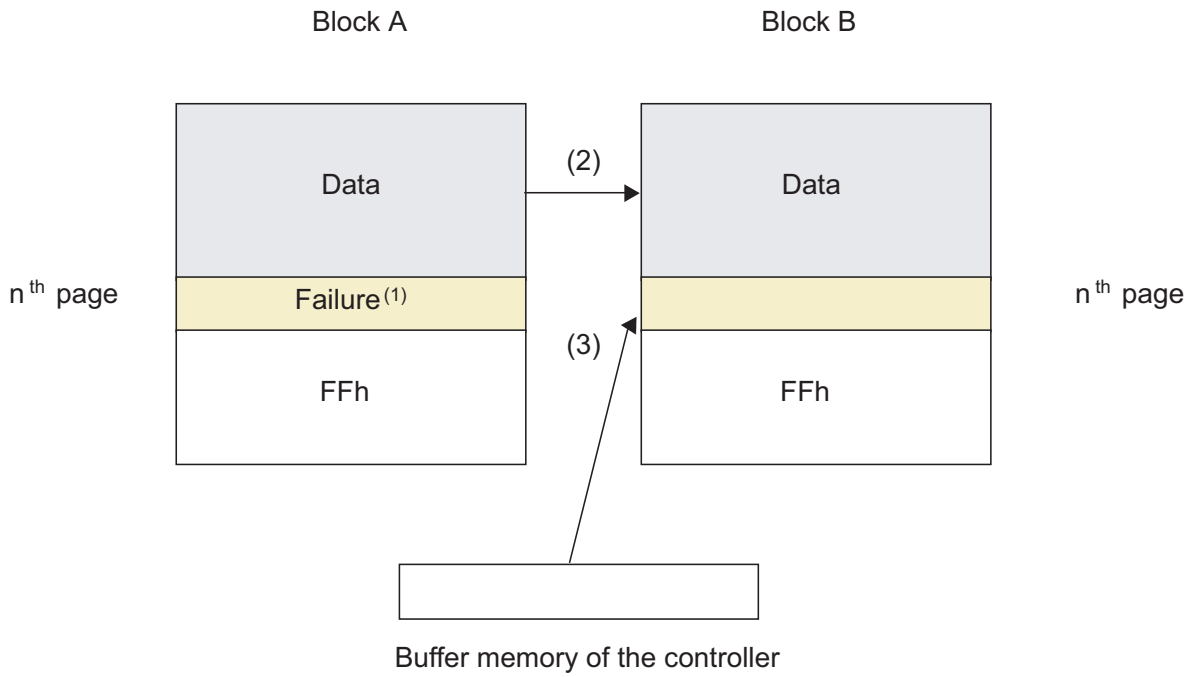


Figure 32: Bad Block Replacement

NOTE :
1. An error occurs on n^{th} page of the Block A during program or erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. N^{th} data of block A which is in controller buffer memory is copied into n^{th} page of Block B
4. Bad block table should be updated to prevent from eraseing or programming Block A

Write Protect Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows (Figure 33~36)

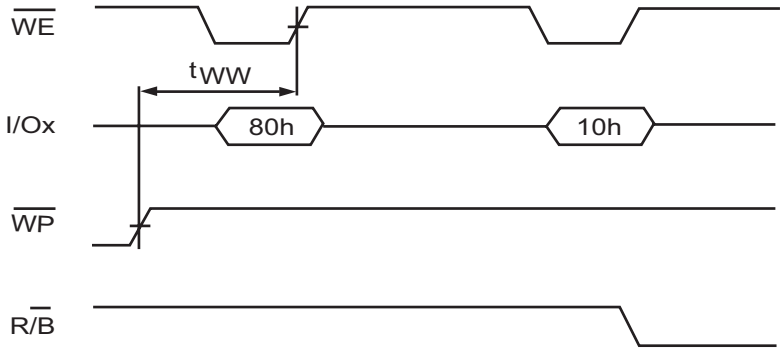


Figure 33: Enable Programming

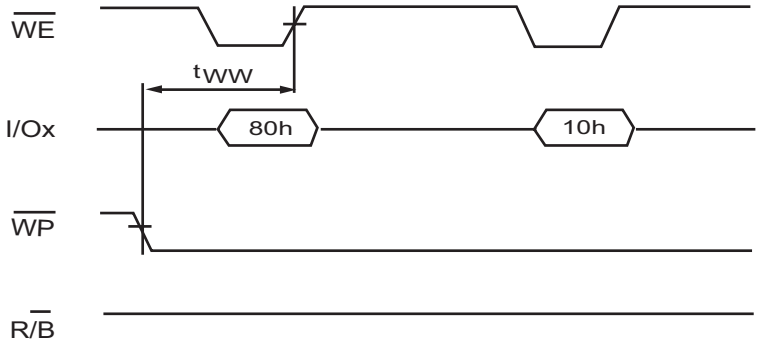


Figure 34: Disable Programming

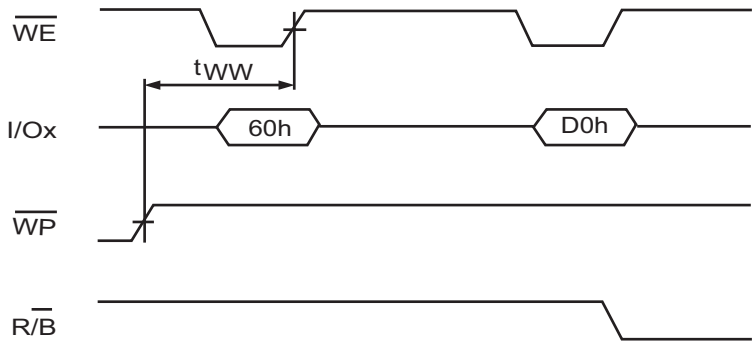


Figure 35: Enable Erasing

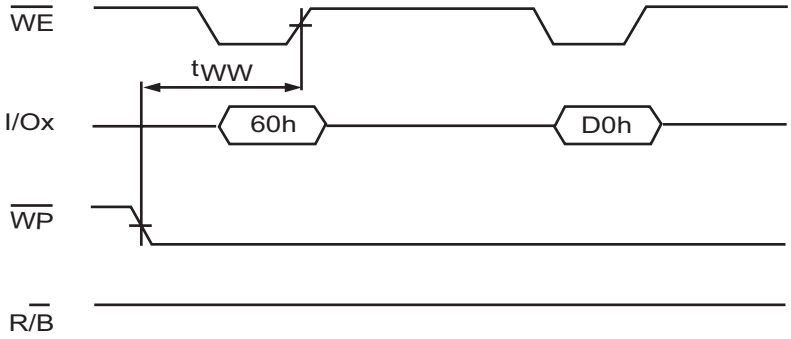


Figure 36: Disable Erasing

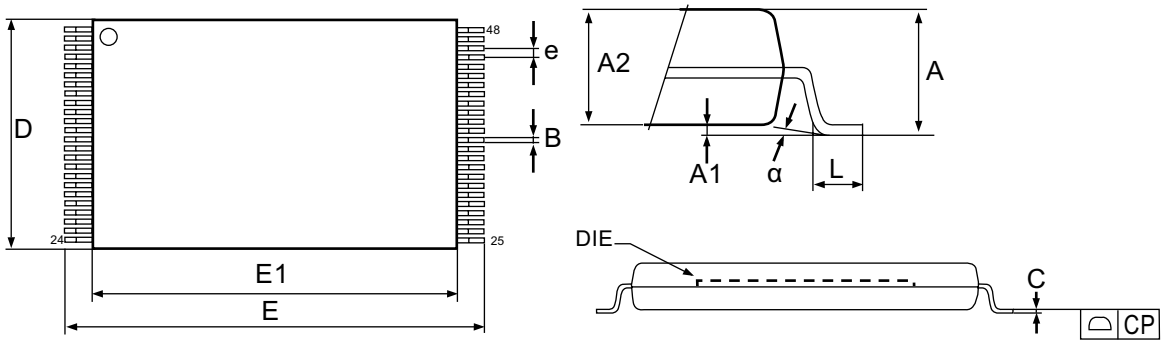


Figure 37: 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Outline

Symbol	millimeters		
	Min	Typ	Max
A			1.200
A1	0.050		0.150
A2	0.980		1.030
B	0.170		0.250
C	0.100		0.200
CP			0.100
D	11.910	12.000	12.120
E	19.900	20.000	20.100
E1	18.300	18.400	18.500
e		0.500	
L	0.500		0.680
alpha	0		5

Table 24: 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Mechanical Data

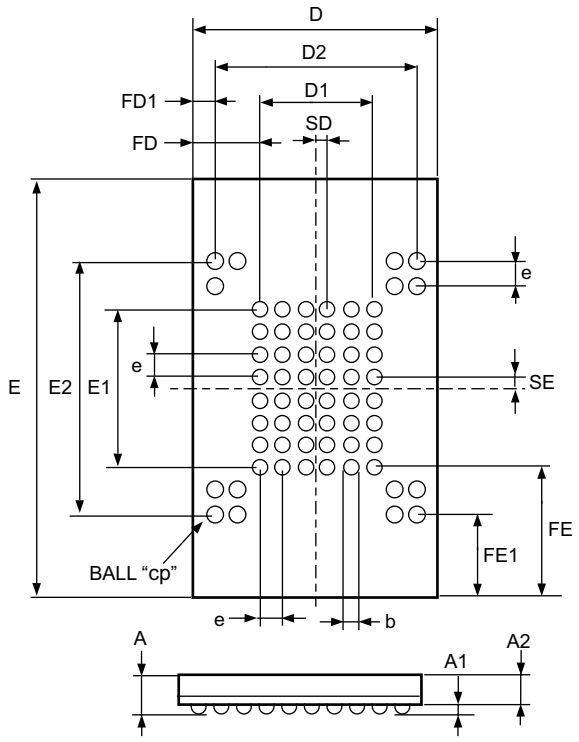


Figure 38: 63-ball FBGA - 9 x 11 ball array 0.8mm pitch, Pakage Outline

NOTE: Drawing is not to scale.

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.90	1.00
A1	0.25	0.30	0.35
A2	0.55	0.60	0.65
b	0.40	0.45	0.50
D	8.90	9.00	9.10
D1		4.00	
D2		7.20	
E	10.90	11.00	11.10
E1		5.60	
E2		8.80	
e		0.80	
FD		2.50	
FD1		0.90	
FE		2.70	
FE1		1.10	
SD		0.40	
SE		0.40	

Table 25: 63-ball FBGA - 9 x 11 ball array 0.8mm pitch, Pakage Mechanical Data

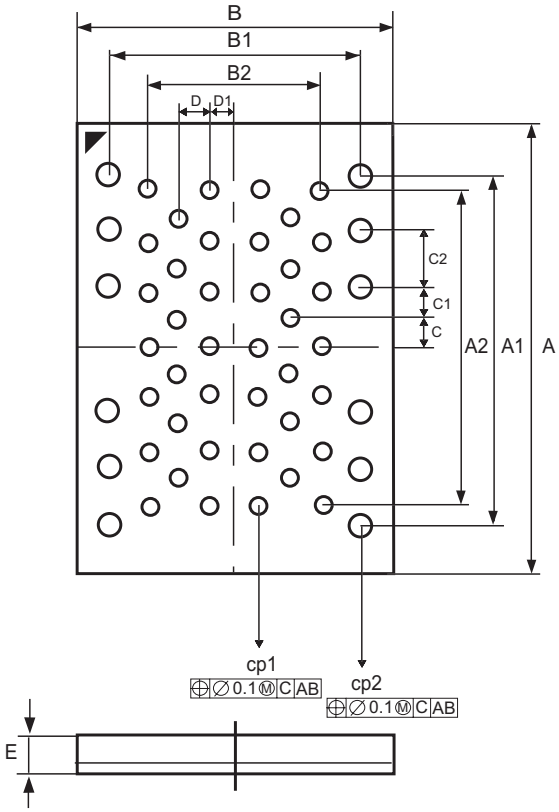


Figure 39: 52-ULGA, 12 x 17mm, Package Outline
(Top view through package)

Symbol	millimeters		
	Min	Typ	Max
A	16.90	17.00	17.10
A1		13.00	
A2		12.00	
B	11.90	12.00	12.10
B1		10.00	
B2		6.00	
C		1.00	
C1		1.50	
C2		2.00	
D		1.00	
D1		1.00	
E			0.65
CP1	0.65	0.70	0.75
CP2	0.95	1.00	1.05

Table 26: 52-ULGA, 12 x 17mm, Package Mechanical Data

MARKING INFORMATION - TSOP1 / FBGA / ULGA

Packag	Marking Example
TSOP1 / FBGA / ULGA	hynix K O R H Y 2 7 U F x x 2 G 2 B x x x x Y W W x x

- hynix	: Hynix Symbol
- KOR	: Origin Country
- HY27UFxx2G2B xxxx	: Part Number
HY: Hynix	
27: NAND Flash	
U: Power Supply	: U(2.7V~3.6V)
F: Classification	: Single Level Cell+Single Die+Large Block
xx : Bit Organization	: 08(x8), 16(x16)
2G: Density	: 2Gbit
2: Mode	: 2(1nCE & 1R/nB; Sequential Row Read Disable)
B: Version	: 3rd Generation
x: Package Type	: T(48-TSOP1), F(63-FBGA), U(52-ULGA)
x: Package Material	: Blank(Normal), P(Lead Free)
x: Operating Temperature	: C(0℃~70℃), I(-40℃~85℃)
x: Bad Block	: B(Included Bad Block), S(1~5 Bad Block), P(All Good Block)
- Y: Year (ex: 5=year 2005, 6= year 2006)	
- ww: Work Week (ex: 12= work week 12)	
- xx: Process Code	
Note	
- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item

ISL1208

I^2C® Real Time Clock/Calendar

Data Sheet | July 29, 2005 | FN8085.3

Low Power RTC with Battery Backed SRAM

The ISL1208 device is a low power real time clock with timing and crystal compensation, clock/calendar, power fail indicator, periodic or polled alarm, intelligent battery backup switching and battery-backed user SRAM.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

Ordering Information

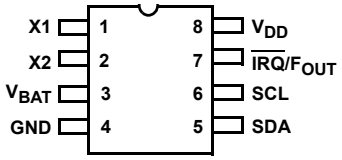
PART NUMBER	MARKING	V_{DD} RANGE	TEMP. RANGE (°C)	PACKAGE
ISL1208IU8	AGS YWW	2.7V to 5.5V	-40 to +85	8 Ld MSOP
ISL1208IU8-TK	AGS YWW	2.7V to 5.5V	-40 to +85	8 Ld MSOP Tape and Reel
ISL1208IU8Z (See Note)	ANW YWW	2.7V to 5.5V	-40 to +85	8 Ld MSOP (Pb-free)
ISL1208IU8Z-TK (See Note)	ANW YWW	2.7V to 5.5V	-40 to +85	8 Ld MSOP Tape and Reel (Pb-free)
ISL1208IB8	1208 YWW	2.7V to 5.5V	-40 to +85	8 Ld SOIC
ISL1208IB8-TK	1208 YWW	2.7V to 5.5V	-40 to +85	8 Ld SOIC Tape and Reel
ISL1208IB8Z (See Note)	1208 YWWZ	2.7V to 5.5V	-40 to +85	8 Ld SOIC (Pb-free)
ISL1208IB8Z-TK (See Note)	1208 YWWZ	2.7V to 5.5V	-40 to +85	8 Ld SOIC Tape and Reel (Pb-free)

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

* Contact Factory for availability.

Pinout

ISL1208
(8-PIN MSOP, SOIC)
TOP VIEW



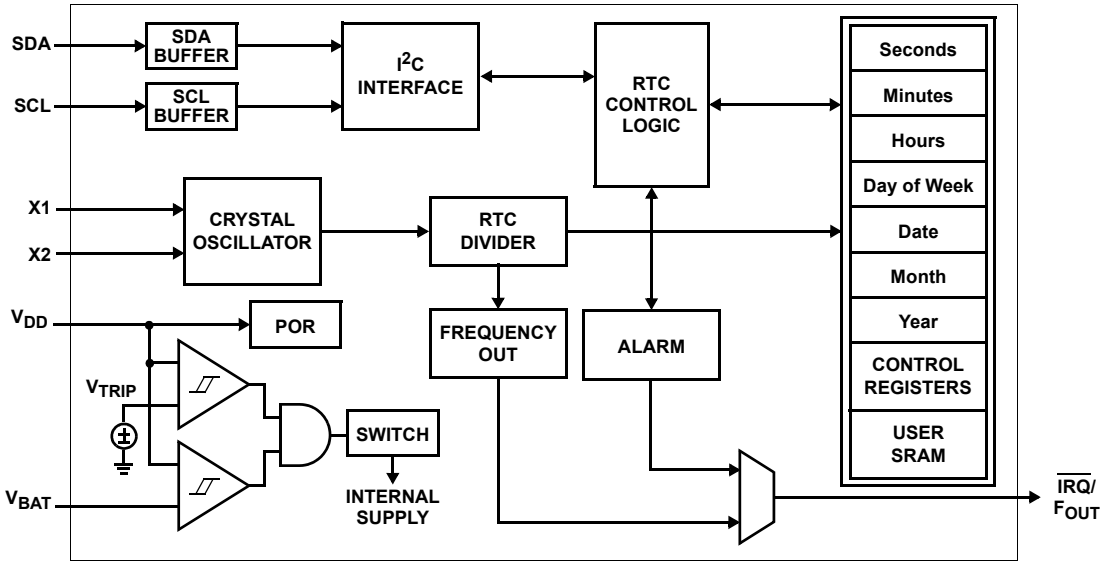
Features

- Real Time Clock/Calendar
  - Tracks Time in Hours, Minutes, and Seconds
  - Day of the Week, Day, Month, and Year
- 15 Selectable Frequency Outputs
- Single Alarm
  - Settable to the Second, Minute, Hour, Day of the Week, Day, or Month
  - Single Event or Pulse Interrupt Mode
- Automatic Backup to Battery or Super Cap
- Power Failure Detection
- On-Chip Oscillator Compensation
- 2 Bytes Battery-Backed User SRAM
- I^2C Interface
  - 400kHz Data Transfer Rate
- 400nA Battery Supply Current
- Same Pin Out as ST M41Txx and Maxim DS13xx Devices
- Small Package Options
  - 8 Ld MSOP and SOIC Packages
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Utility Meters
- HVAC Equipment
- Audio/Video Components
- Set Top Box/Television
- Modems
- Network Routers, Hubs, Switches, Bridges
- Cellular Infrastructure Equipment
- Fixed Broadband Wireless Equipment
- Pagers/PDA
- POS Equipment
- Test Meters/Fixtures
- Office Automation (Copiers, Fax)
- Home Appliances
- Computer Products
- Other Industrial/Medical/Automotive

Block Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	X1	The X1 pin is the input of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. X1 can also be driven directly from a 32.768kHz source.
2	X2	The X2 pin is the output of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal.
3	V_{BAT}	This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin should be tied to ground if not used.
4	GND	Ground.
5	SDA	Serial Data (SDA) is a bidirectional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR'ed with other open drain or open collector outputs.
6	SCL	The Serial Clock (SCL) input is used to clock all serial data into and out of the device.
7	$\overline{IRQ}/F_{OUT}$	Interrupt Output/Frequency Output is a multi-functional pin that can be used as interrupt or frequency output pin. The function is set via the configuration register.
8	V_{DD}	Power supply.

Absolute Maximum Ratings

Voltage on V_{DD}, V_{BAT}, SCL, SDA, and $\overline{IRQ}$ pins (respect to ground) . . . . . -0.5V to 7.0V
Voltage on X1 and X2 pins (respect to ground) . . . . . -0.5V to V_{DD} + 0.5 (V_{DD} Mode), -0.5V to V_{BAT} + 0.5 (V_{BAT} Mode)
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Operating Characteristics – RTC

Temperature = -40°C to +85°C, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS	NOTES
V_{DD}	Main Power Supply		2.7		5.5	V	
V_{BAT}	Battery Supply Voltage		1.8		5.5	V	
I_{DD1}	Supply Current	V_{DD} = 5V		2	6	µA	1, 2
		V_{DD} = 3V		1.2	4	µA	
I_{DD2}	Supply Current With I^2C Active	V_{DD} = 5V		40	120	µA	1, 2
I_{DD3}	Supply Current (Low Power Mode)	V_{DD} = 5V, LPMODE = 1		1.4	5	µA	1
I_{BAT}	Battery Supply Current	V_{BAT} = 3V		400	950	nA	1
I_{LI}	Input Leakage Current on SCL			100		nA	
I_{LO}	I/O Leakage Current on SDA			100		nA	
V_{TRIP}	V_{BAT} Mode Threshold		1.6	2.2	2.6	V	
$V_{TRIPHYS}$	V_{TRIP} Hysteresis		10	30	75	mV	
V_{BATHYS}	V_{BAT} Hysteresis		15	50	100	mV	
$\overline{IRQ}$/F_{OUT}							
V_{OL}	Output Low Voltage	V_{DD} = 5V, I_{OL} = 3mA			0.4	V	
		V_{DD} = 2.7V, I_{OL} = 1mA			0.4	V	

Power-Down Timing

Temperature = -40°C to +85°C, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS	NOTES
$V_{DD\ SR-}$	V_{DD} Negative Slewrate				10	V/ms	3

Serial Interface Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS	NOTES
SERIAL INTERFACE SPECS							
V_{IL}	SDA and SCL input buffer LOW voltage		-0.3		0.3 x V_{DD}	V	
V_{IH}	SDA and SCL input buffer HIGH voltage		0.7 x V_{DD}		V_{DD} + 0.3	V	
Hysteresis	SDA and SCL input buffer hysteresis		0.05 x V_{DD}			V	
V_{OL}	SDA output buffer LOW voltage, sinking 3mA		0		0.4	V	

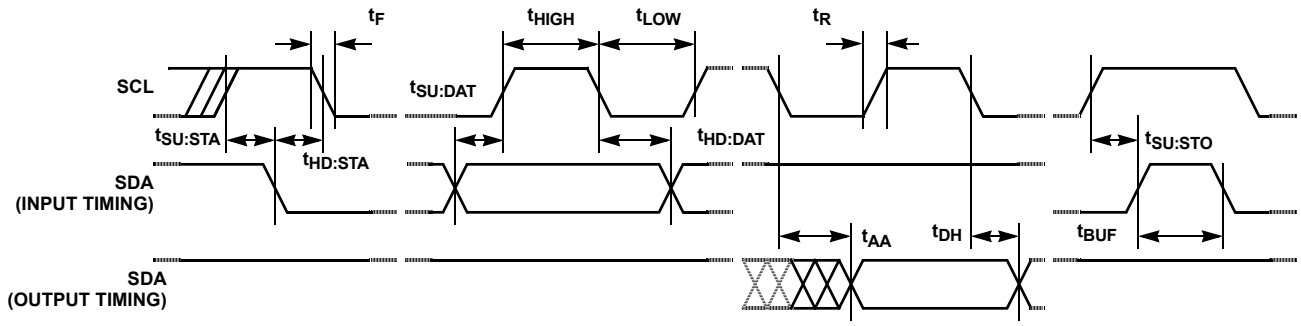
Serial Interface Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS	NOTES
Cpin	SDA and SCL pin capacitance	T_A = 25°C, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF	
f_{SCL}	SCL frequency				400	kHz	
t_{IN}	Pulse width suppression time at SDA and SCL inputs	Any pulse narrower than the max spec is suppressed.			50	ns	
t_{AA}	SCL falling edge to SDA output data valid	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window.			900	ns	
t_{BUF}	Time the bus must be free before the start of a new transmission	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition.	1300			ns	
t_{LOW}	Clock LOW time	Measured at the 30% of V_{DD} crossing.	1300			ns	
t_{HIGH}	Clock HIGH time	Measured at the 70% of V_{DD} crossing.	600			ns	
$t_{SU:STA}$	START condition setup time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}.	600			ns	
$t_{HD:STA}$	START condition hold time	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}.	600			ns	
$t_{SU:DAT}$	Input data setup time	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}	100			ns	
$t_{HD:DAT}$	Input data hold time	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window.	0		900	ns	
$t_{SU:STO}$	STOP condition setup time	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}.	600			ns	
$t_{HD:STO}$	STOP condition hold time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}.	600			ns	
t_{DH}	Output data hold time	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window.	0			ns	
t_R	SDA and SCL rise time	From 30% to 70% of V_{DD}	20 + 0.1 x Cb		300	ns	
t_F	SDA and SCL fall time	From 70% to 30% of V_{DD}	20 + 0.1 x Cb		300	ns	
Cb	Capacitive loading of SDA or SCL	Total on-chip and off-chip	10		400	pF	
Rpu	SDA and SCL bus pull-up resistor off-chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2~2.5kΩ. For Cb = 40pF, max is about 15~20kΩ	1			kΩ	

NOTES:

1. $\overline{IRQ}$ & F_{OUT} Inactive.
2. LPMODE = 0 (default).
3. In order to ensure proper timekeeping, the $V_{DD\ SR-}$ specification must be followed.
4. Typical values are for T = 25°C and 3.3V supply voltage.

SDA vs SCL Timing



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Typical Performance Curves Temperature is 25°C unless otherwise specified

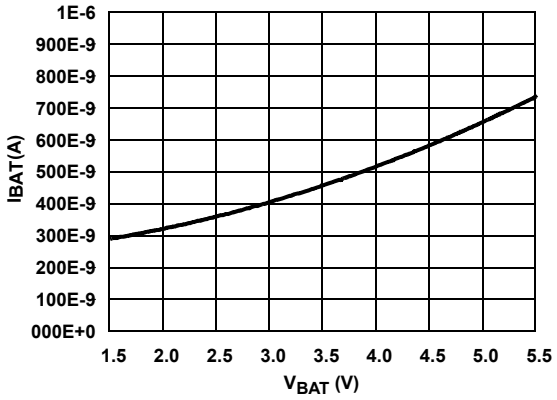


FIGURE 1. I_{BAT} vs V_{BAT}

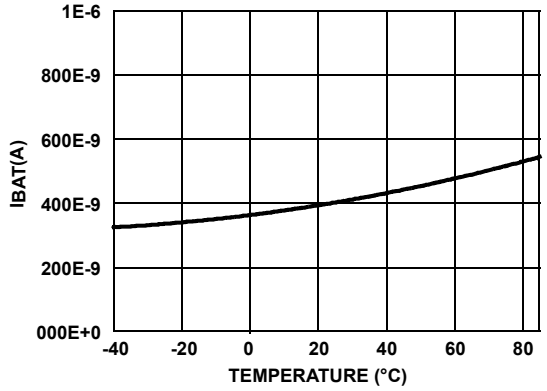


FIGURE 2. I_{BAT} vs TEMPERATURE AT V_{BAT} = 3V

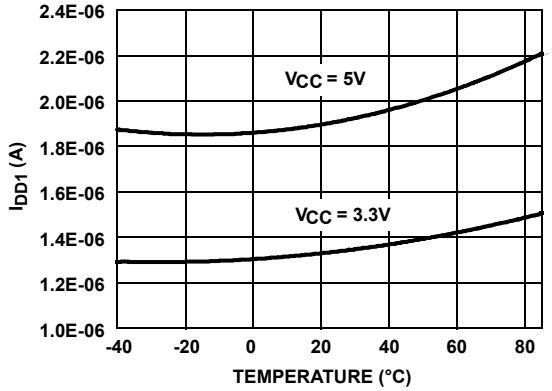


FIGURE 3. I_{DD1} vs TEMPERATURE

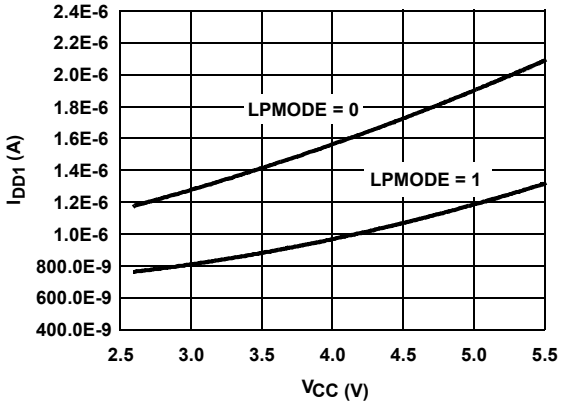


FIGURE 4. I_{DD1} vs V_{CC} WITH LPMODE ON & OFF

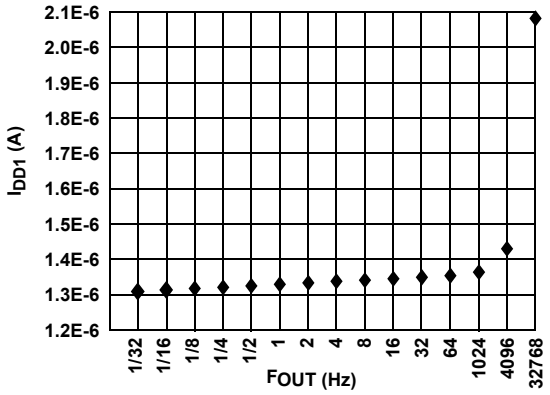


FIGURE 5. I_{DD1} vs F_{OUT} AT V_{DD} = 3.3V

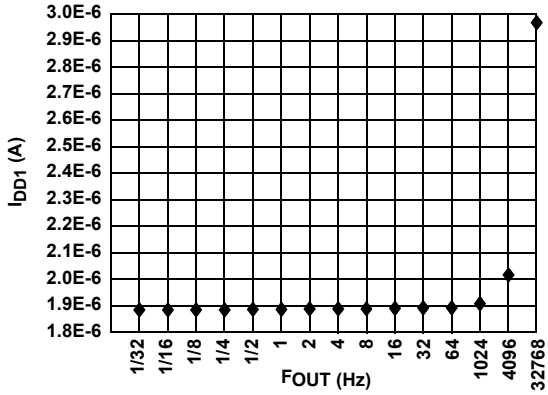


FIGURE 6. I_{DD1} vs F_{OUT} AT V_{DD} = 5V

EQUIVALENT AC OUTPUT LOAD CIRCUIT FOR V_{DD} = 5V

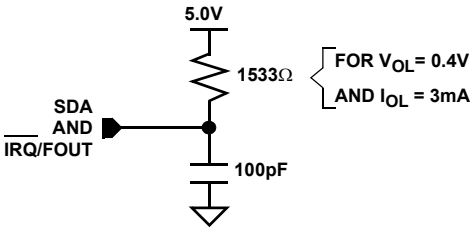


FIGURE 7. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH V_{DD} = 5.0V

General Description

The ISL1208 device is a low power real time clock with timing and crystal compensation, clock/calendar, power fail indicator, periodic or polled alarm, intelligent battery backup switching, and battery-backed user SRAM.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

The ISL1208's powerful alarm can be set to any clock/calendar value for a match. For example, every minute, every Tuesday or at 5:23 AM on March 21. The alarm status is available by checking the Status Register, or the device can be configured to provide a hardware interrupt via the IRQ pin. There is a repeat mode for the alarm allowing a periodic interrupt every minute, every hour, every day, etc.

The device also offers a backup power input pin. This V_{BAT} pin allows the device to be backed up by battery or SuperCap with automatic switchover from V_{DD} to V_{BAT}. The entire ISL1208 device is fully operational from 2.0V to 5.5V and the clock/calendar portion of the device remains fully operational down to 1.8V (Standby Mode).

Pin Description

X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal is used with the ISL1208 to supply a timebase for the real time clock. Internal compensation circuitry provides high accuracy over the operating temperature range from -40°C to +85°C. This oscillator compensation network can be used to calibrate the crystal timing accuracy over temperature either during manufacturing or with an external temperature sensor and microcontroller for active compensation. The device can also be driven directly from a 32.768kHz source at pin X1.

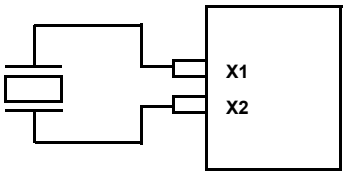


FIGURE 8. RECOMMENDED CRYSTAL CONNECTION

V_{BAT}

This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin can be connected to a battery, a Super Cap or tied to ground if not used.

$\overline{IRQ}/F_{OUT}$ (Interrupt Output/Frequency Output)

This dual function pin can be used as an interrupt or frequency output pin. The $\overline{IRQ}/F_{OUT}$ mode is selected via the frequency out control bits of the control/status register.

- **Interrupt Mode.** The pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action. It is an open drain active low output.
- **Frequency Output Mode.** The pin outputs a clock signal which is related to the crystal frequency. The frequency output is user selectable and enabled via the I^2C bus. It is an open drain active low output.

Serial Clock (SCL)

The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). It is disabled when the backup power supply on the V_{BAT} pin is activated to minimize power consumption.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be ORed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode.

An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz I^2C interface speeds. It is disabled when the backup power supply on the V_{BAT} pin is activated.

V_{DD}, GND

Chip power supply and ground pins. The device will operate with a power supply from 2.0V to 5.5VDC. A 0.1µF capacitor is recommended on the V_{DD} pin to ground.

Functional Description

Power Control Operation

The power control circuit accepts a V_{DD} and a V_{BAT} input. Many types of batteries can be used with Intersil RTC products. For example, 3.0V or 3.6V Lithium batteries are appropriate, and battery sizes are available that can power

the ISL1208 for up to 10 years. Another option is to use a Super Cap for applications where V_{DD} is interrupted for up to a month. See the Applications Section for more information.

Normal Mode (V_{DD}) to Battery Backup Mode (V_{BAT})

To transition from the V_{DD} to V_{BAT} mode, both of the following conditions must be met:

Condition 1:

$V_{DD} < V_{BAT} - V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

Condition 2:

$V_{DD} < V_{TRIP}$
where $V_{TRIP} \approx 2.2V$

Battery Backup Mode (V_{BAT}) to Normal Mode (V_{DD})

The ISL1208 device will switch from the V_{BAT} to V_{DD} mode when one of the following conditions occurs:

Condition 1:

$V_{DD} > V_{BAT} + V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

Condition 2:

$V_{DD} > V_{TRIP} + V_{TRIPHYS}$
where $V_{TRIPHYS} \approx 30mV$

These power control situations are illustrated in Figures 9 and 10.

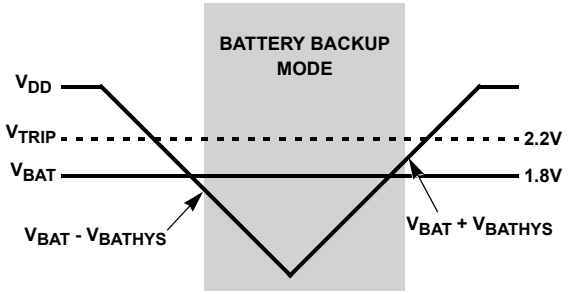


FIGURE 9. BATTERY SWITCHOVER WHEN $V_{BAT} < V_{TRIP}$

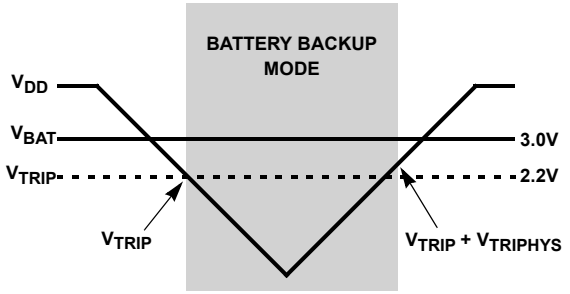


FIGURE 10. BATTERY SWITCHOVER WHEN $V_{BAT} > V_{TRIP}$

The I^2C bus is deactivated in battery backup mode to provide lower power. Aside from this, all RTC functions are operational during battery backup mode. Except for SCL and SDA, all the inputs and outputs of the ISL1208 are active during battery backup mode unless disabled via the control register. The User SRAM is operational in battery backup mode down to 2V.

Power Failure Detection

The ISL1208 provides a Real Time Clock Failure Bit (RTCF) to detect total power failure. It allows users to determine if the device has powered up after having lost all power to the device (both V_{DD} and V_{BAT}).

Low Power Mode

The normal power switching of the ISL1208 is designed to switch into battery backup mode only if the V_{DD} power is lost. This will ensure that the device can accept a wide range of backup voltages from many types of sources while reliably switching into backup mode. Another mode, called Low Power Mode, is available to allow direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below V_{TRIP}. Since the additional monitoring of V_{DD} vs V_{TRIP} is no longer needed, that circuitry is shut down and less power is used while operating from V_{DD}. Power savings are typically 600nA at V_{DD} = 5V. Low Power Mode is activated via the LPMODE bit in the control and status registers.

Low Power Mode is useful in systems where V_{DD} is normally higher than V_{BAT} at all times. The device will switch from V_{DD} to V_{BAT} when V_{DD} drops below V_{BAT}, with about 50mV of hysteresis to prevent any switchback of V_{DD} after switchover. In a system with a V_{DD} = 5V and backup lithium battery of V_{BAT} = 3V, Low Power Mode can be used. However, it is not recommended to use Low Power Mode in a system with V_{DD} = 3.3V ±10%, $V_{BAT} \geq 3.0V$, and when there is a finite I-R voltage drop in the V_{DD} line.

InterSeal™ Battery Saver

The ISL1208 has the InterSeal™ Battery Saver which prevents initial battery current drain before it is first used. For example, battery-backed RTCs are commonly packaged on a board with a battery connected. In order to preserve battery life, the ISL1208 will not draw any power from the battery source until after the device is first powered up from the V_{DD} source. Thereafter, the device will switchover to battery backup mode whenever V_{DD} power is lost.

Real Time Clock Operation

The Real Time Clock (RTC) uses an external 32.768kHz quartz crystal to maintain an accurate internal representation of second, minute, hour, day of week, date, month, and year. The RTC also has leap-year correction. The clock also corrects for months having fewer than 31 days and has a bit that controls 24 hour or AM/PM format. When the ISL1208 powers up after the loss of both V_{DD} and V_{BAT}, the clock will

not begin incrementing until at least one byte is written to the clock register.

Accuracy of the Real Time Clock

The accuracy of the Real Time Clock depends on the frequency of the quartz crystal that is used as the time base for the RTC. Since the resonant frequency of a crystal is temperature dependent, the RTC performance will also be dependent upon temperature. The frequency deviation of the crystal is a function of the turnover temperature of the crystal from the crystal's nominal frequency. For example, a ~20ppm frequency deviation translates into an accuracy of ~1 minute per month. These parameters are available from the crystal manufacturer. The ISL1208 provides on-chip crystal compensation networks to adjust load capacitance to tune oscillator frequency from -94ppm to +140ppm. For more detailed information see the Application Section.

Single Event and Interrupt

The alarm mode is enabled via the ALME bit. Choosing single event or interrupt alarm mode is selected via the IM bit. Note that when the frequency output function is enabled, the alarm function is disabled.

The standard alarm allows for alarms of time, date, day of the week, month, and year. When a time alarm occurs in single event mode, an $\overline{IRQ}$ pin will be pulled low and the alarm status bit (ALM) will be set to "1".

The pulsed interrupt mode allows for repetitive or recurring alarm functionality. Hence, once the alarm is set, the device will continue to alarm for each occurring match of the alarm and present time. Thus, it will alarm as often as every minute (if only the nth second is set) or as infrequently as once a year (if at least the nth month is set). During pulsed interrupt mode, the $\overline{IRQ}$ pin will be pulled low for 250ms and the alarm status bit (ALM) will be set to "1".

NOTE: The ALM bit can be reset by the user or cleared automatically using the auto reset mode (see ARST bit).

The alarm function can be enabled/disabled during battery backup mode using the FOBATB bit. For more information on the alarm, please see the Alarm Registers Description.

Frequency Output Mode

The ISL1208 has the option to provide a frequency output signal using the $\overline{IRQ}/F_{OUT}$ pin. The frequency output mode is set by using the FO bits to select 15 possible output frequency values from 0 to 32kHz. The frequency output can be enabled/disabled during battery backup mode using the FOBATB bit.

General Purpose User SRAM

The ISL1208 provides 2 bytes of user SRAM. The SRAM will continue to operate in battery backup mode. However, it should be noted that the I^2C bus is disabled in battery backup mode.

I^2C Serial Interface

The ISL1208 has an I^2C serial bus interface that provides access to the control and status registers and the user SRAM. The I^2C serial interface is compatible with other industry I^2C serial bus protocols using a bidirectional data signal (SDA) and a clock signal (SCL).

Oscillator Compensation

The ISL1208 provides the option of timing correction due to temperature variation of the crystal oscillator for either manufacturing calibration or active calibration. The total possible compensation is typically -94ppm to +140ppm. Two compensation mechanisms that are available are as follows:

1. An analog trimming (ATR) register that can be used to adjust individual on-chip digital capacitors for oscillator capacitance trimming. The individual digital capacitor is selectable from a range of 9pF to 40.5pF (based upon 32.758kHz). This translates to a calculated compensation of approximately -34ppm to +80ppm. (See ATR description.)
2. A digital trimming register (DTR) that can be used to adjust the timing counter by ±60ppm. (See DTR description.)

Also provided is the ability to adjust the crystal capacitance when the ISL1208 switches from V_{DD} to battery backup mode. (See Battery Mode ATR Selection for more details.)

Register Descriptions

The battery-backed registers are accessible following a slave byte of "1101111x" and reads or writes to addresses [00h:13h]. The defined addresses and default values are described in the Table 1. Address 09h is not used. Reads or writes to 09h will not affect operation of the device but should be avoided.

REGISTER ACCESS

The contents of the registers can be modified by performing a byte or a page write operation directly to any register address.

The registers are divided into 4 sections. These are:

1. Real Time Clock (7 bytes): Address 00h to 06h.
2. Control and Status (5 bytes): Address 07h to 0Bh.
3. Alarm (6 bytes): Address 0Ch to 11h.
4. User SRAM (2 bytes): Address 12h to 13h.

There are no addresses above 13h.

Write capability is allowable into the RTC registers (00h to 06h) only when the WRTC bit (bit 4 of address 07h) is set to “1”. **A multi-byte read or write operation is limited to one section per operation.** Access to another section requires a new operation. A read or write can begin at any address within the section.

A register can be read by performing a random read at any address at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. For the RTC and Alarm registers, the read instruction latches all clock registers into a buffer, so an update of the clock does not change the time being read. A sequential read will not result in the output of data from the memory array. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read, the address remains at the previous address +1 so the user can execute a current address read and continue reading the next register.

It is not necessary to set the WRTC bit prior to writing into the control and status, alarm, and user SRAM registers.

TABLE 1. REGISTER MEMORY MAP

ADDR.	SECTION	REG NAME	BIT								RANGE	DEFAULT
			7	6	5	4	3	2	1	0		
00h	RTC	SC	0	SC22	SC21	SC20	SC13	SC12	SC11	SC10	0-59	00h
01h		MN	0	MN22	MN21	MN20	MN13	MN12	MN11	MN10	0-59	00h
02h		HR	MIL	0	HR21	HR20	HR13	HR12	HR11	HR10	0-23	00h
03h		DT	0	0	DT21	DT20	DT13	DT12	DT11	DT10	1-31	00h
04h		MO	0	0	0	MO20	MO13	MO12	MO11	MO10	1-12	00h
05h		YR	YR23	YR22	YR21	YR20	YR13	YR12	YR11	YR10	0-99	00h
06h		DW	0	0	0	0	0	DW2	DW1	DW0	0-6	00h
07h	Control and Status	SR	ARST	XTOSCB	Reserved	WRTC	Reserved	ALM	BAT	RTCF	N/A	01h
08h		INT	IM	ALME	LPMODE	FOBATB	FO3	FO2	FO1	FO0	N/A	00h
09h		Reserved									N/A	00h
0Ah		ATR	BMATR1	BMATR0	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0	N/A	00h
0Bh		DTR	Reserved					DTR2	DTR1	DTR0	N/A	00h
0Ch	Alarm	SCA	ESCA	ASC22	ASC21	ASC20	ASC13	ASC12	ASC11	ASC10	00-59	00h
0Dh		MNA	EMNA	AMN22	AMN21	AMN20	AMN13	AMN12	AMN11	AMN10	00-59	00h
0Eh		HRA	EHRA	0	AHR21	AHR20	AHR13	AHR12	AHR11	AHR10	0-23	00h
0Fh		DTA	EDTA	0	ADT21	ADT20	ADT13	ADT12	ADT11	ADT10	1-31	00h
10h		MOA	EMOA	0	0	AMO20	AMO13	AMO12	AMO11	AMO10	1-12	00h
11h		DWA	EDWA	0	0	0	0	ADW12	ADW11	ADW10	0-6	00h
12h	User	USR1	USR17	USR16	USR15	USR14	USR13	USR12	USR11	USR10	N/A	00h
13h		USR2	USR27	USR26	USR25	USR24	USR23	USR22	USR21	USR20	N/A	00h

Real Time Clock Registers

Addresses [00h to 06h]

RTC REGISTERS (SC, MN, HR, DT, MO, YR, DW)

These registers depict BCD representations of the time. As such, SC (Seconds) and MN (Minutes) range from 0 to 59, HR (Hour) can either be a 12-hour or 24-hour mode, DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (Year) is 0 to 99, and DW (Day of the Week) is 0 to 6.

The DW register provides a Day of the Week status and uses three bits DW2 to DW0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-… The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The default value is defined as “0”.

24 HOUR TIME

If the MIL bit of the HR register is “1”, the RTC uses a 24-hour format. If the MIL bit is “0”, the RTC uses a 12-hour format and HR21 bit functions as an AM/PM indicator with a “1” representing PM. The clock defaults to 12-hour format time with HR21 = “0”.

LEAP YEARS

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year, the year 2100 is not. The ISL1208 does not correct for the leap year in the year 2100.

Control and Status Registers

Addresses [07h to 0Bh]

The Control and Status Registers consist of the Status Register, Interrupt and Alarm Register, Analog Trimming and Digital Trimming Registers.

Status Register (SR)

The Status Register is located in the memory map at address 07h. This is a volatile register that provides either control or status of RTC failure, battery mode, alarm trigger, write protection of clock counter, crystal oscillator enable and auto reset of status bits.

TABLE 2. STATUS REGISTER (SR)

ADDR	7	6	5	4	3	2	1	0
07h	ARST	XTOSCB	reserved	WRTC	reserved	ALM	BAT	RTCF
Default	0	0	0	0	0	0	0	0

REAL TIME CLOCK FAIL BIT (RTCF)

This bit is set to a “1” after a total power failure. This is a read only bit that is set by hardware (ISL1208 internally) when the device powers up after having lost all power to the device. The bit is set regardless of whether V_{DD} or V_{BAT} is applied first. The loss of only one of the supplies does not set the RTCF bit to “1”. The first valid write to the RTC section after a complete power failure resets the RTCF bit to “0” (writing one byte is sufficient).

BATTERY BIT (BAT)

This bit is set to a “1” when the device enters battery backup mode. This bit can be reset either manually by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”.

ALARM BIT (ALM)

These bits announce if the alarm matches the real time clock. If there is a match, the respective bit is set to “1”. This bit can be manually reset to “0” by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”.

NOTE: An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

WRITE RTC ENABLE BIT (WRTC)

The WRTC bit enables or disables write capability into the RTC Timing Registers. The factory default setting of this bit is “0”. Upon initialization or power up, the WRTC must be set to “1” to enable the RTC. Upon the completion of a valid write (STOP), the RTC starts counting. The RTC internal 1Hz signal is synchronized to the STOP condition during a valid write cycle.

CRYSTAL OSCILLATOR ENABLE BIT (XTOSCB)

This bit enables/disables the internal crystal oscillator. When the XTOSCB is set to “1”, the oscillator is disabled, and the X1 pin allows for an external 32kHz signal to drive the RTC. The XTOSCB bit is set to “0” on powerup.

AUTO RESET ENABLE BIT (ARST)

This bit enables/disables the automatic reset of the BAT and ALM status bits only. When ARST bit is set to “1”, these status bits are reset to “0” after a valid read of the respective status register (with a valid STOP condition). When the ARST is cleared to “0”, the user must manually reset the BAT and ALM bits.

Interrupt Control Register (INT)

TABLE 3. INTERRUPT CONTROL REGISTER (INT)

ADDR	7	6	5	4	3	2	1	0
08h	IM	ALME	LPMODE	FOBATB	FO3	FO2	FO1	FO0
Default	0	0	0	0	0	0	0	0

FREQUENCY OUT CONTROL BITS (FO <3:0>)

These bits enable/disable the frequency output function and select the output frequency at the $\overline{IRQ}/F_{OUT}$ pin. See Table 4 for frequency selection. When the frequency mode is enabled, it will override the alarm mode at the $\overline{IRQ}/F_{OUT}$ pin.

TABLE 4. FREQUENCY SELECTION OF F_{OUT} PIN

FREQUENCY, F_{OUT}	UNITS	FO3	FO2	FO1	FO0
0	Hz	0	0	0	0
32768	Hz	0	0	0	1
4096	Hz	0	0	1	0
1024	Hz	0	0	1	1
64	Hz	0	1	0	0
32	Hz	0	1	0	1
16	Hz	0	1	1	0
8	Hz	0	1	1	1
4	Hz	1	0	0	0
2	Hz	1	0	0	1
1	Hz	1	0	1	0
1/2	Hz	1	0	1	1
1/4	Hz	1	1	0	0
1/8	Hz	1	1	0	1
1/16	Hz	1	1	1	0
1/32	Hz	1	1	1	1

FREQUENCY OUTPUT AND INTERRUPT BIT (FOBATB)

This bit enables/disables the $F_{OUT}/\overline{IRQ}$ pin during battery backup mode (i.e. V_{BAT} power source active). When the FOBATB is set to "1" the $F_{OUT}/\overline{IRQ}$ pin is disabled during battery backup mode. This means that both the frequency output and alarm output functions are disabled. When the FOBATB is cleared to "0", the $F_{OUT}/\overline{IRQ}$ pin is enabled during battery backup mode.

LOW POWER MODE BIT (LPMODE)

This bit enables/disables low power mode. With LPMODE = "0", the device will be in normal mode and the V_{BAT} supply will be used when $V_{DD} < V_{BAT} - V_{BATHYS}$ and $V_{DD} < V_{TRIP}$. With LPMODE = "1", the device will be in low power mode and the V_{BAT} supply will be used when $V_{DD} < V_{BAT} - V_{BATHYS}$. There is a supply current saving of about 600nA when using LPMODE = "1" with V_{DD} = 5V. (See Typical Performance Curves: I_{DD} vs V_{CC} with LPMODE ON & OFF.)

ALARM ENABLE BIT (ALME)

This bit enables/disables the alarm function. When the ALME bit is set to "1", the alarm function is enabled. When the ALME is cleared to "0", the alarm function is disabled. The alarm function can operate in either a single event alarm or a periodic interrupt alarm (see IM bit).

NOTE: When the frequency output mode is enabled, the alarm function is disabled.

INTERRUPT/ALARM MODE BIT (IM)

This bit enables/disables the interrupt mode of the alarm function. When the IM bit is set to "1", the alarm will operate in the interrupt mode, where an active low pulse width of 250ms will appear at the $\overline{IRQ}/F_{OUT}$ pin when the RTC is triggered by the alarm as defined by the alarm registers (0Ch to 11h). When the IM bit is cleared to "0", the alarm will operate in standard mode, where the $\overline{IRQ}/F_{OUT}$ pin will be tied low until the ALM status bit is cleared to "0".

IM BIT	INTERRUPT/ALARM FREQUENCY
0	Single Time Event Set By Alarm
1	Repetitive/Recurring Time Event Set By Alarm

Analog Trimming Register

ANALOG TRIMMING REGISTER (ATR<5:0>)

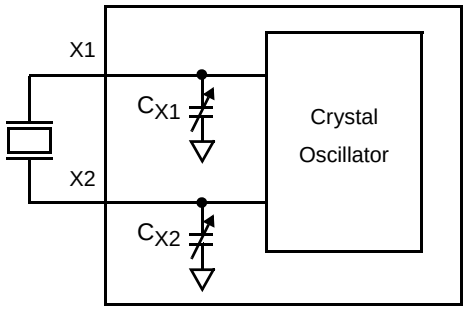


FIGURE 11. DIAGRAM OF ATR

Six analog trimming bits, **ATR0** to **ATR5**, are provided in order to adjust the on-chip load capacitance value for frequency compensation of the RTC. Each bit has a different weight for capacitance adjustment. For example, using a Citizen CFS-206 crystal with different ATR bit combinations provides an estimated ppm adjustment range from -34 to +80ppm to the nominal frequency compensation. The combination of analog and digital trimming can give up to -94 to +140ppm of total adjustment.

The effective on-chip series load capacitance, C_{LOAD}, ranges from 4.5pF to 20.25pF with a mid-scale value of 12.5pF (default). C_{LOAD} is changed via two digitally controlled capacitors, C_{X1} and C_{X2}, connected from the X1

and X2 pins to ground (see Figure 11). The value of C_{X1} and C_{X2} is given by the following formula:

$$C_X = (16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9)pF$$

The effective series load capacitance is the combination of C_{X1} and C_{X2}:

$$C_{LOAD} = \frac{1}{\left(\frac{1}{C_{X1}} + \frac{1}{C_{X2}}\right)}$$

$$C_{LOAD} = \left(\frac{16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9}{2}\right)pF$$

For example, C_{LOAD}(ATR=00000) = 12.5pF, C_{LOAD}(ATR=100000) = 4.5pF, and C_{LOAD}(ATR=011111) = 20.25pF. The entire range for the series combination of load capacitance goes from 4.5pF to 20.25pF in 0.25pF steps. Note that these are typical values.

BATTERY MODE ATR SELECTION (BMATR <1:0>)

Since the accuracy of the crystal oscillator is dependent on the V_{DD}/V_{BAT} operation, the ISL1208 provides the capability to adjust the capacitance between V_{DD} and V_{BAT} when the device switches between power sources.

BMATR1	BMATR0	DELTA CAPACITANCE (C_{BAT} TO C_{VDD})
0	0	0pF
0	1	-0.5pF (≈ +2ppm)
1	0	+0.5pF (≈ -2ppm)
1	1	+1pF (≈ -4ppm)

DIGITAL TRIMMING REGISTER (DTR <2:0>)

The digital trimming bits DTR0, DTR1, and DTR2 adjust the average number of counts per second and average the ppm error to achieve better accuracy.

- DTR2 is a sign bit. DTR2 = “0” means frequency compensation is >0. DTR2 = “1” means frequency compensation is <0.
- DTR1 and DTR0 are both scale bits. DTR1 gives 40ppm adjustment and DTR0 gives 20ppm adjustment.

A range from -60ppm to +60ppm can be represented by using these three bits (see Table 5).

TABLE 5. DIGITAL TRIMMING REGISTERS

DTR REGISTER			ESTIMATED FREQUENCY PPM
DTR2	DTR1	DTR0	
0	0	0	0 (default)
0	0	1	+20
0	1	0	+40
0	1	1	+60
1	0	0	0
1	0	1	-20
1	1	0	-40
1	1	1	-60

Alarm Registers

Addresses [0Ch to 11h]

The alarm register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = “1”). These enable bits specify which alarm registers (seconds, minutes, etc) are used to make the comparison. Note that there is no alarm byte for year.

The alarm function works as a comparison between the alarm registers and the RTC registers. As the RTC advances, the alarm will be triggered once a match occurs between the alarm registers and the RTC registers. Any one alarm register, multiple registers, or all registers can be enabled for a match.

There are two alarm operation modes: Single Event and periodic Interrupt Mode:

- **Single Event Mode** is enabled by setting the ALME bit to “1”, the IM bit to “0”, and disabling the frequency output. This mode permits a one-time match between the alarm registers and the RTC registers. Once this match occurs, the ALM bit is set to “1” and the $\overline{IRQ}$ output will be pulled low and will remain low until the ALM bit is reset. This can be done manually or by using the auto-reset feature.
- **Interrupt Mode** is enabled by setting the ALME bit to “1”, the IM bit to “1”, and disabling the frequency output. The $\overline{IRQ}$ output will now be pulsed each time an alarm occurs. This means that once the interrupt mode alarm is set, it will continue to alarm for each occurring match of the alarm and present time. This mode is convenient for hourly or daily hardware interrupts in microcontroller applications such as security cameras or utility meter reading.

To clear an alarm, the ALM bit in the status register must be set to “0” with a write. Note that if the ARST bit is set to 1 (address 07h, bit 7), the ALM bit will automatically be cleared when the status register is read.

Below are examples of both Single Event and periodic Interrupt Mode alarms.

Example 1 – Alarm set with single interrupt (IM="0")

A single alarm will occur on January 1 at 11:30am.

A. Set Alarm registers as follows:

ALARM REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
SCA	0	0	0	0	0	0	0	0	00h	Seconds disabled
MNA	1	0	1	1	0	0	0	0	B0h	Minutes set to 30, enabled
HRA	1	0	0	1	0	0	0	1	91h	Hours set to 11, enabled
DTA	1	0	0	0	0	0	0	1	81h	Date set to 1, enabled
MOA	1	0	0	0	0	0	0	1	81h	Month set to 1, enabled
DWA	0	0	0	0	0	0	0	0	00h	Day of week disabled

B. Also the ALME bit must be set as follows:

CONTROL REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
INT	0	1	x	x	0	0	0	0	x0h	Enable Alarm

xx indicate other control bits

After these registers are set, an alarm will be generated when the RTC advances to exactly 11:30am on January 1 (after seconds changes from 59 to 00) by setting the ALM bit in the status register to "1" and also bringing the $\overline{IRQ}$ output low.

Example 2 – Pulsed interrupt once per minute (IM="1")

Interrupts at one minute intervals when the seconds register is at 30 seconds.

A. Set Alarm registers as follows:

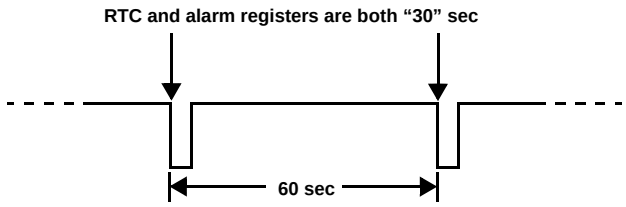
ALARM REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
SCA	1	0	1	1	0	0	0	0	B0h	Seconds set to 30, enabled
MNA	0	0	0	0	0	0	0	0	00h	Minutes disabled
HRA	0	0	0	0	0	0	0	0	00h	Hours disabled
DTA	0	0	0	0	0	0	0	0	00h	Date disabled
MOA	0	0	0	0	0	0	0	0	00h	Month disabled
DWA	0	0	0	0	0	0	0	0	00h	Day of week disabled

B. Set the Interrupt register as follows:

CONTROL REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
INT	1	1	x	x	0	0	0	0	x0h	Enable Alarm and Int Mode

xx indicate other control bits

Once the registers are set, the following waveform will be seen at IRQ-:



Note that the status register ALM bit will be set each time the alarm is triggered, but does not need to be read or cleared.

User Registers

Addresses [12h to 13h]

These registers are 2 bytes of battery-backed user memory storage.

I^2C Serial Interface

The ISL1208 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL1208 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 12). On power up of the ISL1208, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL1208 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 12). A START condition is ignored during the power-up sequence.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 12). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the

receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 13).

The ISL1208 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL1208 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

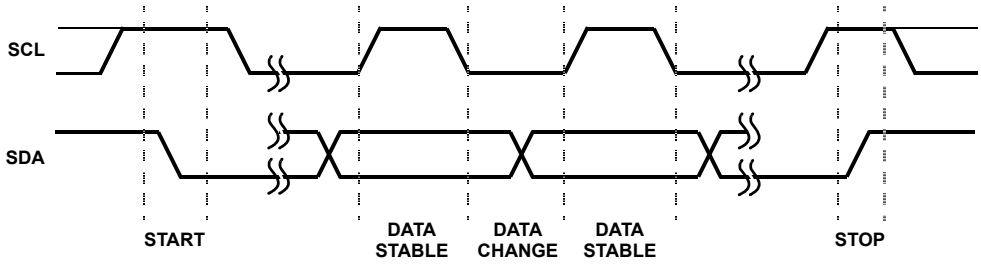


FIGURE 12. VALID DATA CHANGES, START, AND STOP CONDITIONS

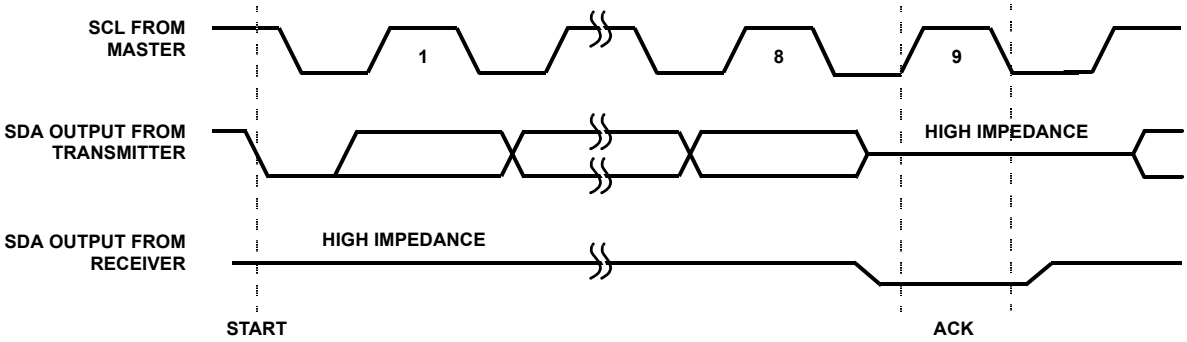


FIGURE 13. ACKNOWLEDGE RESPONSE FROM RECEIVER

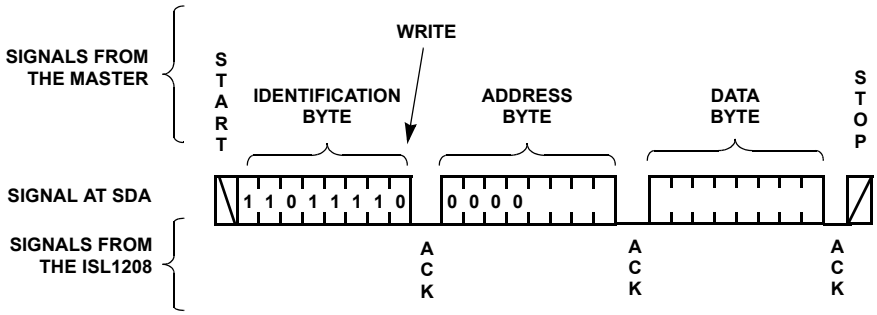


FIGURE 14. BYTE WRITE SEQUENCE

Device Addressing

Following a start condition, the master must output a Slave Address Byte. The 7 MSBs are the device identifier. These bits are “1101111”. Slave bits “1101” access the register. Slave bits “111” specify the device select bits.

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a “1”, then a read operation is selected. A “0” selects a write operation (Refer to Figure 15).

After loading the entire Slave Address Byte from the SDA bus, the ISL1208 compares the device identifier and device select bits with “1101111”. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power up the internal address counter is set to address 0h, so a current address read of the CCR array starts at address 0h. When required, as part of a random read, the master must supply the 1 Word Address Bytes as shown in Figure 16.

In a random read operation, the slave byte in the “dummy write” portion must match the slave byte in the “read” section. For a random read of the Clock/Control Registers, the slave byte must be “1101111x” in both places.

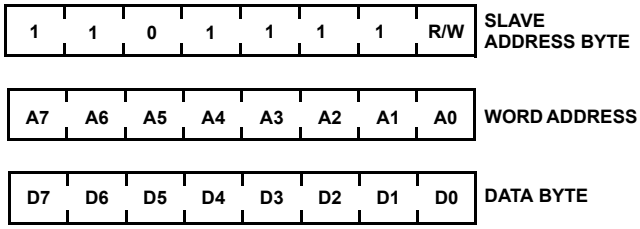


FIGURE 15. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL1208 responds with an ACK. At this time, the I^2C interface enters a standby state.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (See Figure 16). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL1208 responds with an ACK. Then the ISL1208 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (See Figure 16).

The Data Bytes are from the memory location indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 13h the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.

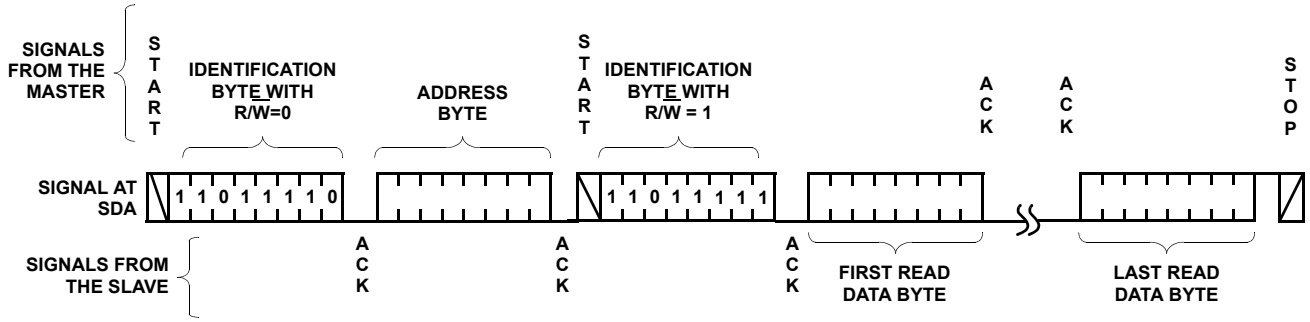


FIGURE 16. READ SEQUENCE

Application Section

Oscillator Crystal Requirements

The ISL1208 uses a standard 32.768kHz crystal. Either through hole or surface mount crystals can be used. Table 6 lists some recommended surface mount crystals and the parameters of each. This list is not exhaustive and other surface mount devices can be used with the ISL1208 if their specifications are very similar to the devices listed. The crystal should have a required parallel load capacitance of 12.5pF and an equivalent series resistance of less than 50k. The crystal's temperature range specification should match the application. Many crystals are rated for -10°C to +60°C (especially through hole and tuning fork types), so an appropriate crystal should be selected if extended temperature range is required.

TABLE 6. SUGGESTED SURFACE MOUNT CRYSTALS

MANUFACTURER	PART NUMBER
Citizen	CM200S
Epson	MC-405, MC-406
Raltron	RSM-200S
SaRonix	32S12
Ecliptek	ECPSM29T-32.768K
ECS	ECX-306
Fox	FSM-327

Crystal Oscillator Frequency Adjustment

The ISL1208 device contains circuitry for adjusting the frequency of the crystal oscillator. This circuitry can be used to trim oscillator initial accuracy as well as adjust the frequency to compensate for temperature changes.

The Analog Trimming Register (ATR) is used to adjust the load capacitance seen by the crystal. There are six bits of ATR control, with linear capacitance increments available for adjustment. Since the ATR adjustment is essentially "pulling" the frequency of the oscillator, the resulting frequency changes will not be linear with incremental capacitance changes. The equations which govern pulling show that lower capacitor values of ATR adjustment will provide larger increments. Also, the higher values of ATR adjustment will produce smaller incremental frequency changes. These values typically vary from 6-10 ppm/bit at the low end to <1ppm/bit at the highest capacitance settings. The range afforded by the ATR adjustment with a typical surface mount crystal is typically -34 to +80ppm around the ATR=0 default setting because of this property. The user should note this when using the ATR for calibration. The temperature drift of the capacitance used in the ATR control is extremely low, so this feature can be used for temperature compensation with good accuracy.

In addition to the analog compensation afforded by the adjustable load capacitance, a digital compensation feature is available for the ISL1208. There are 3 bits known as the Digital Trimming Register (DTR). The range provided is ±60ppm in increments of 20ppm. DTR operates by adding or skipping pulses in the clock counter. It is very useful for coarse adjustments of frequency drift over temperature or extending the adjustment range available with the ATR register.

Initial accuracy is best adjusted by enabling the frequency output (using the INT register, address 08h), and monitoring the ~IRQ/F_{OUT} pin with a calibrated frequency counter. The frequency used is unimportant, although 1Hz is the easiest to monitor. The gating time should be set long enough to ensure accuracy to at least 1ppm. The ATR should be set to the center position, or 100000Bh, to begin with. Once the initial measurement is made, then the ATR register can be changed to adjust the frequency. Note that increasing the ATR register for increased capacitance will lower the frequency, and vice-versa. If the initial measurement shows the frequency is far off, it will be necessary to use the DTR register to do a coarse adjustment. Note that most all crystals will have tight enough initial accuracy at room temperature so that a small ATR register adjustment should be all that is needed.

Temperature Compensation

The ATR and DTR controls can be combined to provide crystal drift temperature compensation. The typical 32.768kHz crystal has a drift characteristic that is similar to that shown in Figure 17. There is a turnover temperature (T_0) where the drift is very near zero. The shape is parabolic as it varies with the square of the difference between the actual temperature and the turnover temperature.

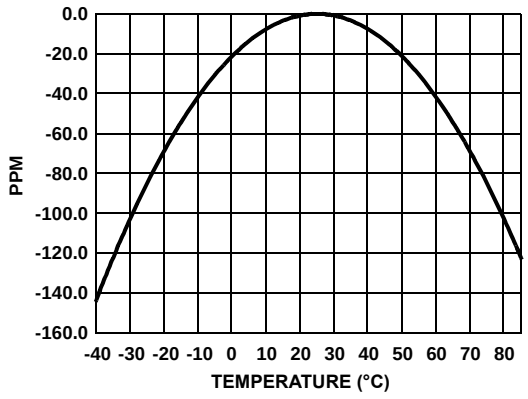


FIGURE 17. RTC CRYSTAL TEMPERATURE DRIFT

If full industrial temperature compensation is desired in an ISL1208 circuit, then both the DTR and ATR registers will need to be utilized (total correction range = -94 to +140ppm).

A system to implement temperature compensation would consist of the ISL1208, a temperature sensor, and a microcontroller. These devices may already be in the system so the function will just be a matter of implementing software and performing some calculations. Fairly accurate temperature compensation can be implemented just by using the crystal manufacturer's specifications for the turnover temperature T_0 and the drift coefficient (β). The formula for calculating the oscillator adjustment necessary is:

Adjustment (ppm) = $(T - T_0)^2 * \beta$

Once the temperature curve for a crystal is established, then the designer should decide at what discrete temperatures the compensation will change. Since drift is higher at extreme temperatures, the compensation may not be needed until the temperature is greater than 20°C from T_0.

A sample curve of the ATR setting vs. Frequency Adjustment for the ISL1208 and a typical RTC crystal is given in Figure 18. This curve may vary with different crystals, so it is good practice to evaluate a given crystal in an ISL1208 circuit before establishing the adjustment values.

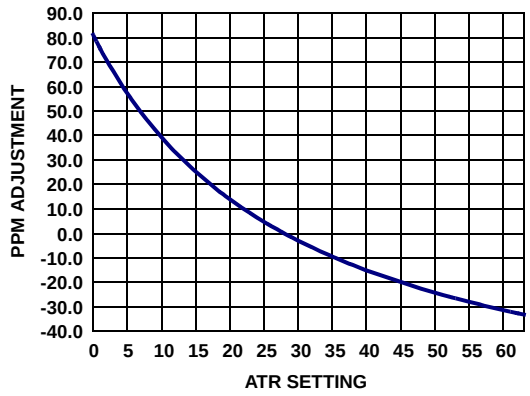


FIGURE 18. ATR SETTING vs OSCILLATOR FREQUENCY ADJUSTMENT

This curve is then used to figure what ATR and DTR settings are used for compensation. The results would be placed in a lookup table for the microcontroller to access.

Layout Considerations

The crystal input at X1 has a very high impedance, and oscillator circuits operating at low frequencies such as 32.768kHz are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and insure accurate clocking.

Figure 19 shows a suggested layout for the ISL1208 device using a surface mount crystal. Two main precautions should be followed:

Do not run the serial bus lines or any high speed logic lines in the vicinity of the crystal. These logic level lines can induce noise in the oscillator circuit to cause misclocking.

Add a ground trace around the crystal with one end terminated at the chip ground. This will provide termination for emitted noise in the vicinity of the RTC device.

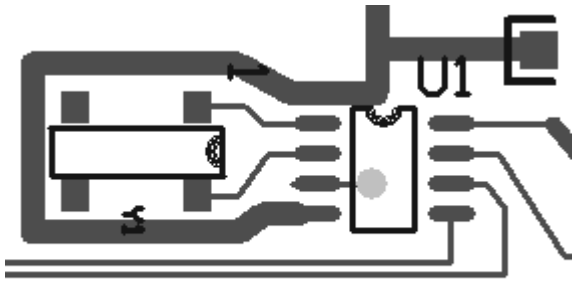


FIGURE 19. SUGGESTED LAYOUT FOR ISL1208 AND CRYSTAL

In addition, it is a good idea to avoid a ground plane under the X1 and X2 pins and the crystal, as this will affect the load capacitance and therefore the oscillator accuracy of the circuit. If the ~IRQ/F_{OUT} pin is used as a clock, it should be routed away from the RTC device as well. The traces for the V_{BAT} and V_{CC} pins can be treated as a ground, and should be routed around the crystal.

Super Capacitor Backup

The ISL1208 device provides a V_{BAT} pin which is used for a battery backup input. A Super Capacitor can be used as an alternative to a battery in cases where shorter backup times are required. Since the battery backup supply current required by the ISL1208 is extremely low, it is possible to get months of backup operation using a Super Capacitor. Typical capacitor values are a few µF to 1 Farad or more depending on the application.

If backup is only needed for a few minutes, then a small inexpensive electrolytic capacitor can be used. For extended periods, a low leakage, high capacity Super Capacitor is the best choice. These devices are available from such vendors as Panasonic and Murata. The main specifications include working voltage and leakage current. If the application is for charging the capacitor from a +5V ±5% supply with a signal diode, then the voltage on the capacitor can vary from ~4.5V to slightly over 5.0V. A capacitor with a rated WV of 5.0V may have a reduced lifetime if the supply voltage is slightly high. The leakage current should be as small as possible. For example, a Super Capacitor should be specified with leakage of well below 1µA. A standard electrolytic capacitor with DC leakage current in the microamps will have a severely shortened backup time.

Below are some examples with equations to assist with calculating backup times and required capacitance for the ISL1208 device. The backup supply current plays a major

part in these equations, and a typical value was chosen for example purposes. For a robust design, a margin of 30% should be included to cover supply current and capacitance tolerances over the results of the calculations. Even more margin should be included if periods of very warm temperature operation are expected.

Example 1. Calculating backup time given voltages and capacitor value

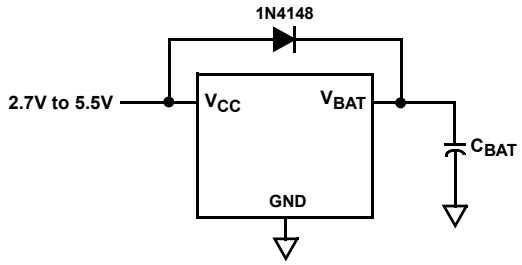


FIGURE 20. SUPERCAPACITOR CHARGING CIRCUIT

In Figure 20, use C_{BAT} = 0.47F and V_{CC} = 5.0V. With V_{CC} = 5.0V, the voltage at V_{BAT} will approach 4.7V as the diode turns off completely. The ISL1208 is specified to operate down to V_{BAT} = 1.8V. The capacitance charge/discharge equation is used to estimate the total backup time:

$$I = C_{BAT} * dV/dT \quad \text{(EQ. 1)}$$

Rearranging gives

$$dT = C_{BAT} * dV/I_{TOT} \text{ to solve for backup time.} \quad \text{(EQ. 2)}$$

C_{BAT} is the backup capacitance and dV is the change in voltage from fully charged to loss of operation. Note that I_{TOT} is the total of the supply current of the ISL1208 (I_{BAT}) plus the leakage current of the capacitor and the diode, I_{LKG}. In these calculations, I_{LKG} is assumed to be extremely small and will be ignored. If an application requires extended operation at temperatures over 50°C, these leakages will increase and hence reduce backup time.

Note that I_{BAT} changes with V_{BAT} almost linearly (see Typical Performance Curves). This allows us to make an approximation of I_{BAT}, using a value midway between the two endpoints. The typical linear equation for I_{BAT} vs V_{BAT} is:

$$I_{BAT} = 1.031E\text{-}7*(V_{BAT}) + 1.036E\text{-}7 \text{ Amps} \quad \text{(EQ. 3)}$$

Using this equation to solve for the average current given 2 voltage points gives:

$$I_{BATAVG} = 5.155E\text{-}8*(V_{BAT2} + V_{BAT1}) + 1.036E\text{-}7 \text{ Amps} \quad \text{(EQ. 4)}$$

Combining with Equation 2 gives the equation for backup time:

$$T_{BACKUP} = C_{BAT} * (V_{BAT2} - V_{BAT1}) / (I_{BATAVG} + I_{LKG}) \text{ seconds} \quad \text{(EQ. 5)}$$

where

C_{BAT} = 0.47F

V_{BAT2} = 4.7V

V_{BAT1} = 1.8V

I_{LKG} = 0 (assumed minimal)

Solving equation 4 for this example, I_{BATAVG} = 4.387E-7 A

T_{BACKUP} = 0.47 * (2.9) / 4.38E-7 = 3.107E6 sec

Since there are 86,400 seconds in a day, this corresponds to 35.96 days. If the 30% tolerance is included for capacitor and supply current tolerances, then worst case backup time would be:

C_{BAT} = 0.70 * 35.96 = 25.2 days

Example 2. Calculating a capacitor value for a given backup time

Referring to Figure 20 again, the capacitor value needs to be calculated to give 2 months (60 days) of backup time, given V_{CC} = 5.0V. As in Example 1, the V_{BAT} voltage will vary from 4.7V down to 1.8V. We will need to rearrange Equation 2 to solve for capacitance:

$$C_{BAT} = dT*I/dV \quad \text{(EQ. 6)}$$

Using the terms described above, this equation becomes:

$$C_{BAT} = T_{BACKUP} * (I_{BATAVG} + I_{LKG})/(V_{BAT2} - V_{BAT1}) \quad \text{(EQ. 7)}$$

where

T_{BACKUP} = 60 days * 86,400 sec/day = 5.18 E6 sec

I_{BATAVG} = 4.387 E-7 A (same as Example 1)

I_{LKG} = 0 (assumed)

V_{BAT2} = 4.7V

V_{BAT1} = 1.8V

Solving gives

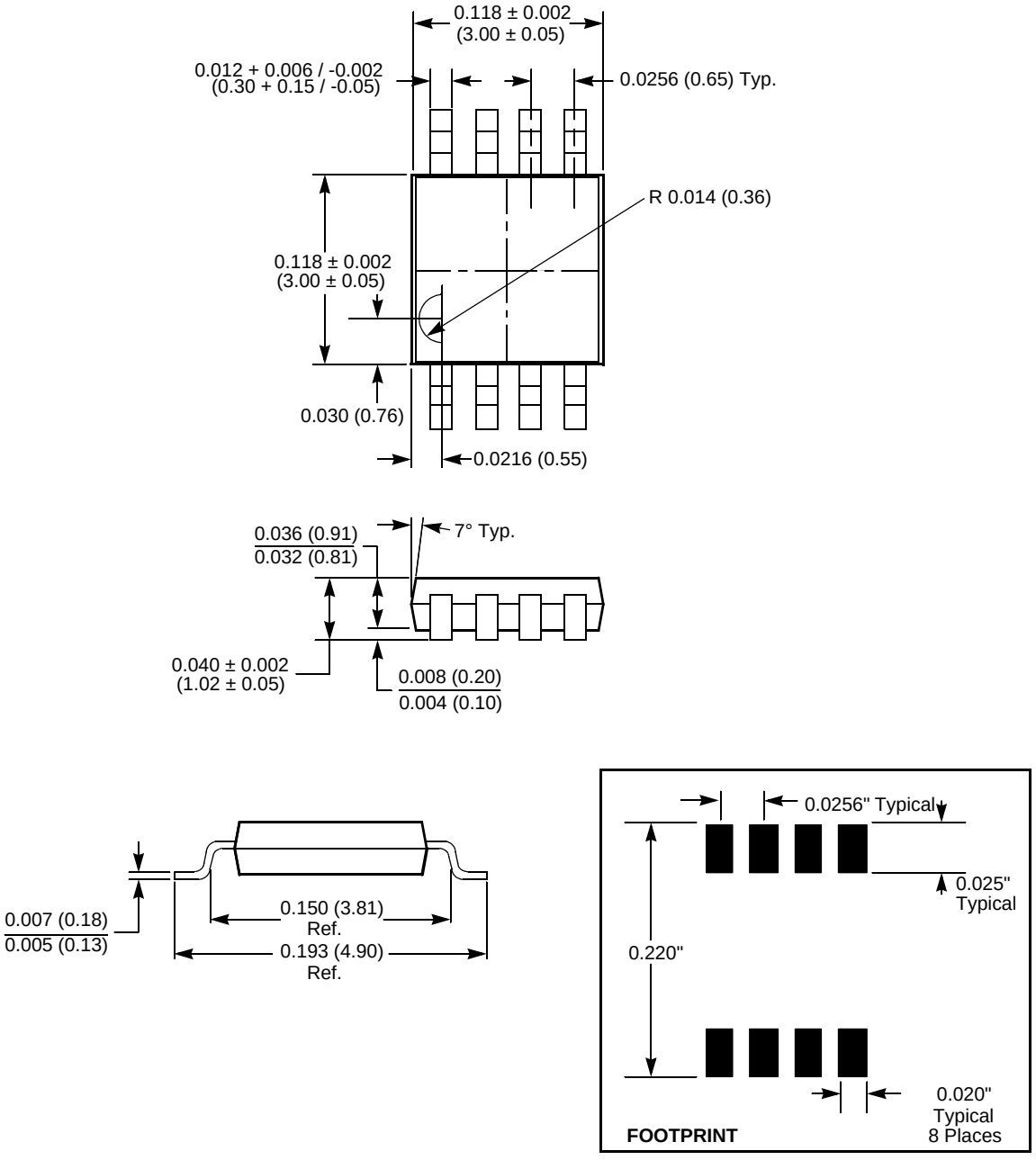
C_{BAT} = 5.18 E6 * (4.387 E-7)/(2.9) = 0.784F

If the 30% tolerance is included for tolerances, then worst case cap value would be

C_{BAT} = 1.3 *.784 = 1.02F

Packaging Information

8-Lead Miniature Small Outline Gull Wing Package Type M

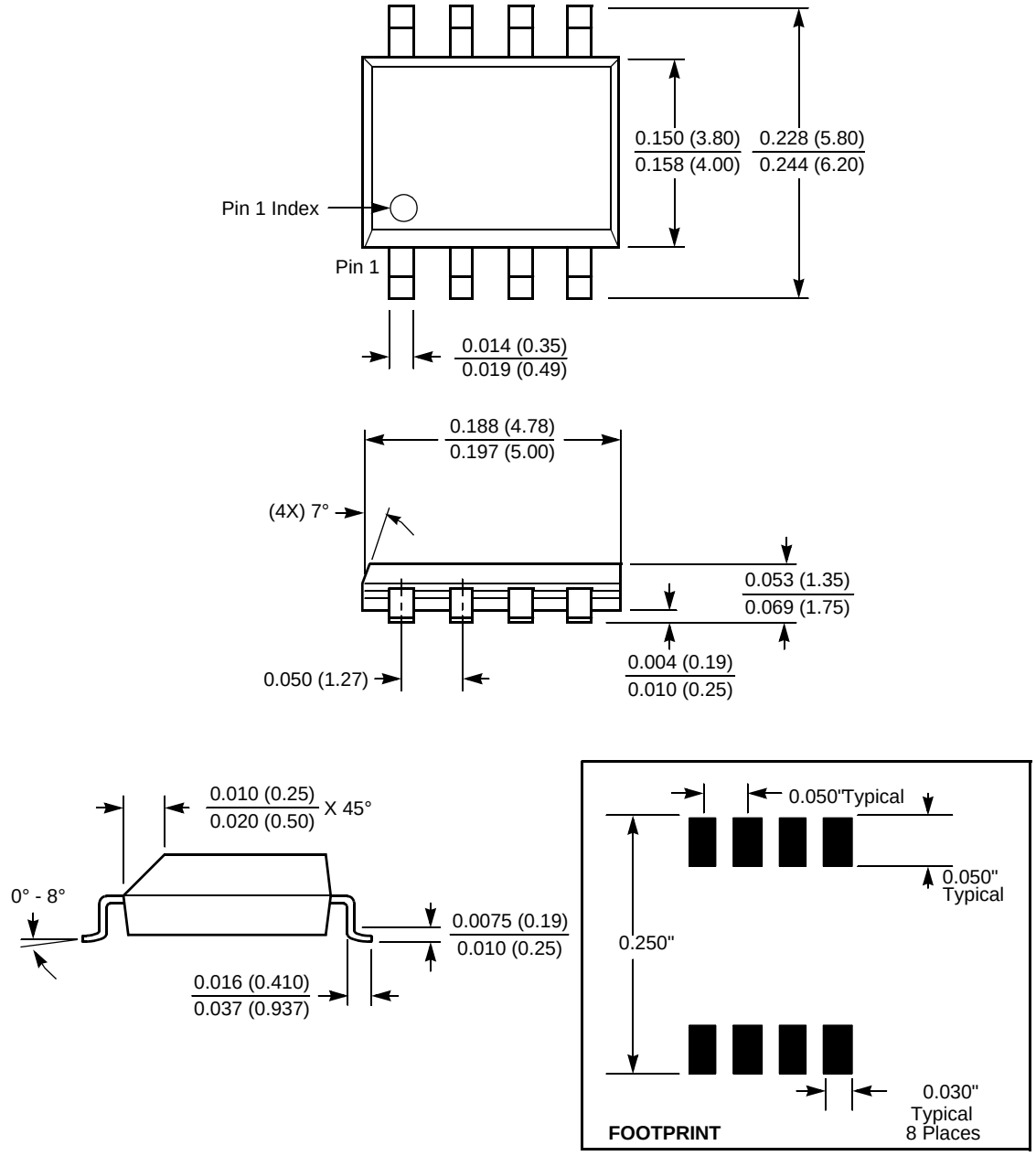


NOTE:

1. All dimensions in inches and (millimeters).

Packaging information

8-Lead Plastic, SOIC, Package Code S8



NOTE: All dimensions in inches (in parentheses in millimeters).

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

128Mb F-die SDRAM Specification

54 TSOP-II with Pb-Free

(RoHS compliant)

Revision 1.2

August 2004

Revision History

Revision 1.0 (January, 2004)

- First release.

Revision 1.1 (May, 2004)

• Added Note 5. sentense of tRDL parameter.

Revision 1.2 (August, 2004)

• Corrected typo.

8M x 4Bit x 4 Banks / 4M x 8Bit x 4 Banks / 2M x 16Bit x 4 Banks SDRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM (x4,x8) & L(U)DQM (x16) for masking
- Auto & self refresh
- 64ms refresh period (4K Cycle)
- **54 TSOP(II) Pb-free Package**
- **RoHS compliant**

GENERAL DESCRIPTION

The K4S280432F / K4S280832F / K4S281632F is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 8,388,608 words by 4 bits / 4 x 4,194,304 words by 8 bits / 4 x 2,097,152 words by 16 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

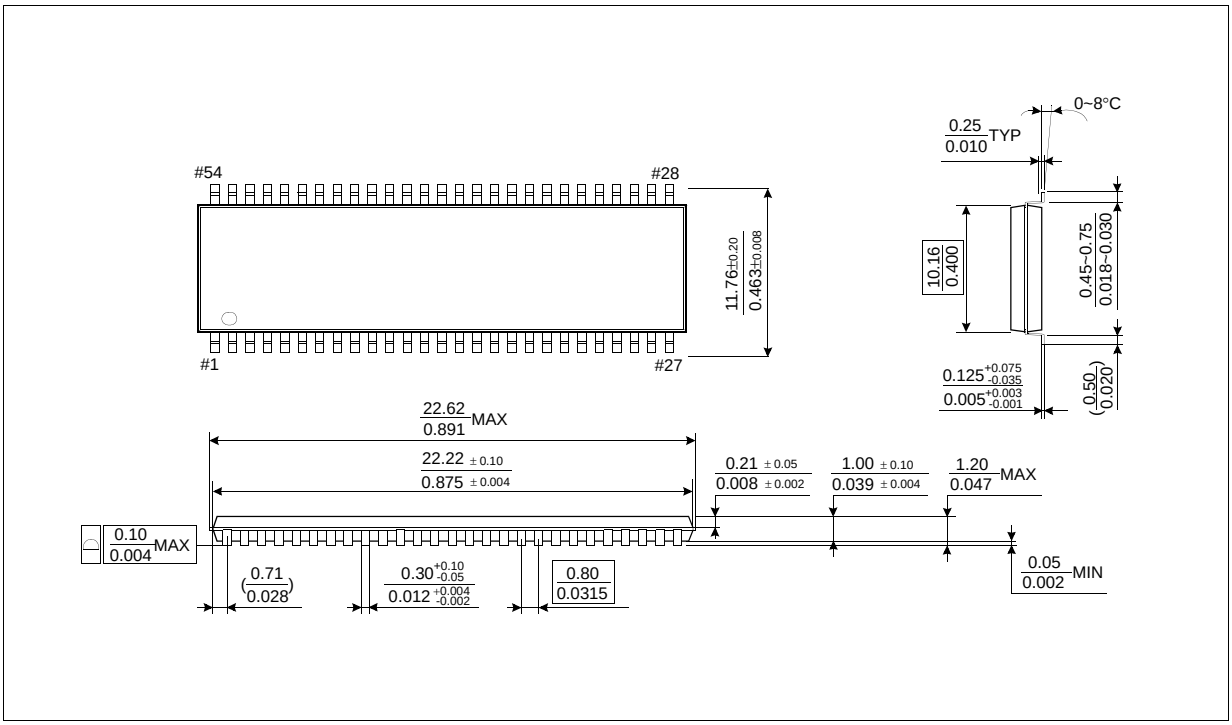
Ordering Information

Part No.	Orgainization	Max Freq.	Interface	Package
K4S280432F-UC(L)75	32M x 4	133MHz	LVTTL	54pin TSOP(II)
K4S280832F-UC(L)75	16M x 8	133MHz	LVTTL	54pin TSOP(II)
K4S281632F-UC(L)60/75	8M x 16	166MHz	LVTTL	54pin TSOP(II)

Organization	Row Address	Column Address
32Mx4	A0~A11	A0-A9, A11
16Mx8	A0~A11	A0-A9
8Mx16	A0~A11	A0-A8

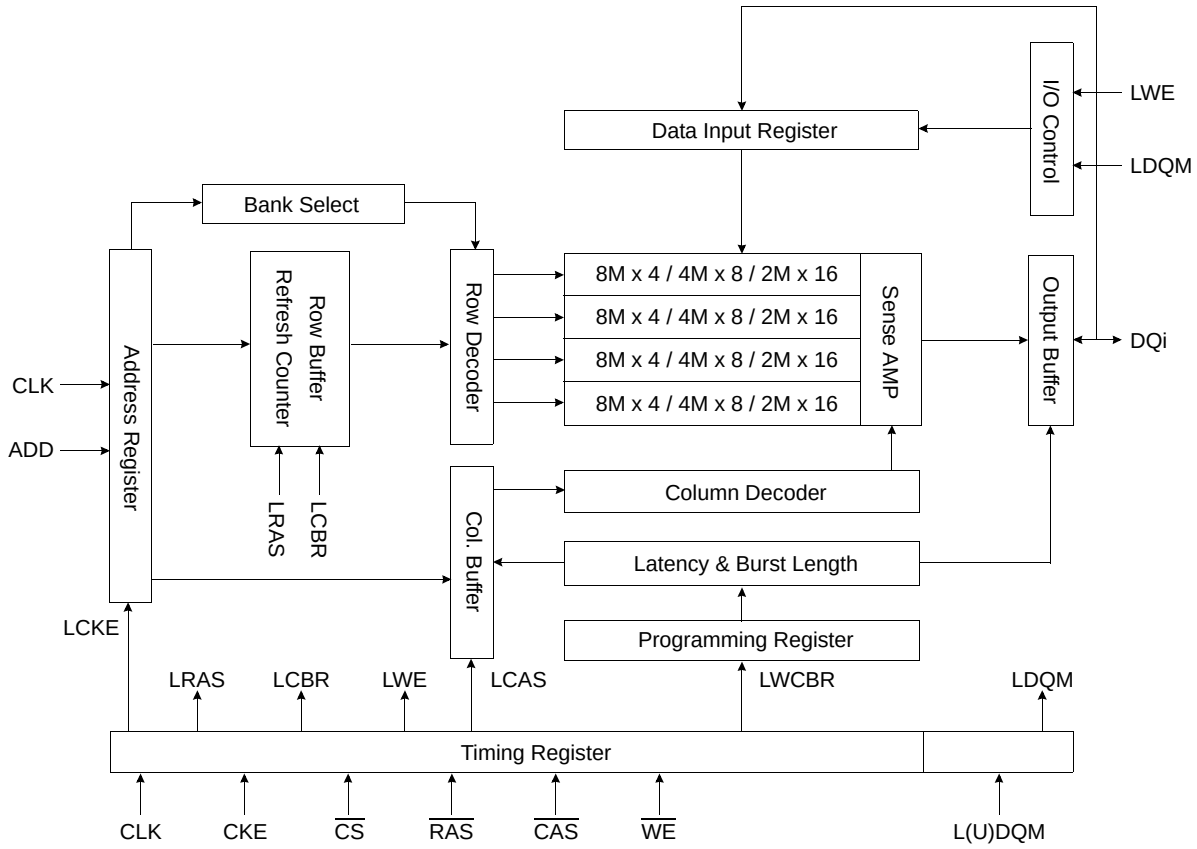
Row & Column address configuration

Package Physical Dimension



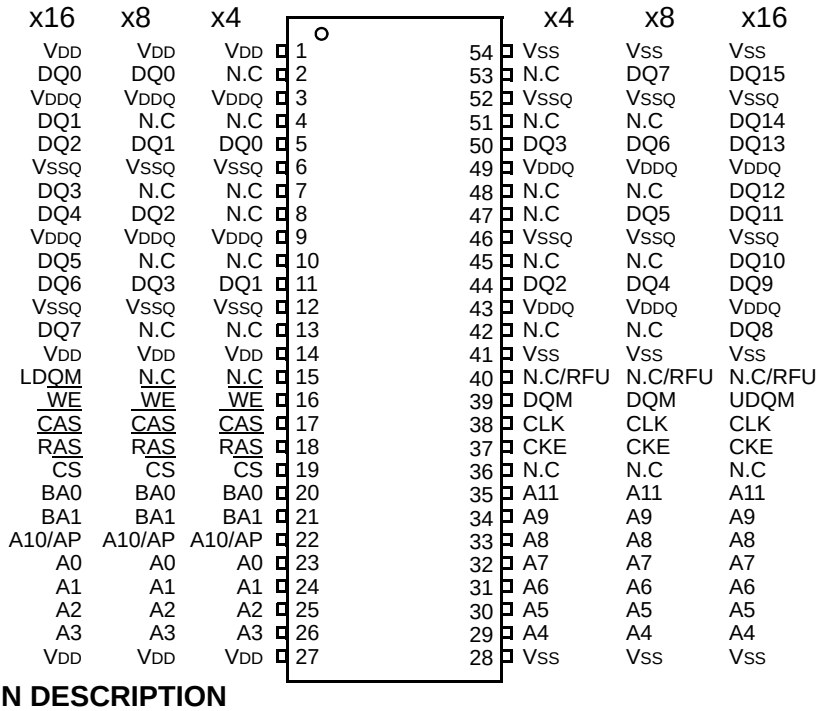
54Pin TSOP Package Dimension

FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)



54Pin TSOP
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{11}	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{11}, Column address : (x4 : CA_0 ~ CA_9,CA_{11}), (x8 : CA_0 ~ CA_9), (x16 : CA_0 ~ CA_8)
BA_0 ~ BA_1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
DQ_0 ~ N	*Data input/output*	Data inputs/outputs are multiplexed on the same pins. (x4 : DQ_0 ~ 3), (x8 : DQ_0 ~ 7), (x16 : DQ_0 ~ 15)
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No connection /reserved for future use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	2.5	3.5	pF	
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	2.5	3.8	pF	
Address	C_{ADD}	2.5	3.8	pF	
(x4 : DQ_0 ~ DQ_3), (x8 : DQ_0 ~ DQ_7), (x16 : DQ_0 ~ DQ_{15})	C_{OUT}	4.0	6.0	pF	

DC CHARACTERISTICS (x4, x8)

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Version -75	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		90	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		2	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		2		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		20	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		10		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		5	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		5		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		30	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		25	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst		110	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		200	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	2	mA	3
			L	800	uA	4

Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S2804(08)32F-UC
4. K4S2804(08)32F-UL
5. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

DC CHARACTERISTICS (x16)

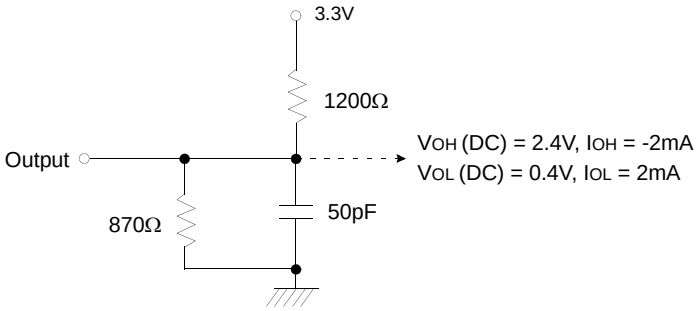
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Version		Unit	Note
				-60	-75		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		130	100	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		2		mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		2			
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		20		mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		10			
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		5		mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		5			
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		30		mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		25		mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst		150	140	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		220	200	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	2		mA	3
			L	800		uA	4

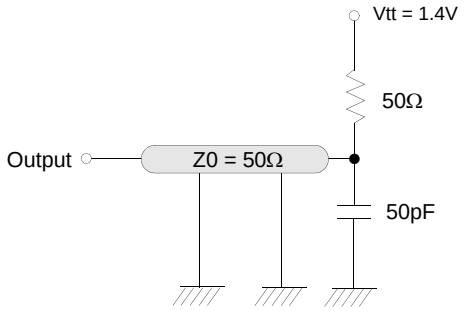
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S281632F-UC
4. K4S281632F-UL
5. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			- 60 (x16 only)	- 75		
Row active to row active delay		tRRD(min)	12	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	18	20	ns	1
Row precharge time		tRP(min)	18	20	ns	1
Row active time		tRAS(min)	42	45	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	60	65	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + tRP		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		-	1		

Notes :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. In 100MHz and below 100MHz operating conditions, tRDL=1CLK and tDAL=1CLK + 20ns is also supported. SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + tRP.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	- 60 (x16 only)		- 75		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	6	1000	7.5	1000	ns	1
	CAS latency=2		-		10			
CLK to valid output delay	CAS latency=3	tSAC		5		5.4	ns	1,2
	CAS latency=2			-		6		
Output data hold time	CAS latency=3	tOH	2.5		3		ns	2
	CAS latency=2		-		3			
CLK high pulse width		tCH	2.5		2.5		ns	3
CLK low pulse width		tCL	2.5		2.5		ns	3
Input setup time		tSS	1.5		1.5		ns	3
Input hold time		tSH	1		0.8		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5		5.4	ns	
	CAS latency=2			-		6		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

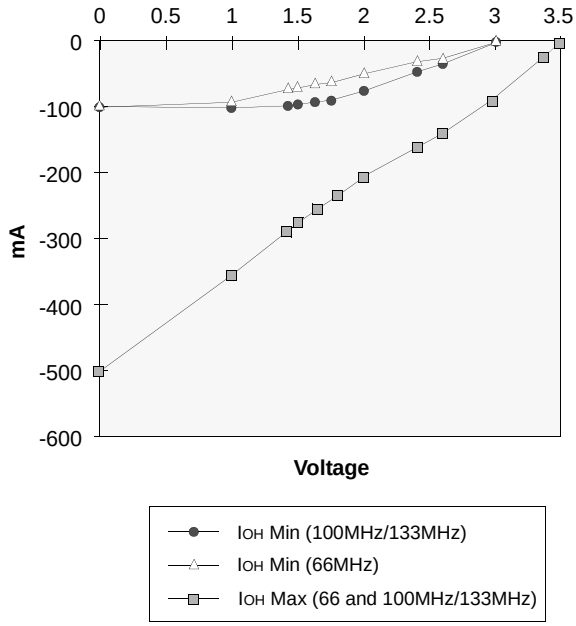
Notes : 1. Rise time specification based on 0pF + 50 Ω to VSS, use these values to design to.
2. Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.
3. Measured into 50pF only, use these values to characterize to.
4. All measurements done with respect to VSS.

IBIS SPECIFICATION

IOH Characteristics (Pull-up)

Voltage	100MHz 133MHz Min	100MHz 133MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0

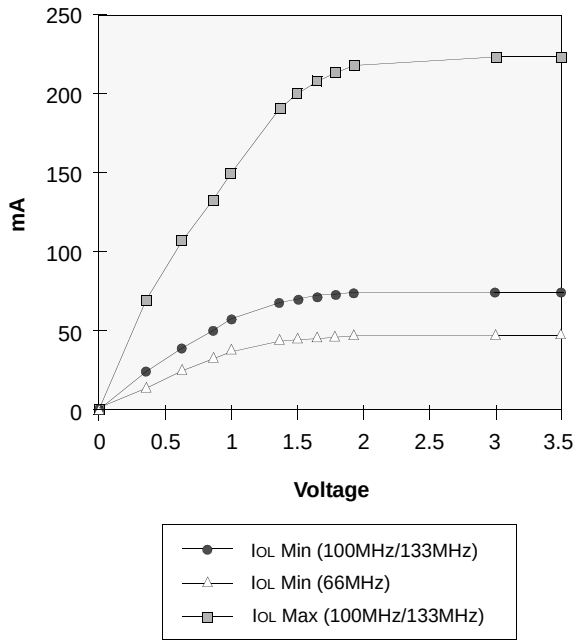
66MHz and 100MHz/133MHz Pull-up



IOL Characteristics (Pull-down)

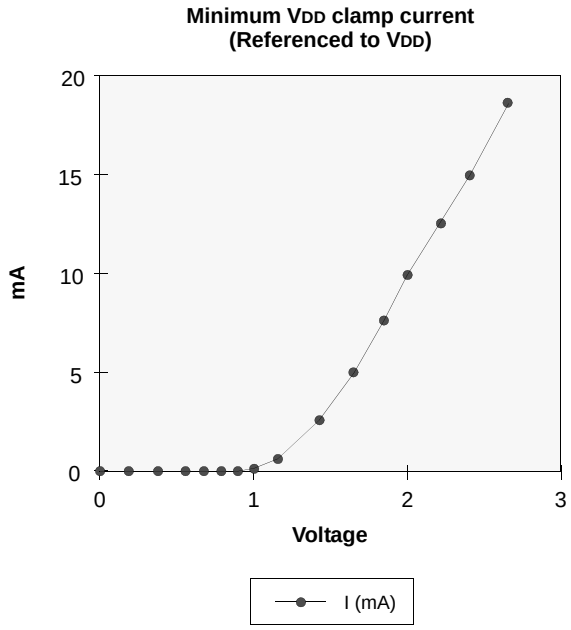
Voltage	100MHz 133MHz Min	100MHz 133MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

66MHz and 100MHz/133MHz Pull-down



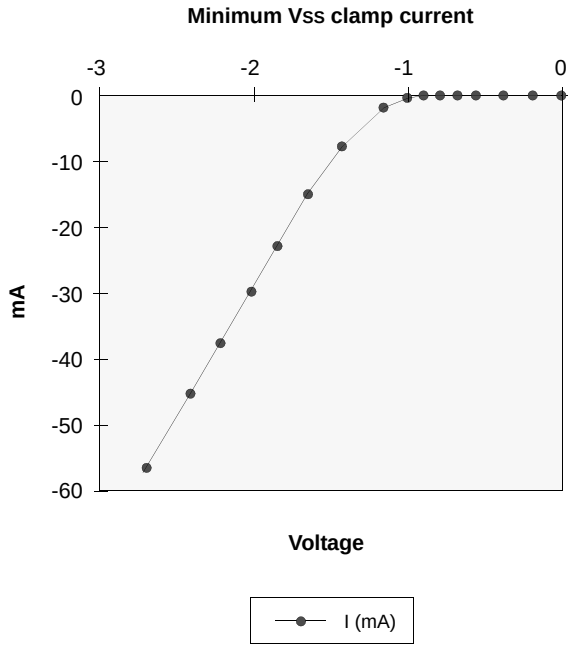
VDD Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

VDD (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31



Vss Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

Vss (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0



SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A0 ~ A9, A11,	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

Notes :
1. OP Code : Operand code
   A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
   If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

3-W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

FEATURES

- **Advanced DC Volume Control With 2-dB Steps From -40 dB to 20 dB**
  - **Fade Mode**
  - **Maximum Volume Setting for SE Mode**
  - **Adjustable SE Volume Control Referenced to BTL Volume Control**
- **3 W Into 3-Ω Speakers**
- **Stereo Input MUX**
- **Differential Inputs**

APPLICATIONS

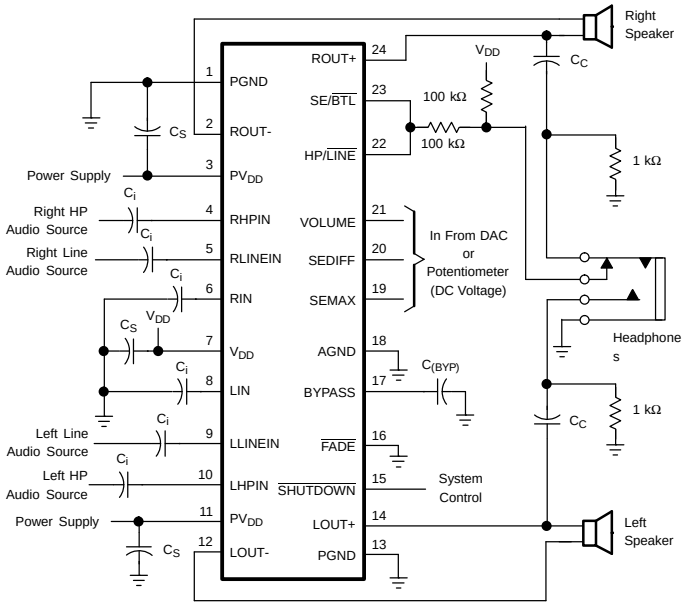
- **Notebook PC**
- **LCD Monitors**
- **Pocket PC**

DESCRIPTION

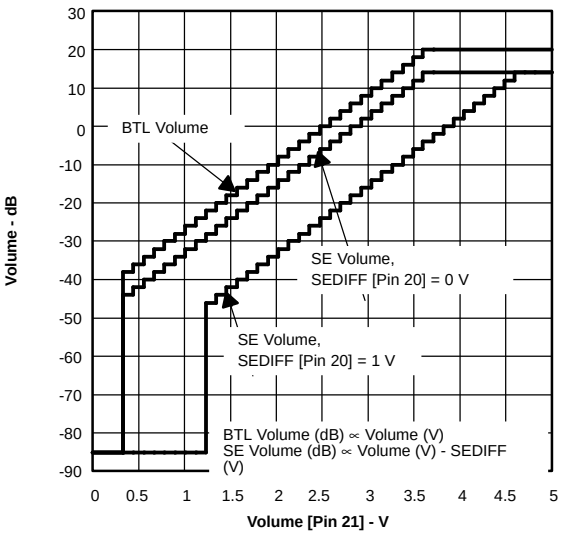
The TPA6011A4 is a stereo audio power amplifier that drives 3 W/channel of continuous RMS power into a 3-Ω load. Advanced dc volume control minimizes external components and allows BTL (speaker) volume control and SE (headphone) volume control. Notebook and pocket PCs benefit from the integrated feature set that minimizes external components without sacrificing functionality.

To simplify design, the speaker volume level is adjusted by applying a dc voltage to the VOLUME terminal. Likewise, the delta between speaker volume and headphone volume can be adjusted by applying a dc voltage to the SEDIFF terminal. To avoid an unexpected high volume level through the headphones, a third terminal, SEMAX, limits the headphone volume level when a dc voltage is applied. Finally, to ensure a smooth transition between active and shutdown modes, a fade mode ramps the volume up and down.

APPLICATION CIRCUIT



DC VOLUME CONTROL



AVAILABLE OPTIONS

T_A	PACKAGE
	24-PIN TSSOP (PWP)(1)
40°C to 85°C	TPA6011A4PWP

(1) The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA6011A4PWPR).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
V_{SS}	Supply voltage, V_{DD}, PV_{DD}	-0.3 V to 6 V
V_I	Input voltage	-0.3 V to V_{DD}+0.3 V
	Continuous total power dissipation	See Dissipation Rating Table
T_A	Operating free-air temperature range	-40°C to 85°C
T_J	Operating junction temperature range	-40°C to 150°C
T_{stg}	Storage temperature range	-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	2.7 mW	21.8 mW/°C	1.7 W	1.4 W

RECOMMENDED OPERATING CONDITIIONS

			MIN	MAX	UNIT
V_{SS}	Supply voltage, V_{DD}, PV_{DD}		4.0	5.5	V
V_{IH}	High-level input voltage	SE/$\overline{BTL}$, HP/$\overline{LINE}$, $\overline{FADE}$	$0.8 \times V_{DD}$		V
		$\overline{SHUTDOWN}$	2		V
V_{IL}	Low-level input voltage	SE/$\overline{BTL}$, HP/$\overline{LINE}$, $\overline{FADE}$		$0.6 \times V_{DD}$	V
		$\overline{SHUTDOWN}$		0.8	V
T_A	Operating free-air temperature		-40	85	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = PV_{DD} = 5.5 V (unless otherwise noted)

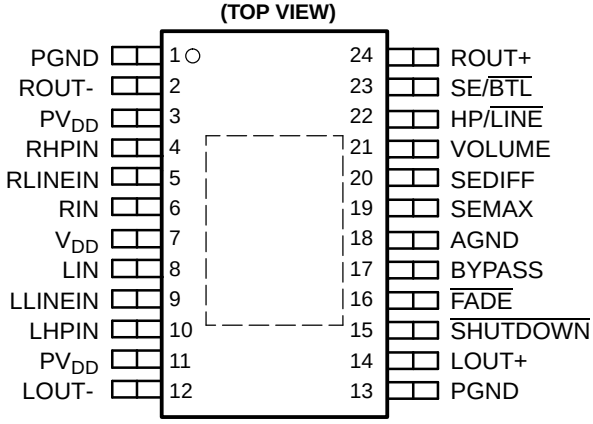
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)	V_{DD} = 5.5 V, Gain = 0 dB, SE/$\overline{BTL}$ = 0 V			30	mV
		V_{DD} = 5.5 V, Gain = 20 dB, SE/$\overline{BTL}$ = 0 V			50	mV
PSRR	Power supply rejection ratio	V_{DD} = PV_{DD} = 4.0 V to 5.5 V	-42	-70		dB
$\lvert I_{IH} \rvert$	High-level input current (SE/$\overline{BTL}$, $\overline{FADE}$, HP/$\overline{LINE}$, $\overline{SHUTDOWN}$, SEDIFF, SEMAX, VOLUME)	V_{DD} = PV_{DD} = 5.5 V, V_I = V_{DD} = PV_{DD}			1	µA
$\lvert I_{IL} \rvert$	Low-level input current (SE/$\overline{BTL}$, $\overline{FADE}$, HP/$\overline{LINE}$, $\overline{SHUTDOWN}$, SEDIFF, SEMAX, VOLUME)	V_{DD} = PV_{DD} = 5.5 V, V_I = 0 V			1	µA
I_{DD}	Supply current, no load	V_{DD} = PV_{DD} = 5.5 V, SE/$\overline{BTL}$ = 0 V, $\overline{SHUTDOWN}$ = 2 V	6.0	7.5	9.0	mA
		V_{DD} = PV_{DD} = 5.5 V, SE/$\overline{BTL}$ = 5.5 V, $\overline{SHUTDOWN}$ = 2 V	3.0	5	6	
I_{DD}	Supply current, max power into a 3-Ω load	V_{DD} = 5 V = PV_{DD}, SE/$\overline{BTL}$ = 0 V, $\overline{SHUTDOWN}$ = 2 V, R_L = 3Ω, P_O = 2 W, stereo		1.5		A_{RMS}
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0.0 V		1	20	µA

OPERATING CHARACTERISTICS

T_A = 25°C, V_{DD} = PV_{DD} = 5 V, R_L = 3 Ω, Gain = 6 dB (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%, f = 1 kHz			2		W
		THD = 10%, f = 1 kHz, V_{DD} = 5.5 V			3		
THD+N	Total harmonic distortion + noise	P_O = 1 W, R_L = 8 Ω , f = 20 Hz to 20 kHz			<0.4%		
V_{OH}	High-level output voltage	R_L = 8 Ω, Measured between output and V_{DD}				700	mV
V_{OL}	Low-level output voltage	R_L = 8 Ω, Measured between output and GND				400	mV
$V_{(Bypass)}$	Bypass voltage (Nominally V_{DD}/2)	Measured at pin 17, No load, V_{DD} = 5.5 V		2.65	2.75	2.85	V
B_{OM}	Maximum output power bandwidth	THD = 5%			>20		kHz
	Supply ripple rejection ratio	f = 1 kHz, Gain = 0 dB, $C_{(BYP)}$ = 0.47 µF	BTL		-63		dB
			SE		-57		dB
	Noise output voltage	f = 20 Hz to20 kHz, Gain = 0 dB, $C_{(BYP)}$ = 0.47 µF	BTL		36		$µV_{RMS}$
Z_I	Input impedance (see Figure 26)	VOLUME = 5.0 V			14		kΩ

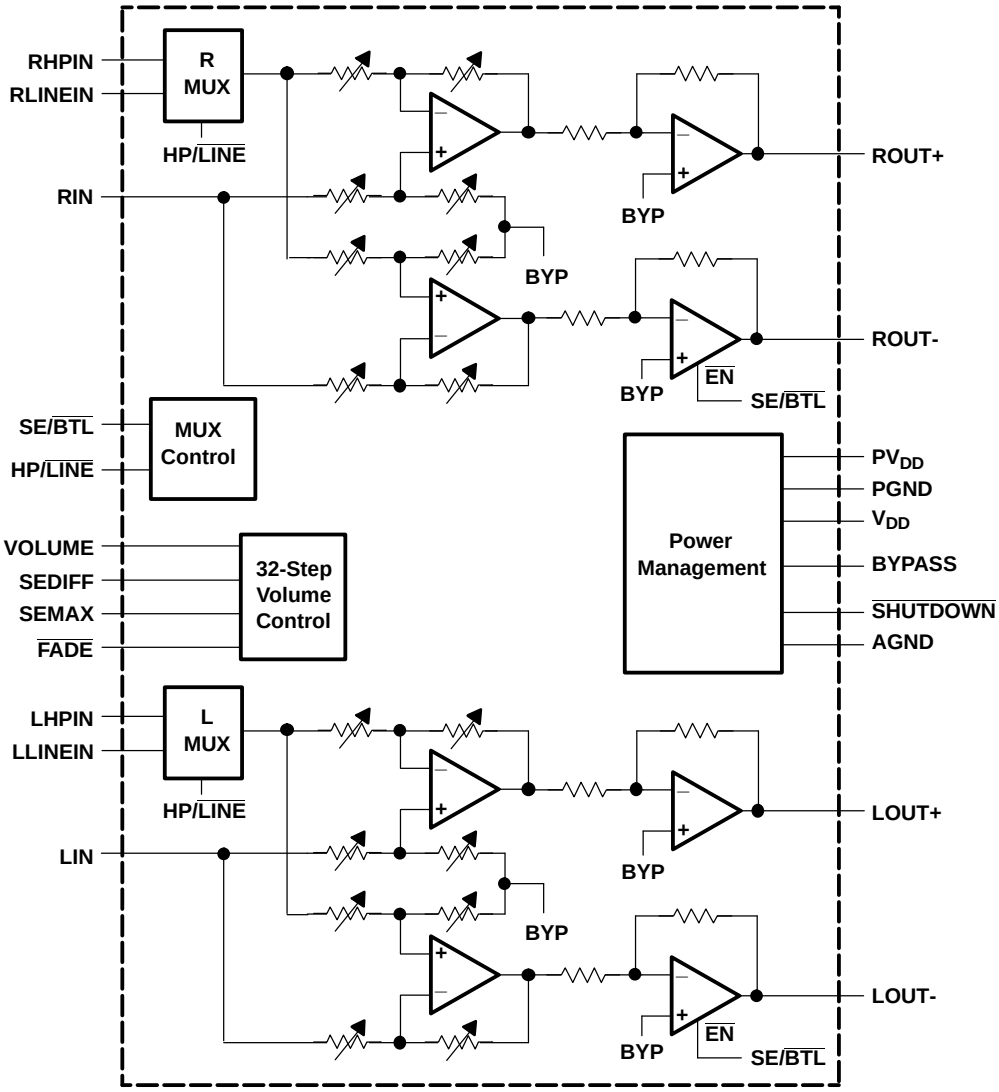
PWP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PGND	1, 13	-	Power ground
LOUT-	12	O	Left channel negative audio output
PV_{DD}	3, 11	-	Supply voltage terminal for power stage
LHPIN	10	I	Left channel headphone input, selected when HP/$\overline{\text{LINE}}$ is held high
LLINEIN	9	I	Left channel line input, selected when HP/$\overline{\text{LINE}}$ is held low
LIN	8	I	Common left channel input for fully differential input. AC ground for single-ended inputs.
V_{DD}	7	-	Supply voltage terminal
RIN	6	I	Common right channel input for fully differential input. AC ground for single-ended inputs.
RLINEIN	5	I	Right channel line input, selected when HP/$\overline{\text{LINE}}$ is held low
RHPIN	4	I	Right channel headphone input, selected when HP/$\overline{\text{LINE}}$ is held high
ROUT-	2	O	Right channel negative audio output
ROUT+	24	O	Right channel positive audio output
$\overline{\text{SHUTDOWN}}$	15	I	Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal
$\overline{\text{FADE}}$	16	I	Places the amplifier in fade mode if a logic low is placed on this terminal; normal operation if a logic high is placed on this terminal
BYPASS	17	I	Tap to voltage divider for internal midsupply bias generator used for analog reference
AGND	18	-	Analog power supply ground
SEMAX	19	I	Sets the maximum volume for single ended operation. DC voltage range is 0 to V_{DD}.
SEDIFF	20	I	Sets the difference between BTL volume and SE volume. DC voltage range is 0 to V_{DD}.
VOLUME	21	I	Terminal for dc volume control. DC voltage range is 0 to V_{DD}.
HP/$\overline{\text{LINE}}$	22	I	Input MUX control. When logic high, RHPIN and LHPIN inputs are selected. When logic low, RLINEIN and LLINEIN inputs are selected.
SE/$\overline{\text{BTL}}$	23	I	Output MUX control. When this terminal is high, SE outputs are selected. When this terminal is low, BTL outputs are selected.
LOUT+	14	O	Left channel positive audio output.

FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor wipers are adjusted with 32 step volume control.

Table 1. DC Volume Control (BTL Mode, V_{DD} = 5 V)(1)

VOLUME (PIN 21)		GAIN OF AMPLIFIER (Typ)
FROM (V)	TO (V)	
0.00	0.26	-85(2)
0.33	0.37	-40
0.44	0.48	-38
0.56	0.59	-36
0.67	0.70	-34
0.78	0.82	-32
0.89	0.93	-30
1.01	1.04	-28
1.12	1.16	-26
1.23	1.27	-24
1.35	1.38	-22
1.46	1.49	-20
1.57	1.60	-18
1.68	1.72	-16
1.79	1.83	-14
1.91	1.94	-12
2.02	2.06	-10
2.13	2.17	-8
2.25	2.28	-6(2)
2.36	2.39	-4
2.47	2.50	-2
2.58	2.61	0
2.70	2.73	2
2.81	2.83	4
2.92	2.95	6
3.04	3.06	8
3.15	3.17	10
3.26	3.29	12
3.38	3.40	14
3.49	3.51	16
3.60	3.63	18
3.71	5.00	20(2)

(1) For other values of V_{DD}, scale the voltage values in the table by a factor of V_{DD}/5.
(2) Tested in production. Remaining gain steps are specified by design.

Table 2. DC Volume Control (SE Mode, V_{DD} = 5 V)(1)

SE_VOLUME = VOLUME - SEDIFF or SEMAX		GAIN OF AMPLIFIER (Typ)
FROM (V)	TO (V)	
0.00	0.26	-85(2)
0.33	0.37	-46
0.44	0.48	-44
0.56	0.59	-42
0.67	0.70	-40
0.78	0.82	-38
0.89	0.93	-36
1.01	1.04	-34
1.12	1.16	-32
1.23	1.27	-30
1.35	1.38	-28
1.46	1.49	-26
1.57	1.60	-24
1.68	1.72	-22
1.79	1.83	-20
1.91	1.94	-18
2.02	2.06	-16
2.13	2.17	-14
2.25	2.28	-12
2.36	2.39	-10
2.47	2.50	-8
2.58	2.61	-6(2)
2.70	2.73	-4
2.81	2.83	-2
2.92	2.95	0(2)
3.04	3.06	2
3.15	3.17	4
3.26	3.29	6(2)
3.38	3.40	8
3.49	3.51	10
3.60	3.63	12
3.71	5.00	14

(1) For other values of V_{DD}, scale the voltage values in the table by a factor of $V_{DD}/5$.
(2) Tested in production. Remaining gain steps are specified by design.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise (BTL)	vs Frequency	1, 2 3
		vs Output power	6, 7, 8
THD+N	Total harmonic distortion plus noise (SE)	vs Frequency	4, 5
		vs Output power	9
		vs Output voltage	10
	Closed loop response		11, 12
I_{CC}	Supply current	vs Temperature	13
		vs Supply voltage	14, 15, 16
P_D	Power Dissipation	vs Output power	17, 18
P_O	Output power	vs Load resistance	19, 20
	Crosstalk	vs Frequency	21, 22
	HP/$\overline{\text{LINE}}$ attenuation	vs Frequency	23
PSRR	Power supply ripple rejection (BTL)	vs Frequency	24
PSRR	Power supply ripple rejection (SE)	vs Frequency	25
Z_I	Input impedance	vs BTL gain	26
V_n	Output noise voltage	vs Frequency	27

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
FREQUENCY

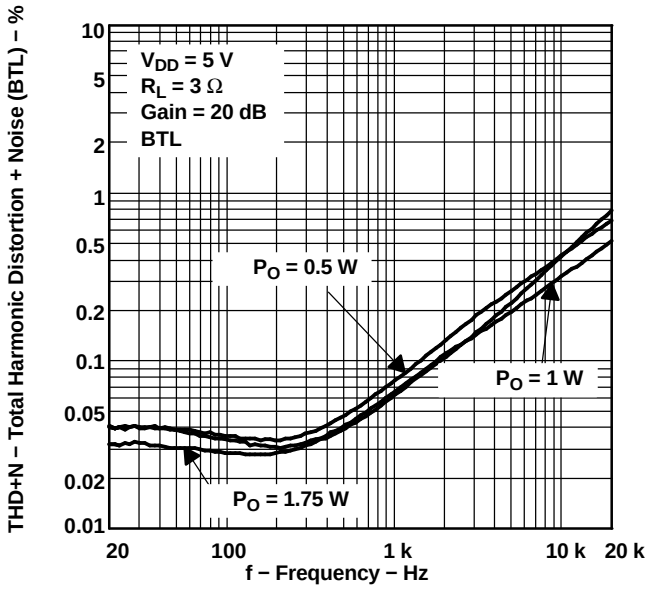


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
FREQUENCY

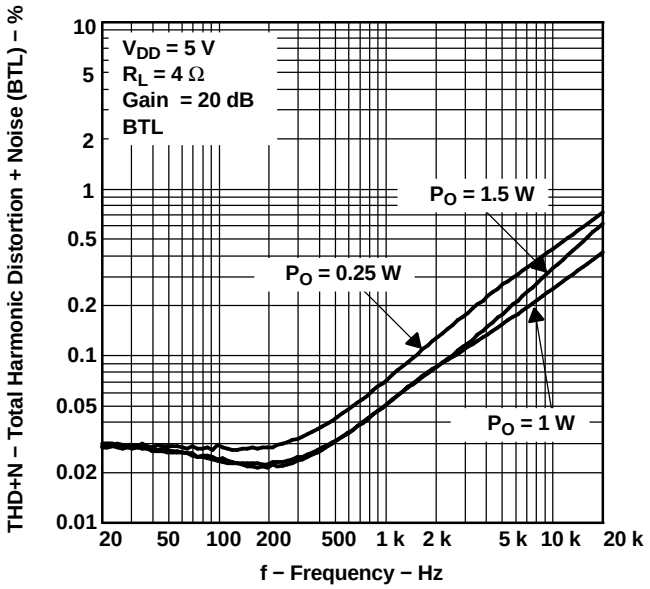


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
FREQUENCY

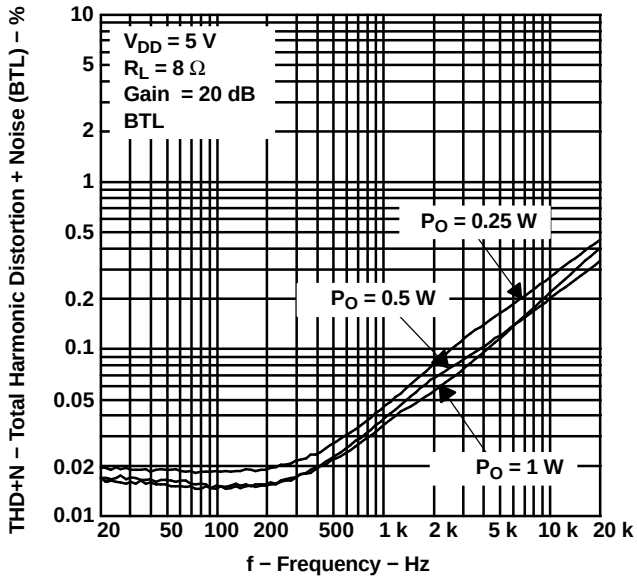


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE (SE)
vs
FREQUENCY

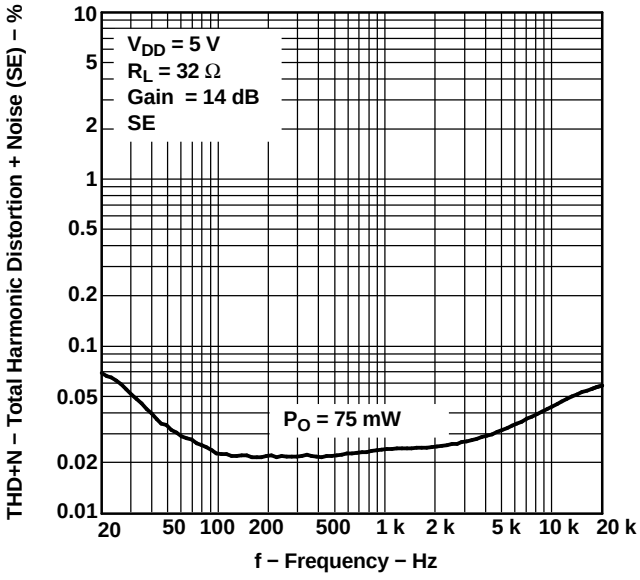


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE (SE)
vs
FREQUENCY

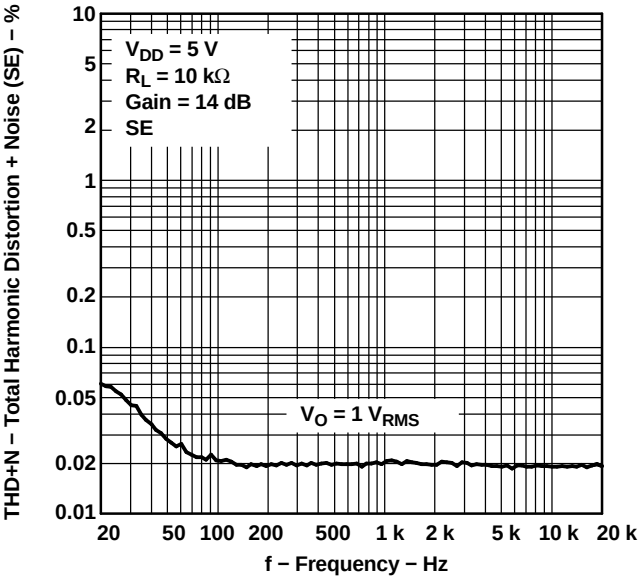


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
OUTPUT POWER

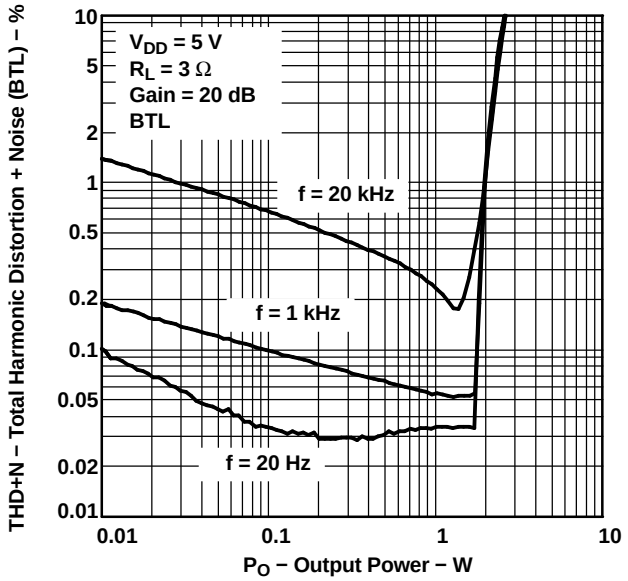


Figure 6.

TEXAS INSTRUMENTS
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TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
OUTPUT POWER

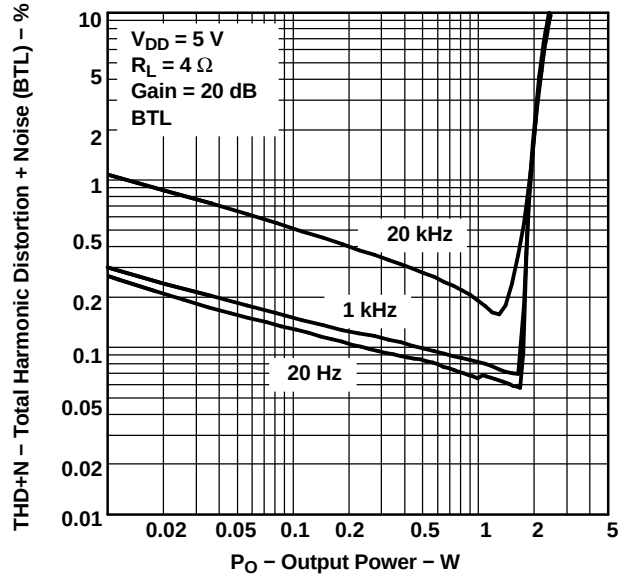


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
OUTPUT POWER

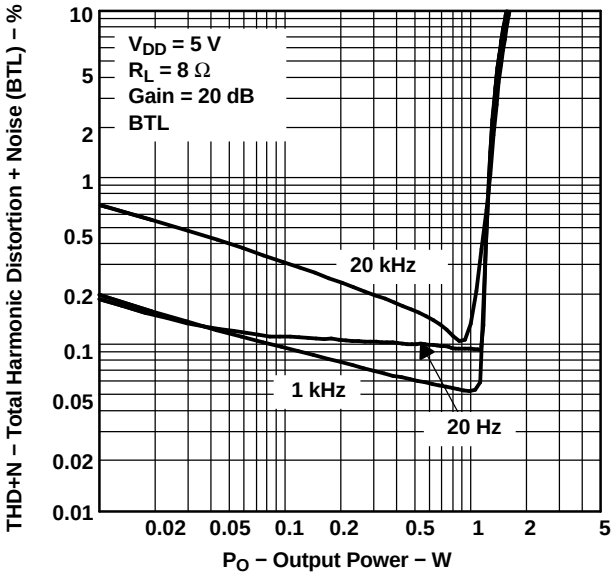


Figure 8.

TOTAL HARMONIC DISTORTION + NOISE (SE)
vs
OUTPUT POWER

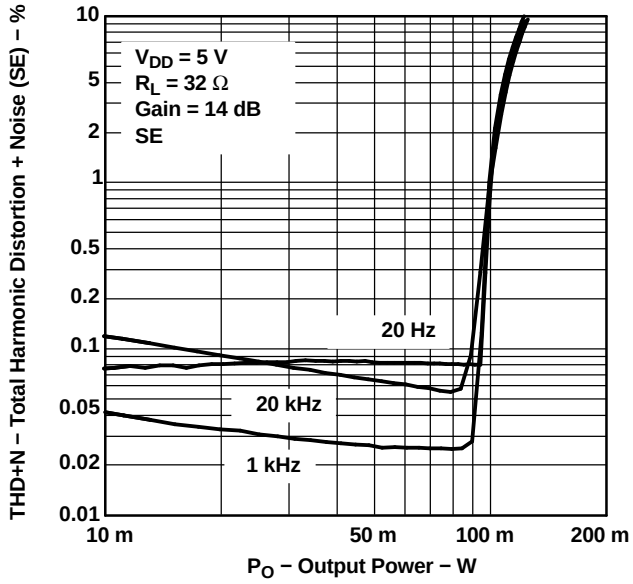


Figure 9.

TOTAL HARMONIC DISTORTION + NOISE (SE)
vs
OUTPUT VOLTAGE

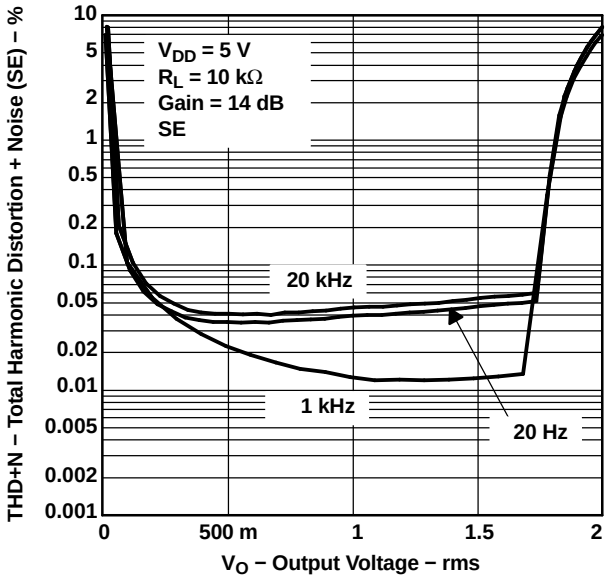


Figure 10.

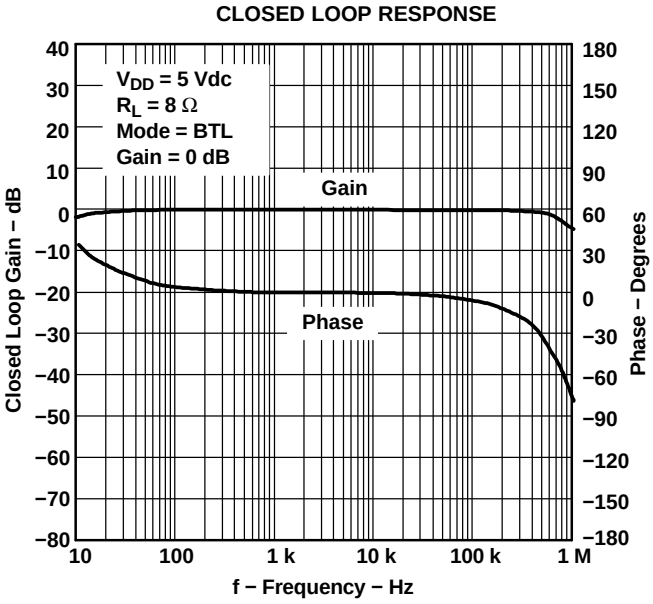
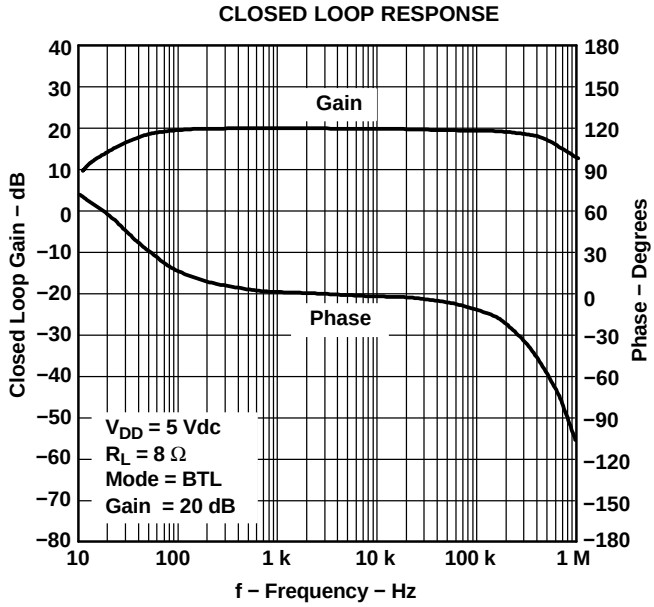


Figure 11.



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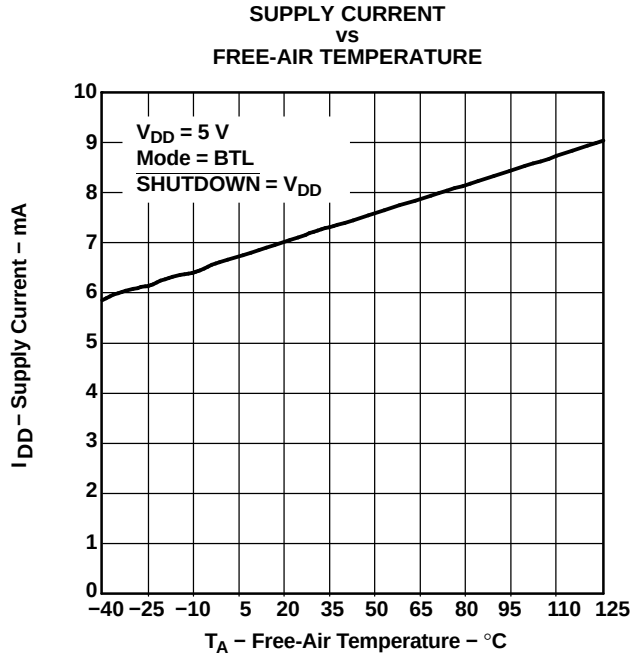


Figure 13.

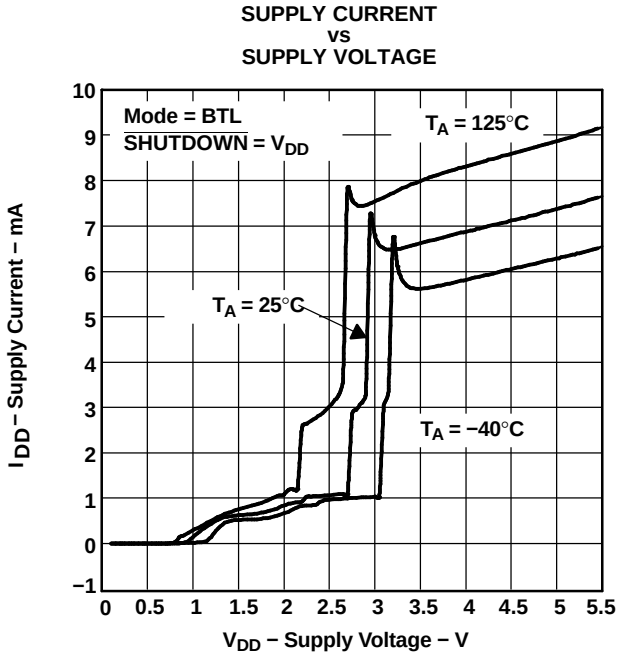


Figure 14.

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

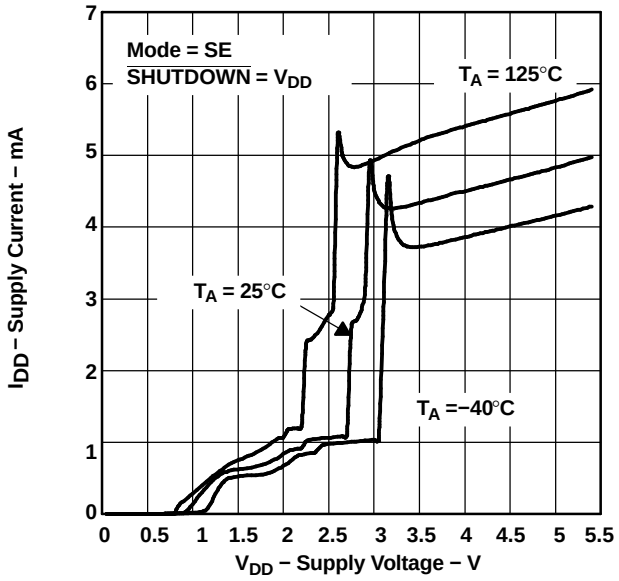


Figure 15.

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

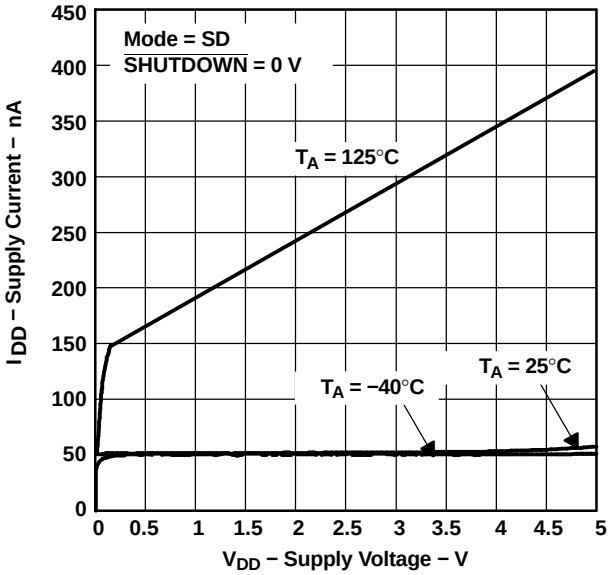


Figure 16.

POWER DISSIPATION (PER CHANNEL)
vs
OUTPUT POWER

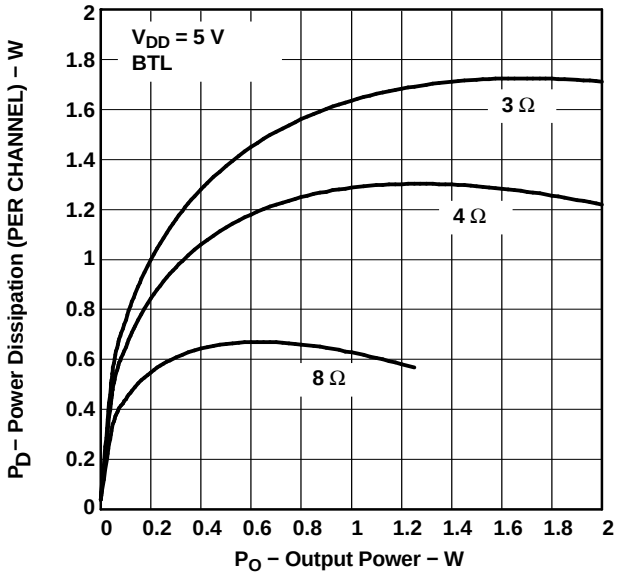


Figure 17.

POWER DISSIPATION (PER CHANNEL)
vs
OUTPUT POWER

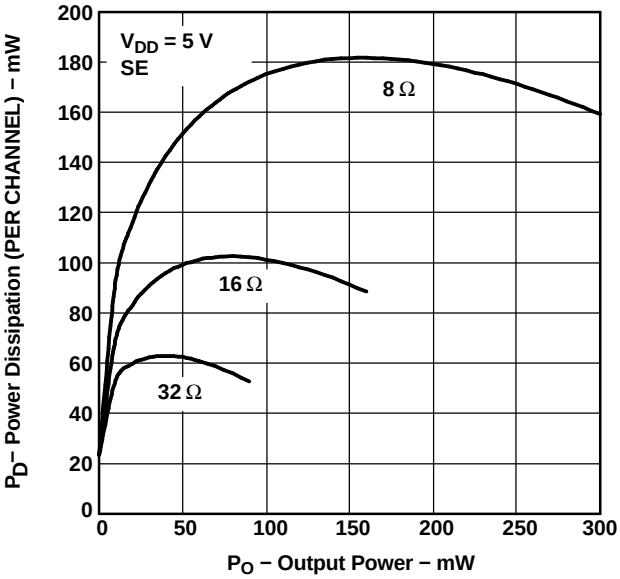
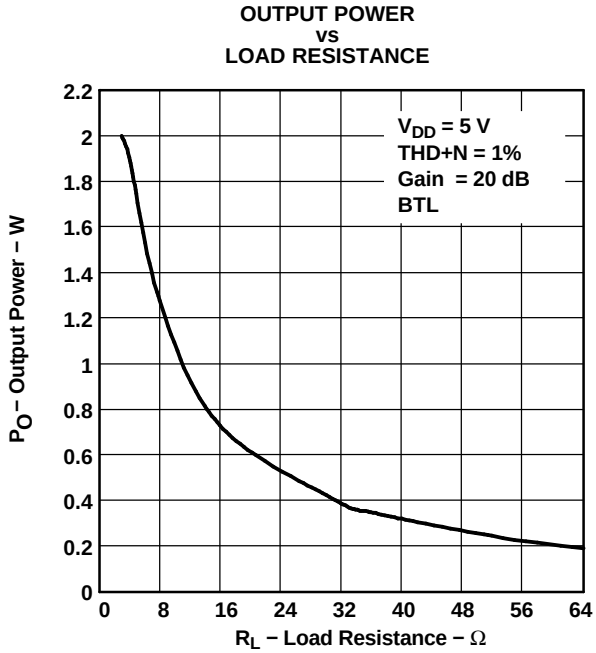


Figure 18.



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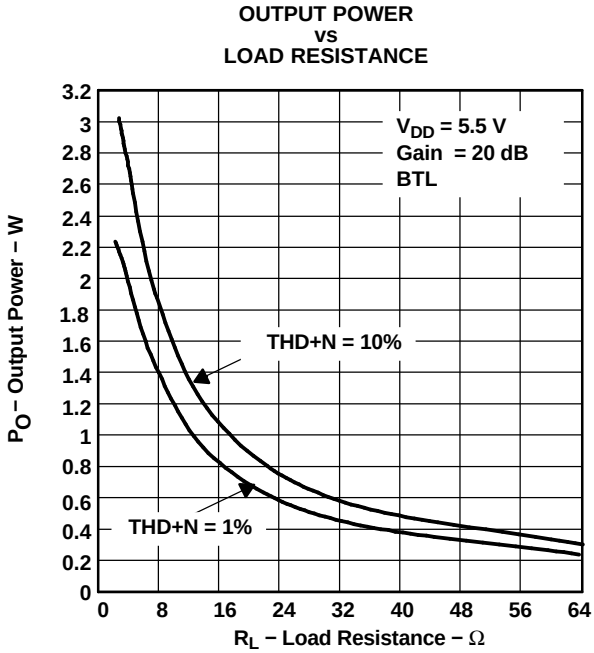


Figure 20.

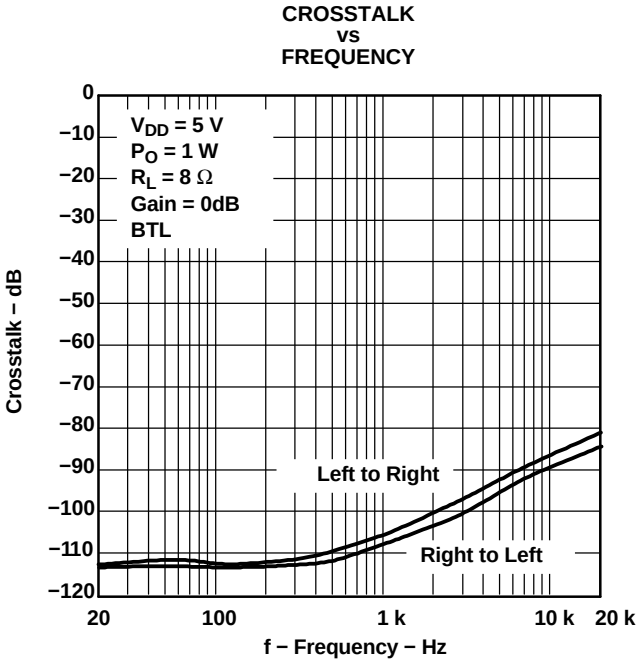


Figure 21.

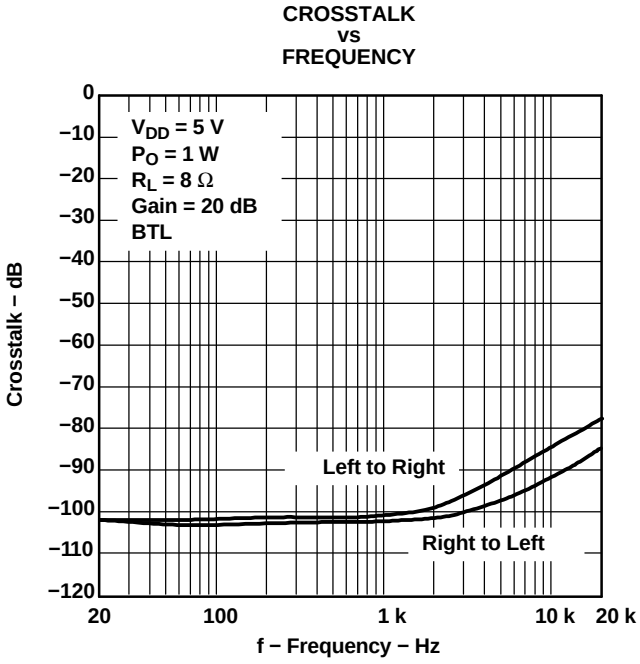


Figure 22.

HP/LINE ATTENUATION vs FREQUENCY

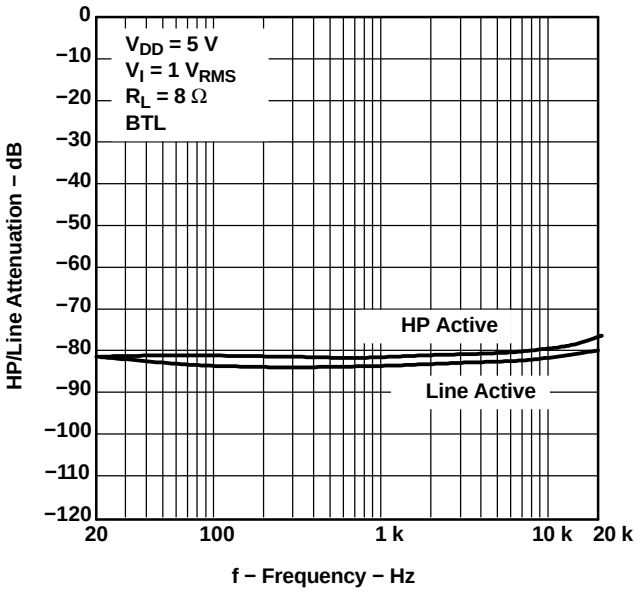


Figure 23.

POWER SUPPLY REJECTION RATIO (BTL) vs FREQUENCY

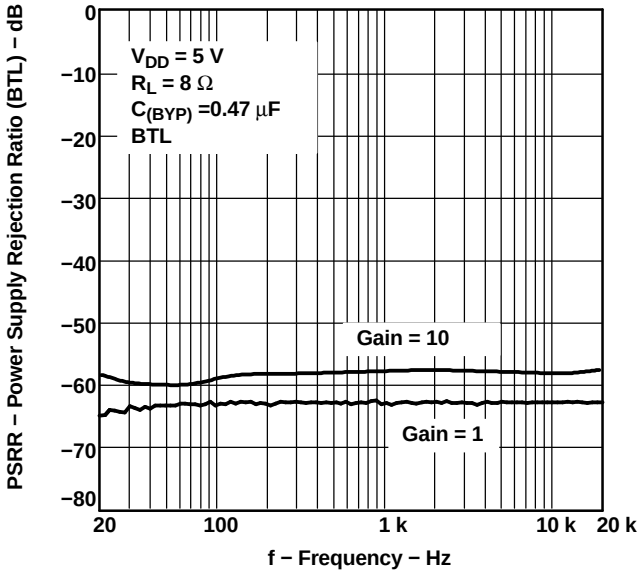


Figure 24.

POWER SUPPLY REJECTION RATIO (SE) vs FREQUENCY

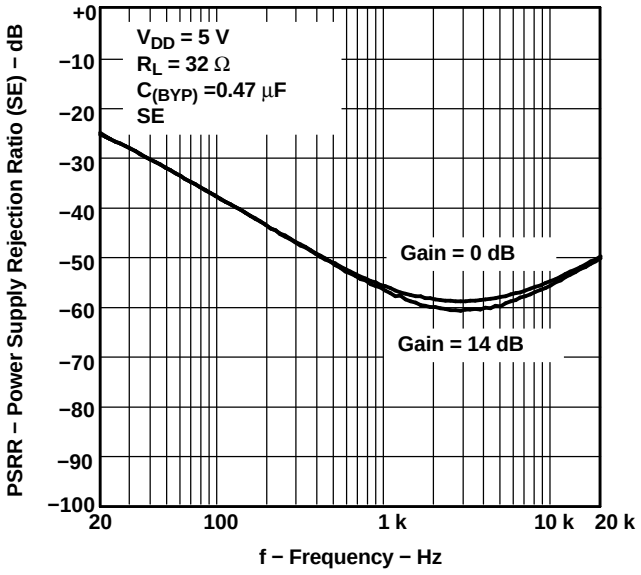


Figure 25.

INPUT IMPEDANCE vs BTL GAIN

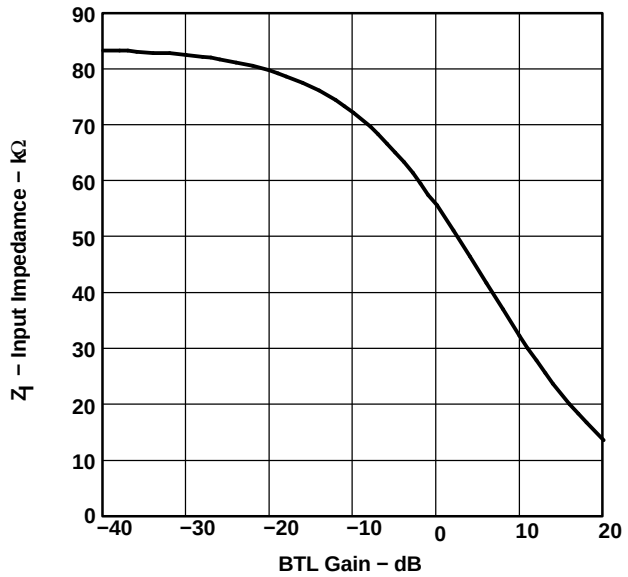


Figure 26.

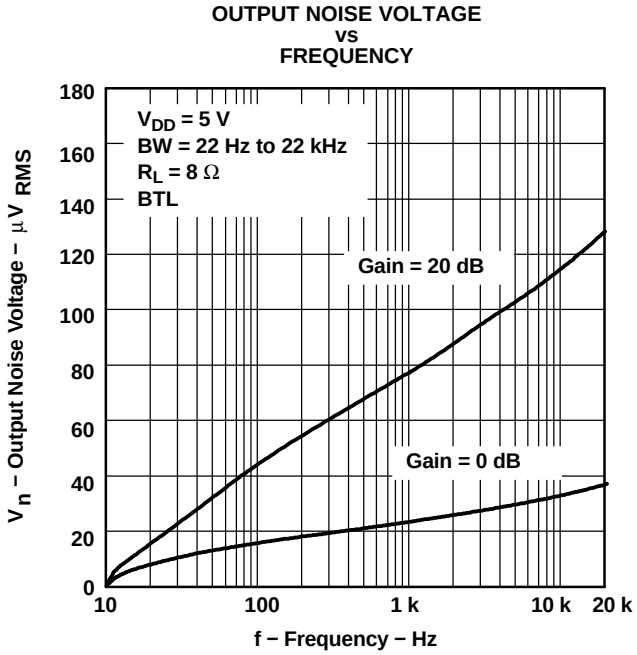
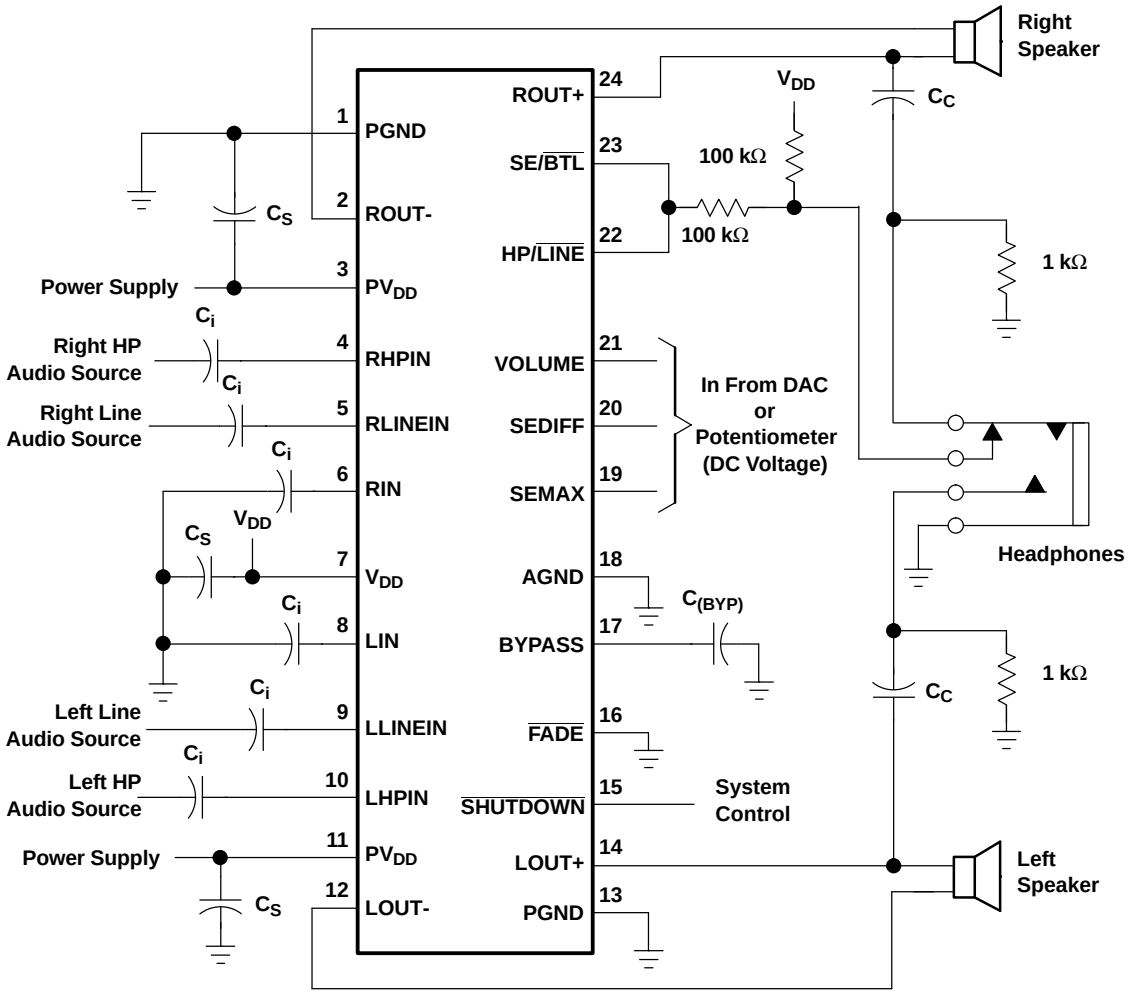

OUTPUT NOISE VOLTAGE
vs
FREQUENCY
V_{DD} = 5 V
BW = 22 Hz to 22 kHz
R_L = 8 Ω
BTL
Gain = 20 dB
Gain = 0 dB
V_n – Output Noise Voltage – μV RMS
180
160
140
120
100
80
60
40
20
0
10
100
1 k
10 k
20 k
f – Frequency – Hz

Figure 27.

APPLICATION INFORMATION

SELECTION OF COMPONENTS

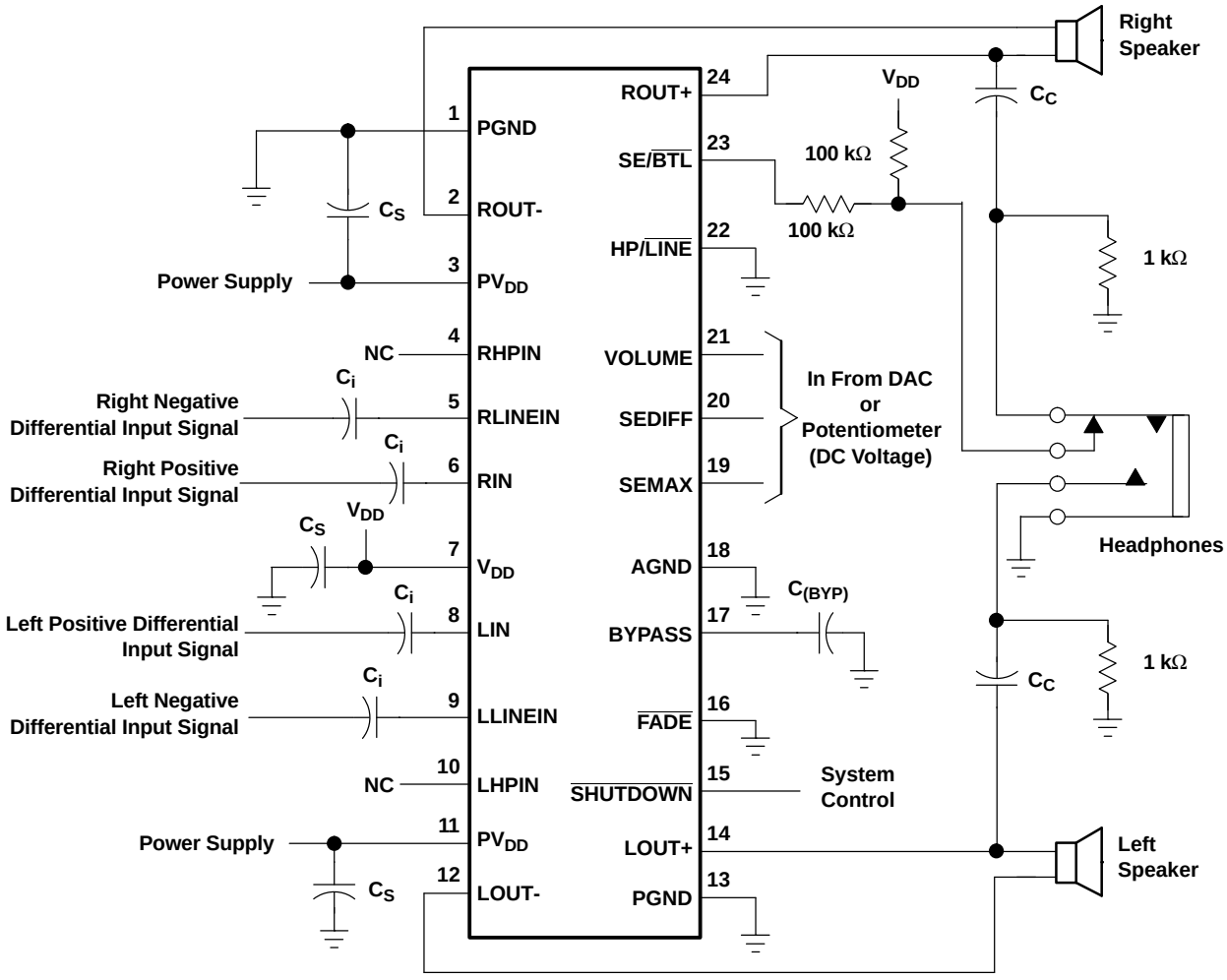
Figure 28 and Figure 29 are schematic diagrams of typical notebook computer application circuits.



A. A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 28. Typical TPA6011A4 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION (continued)



A. A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 29. Typical TPA6011A4 Application Circuit Using Differential Inputs

SE/$\overline{\text{BTL}}$ OPERATION

The ability of the TPA6011A4 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA6011A4, two separate amplifiers drive OUT+ and OUT-. The SE/$\overline{\text{BTL}}$ input controls the operation of the follower amplifier that drives LOUT- and ROUT-. When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA6011A4 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT- amplifiers are in a high output impedance state, which configures the TPA6011A4 as an SE driver from LOUT+ and ROUT+. I_{DD} is reduced by approximately one-third in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 30. The trip level for the SE/$\overline{\text{BTL}}$ input can be found in the *recommended operating conditions* table.

APPLICATION INFORMATION (continued)

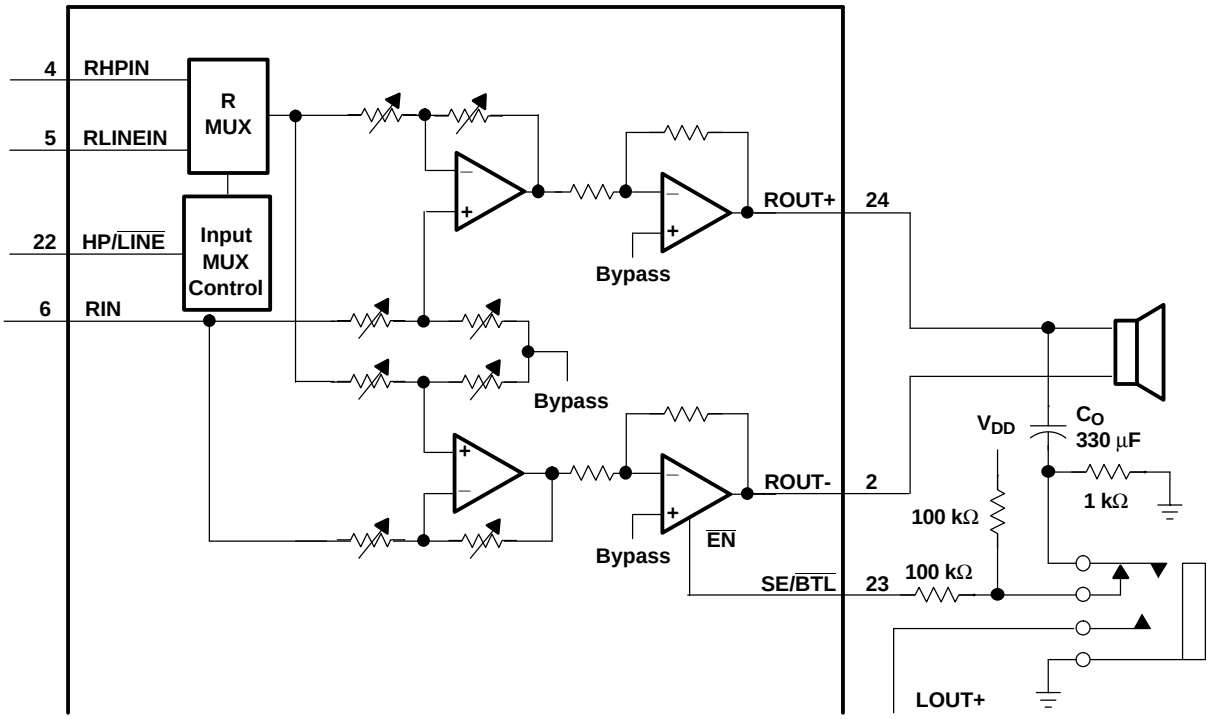


Figure 30. TPA6011A4 Resistor Divider Network Circuit

Using a 1/8-in. (3,5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT- amplifier is shut down causing the speaker to mute (open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_o) into the headphone jack.

HP/$\overline{\text{LINE}}$ OPERATION

The HP/$\overline{\text{LINE}}$ input controls the internal input multiplexer (MUX). Refer to the block diagram in Figure 30. This allows the device to switch between two separate stereo inputs to the amplifier. For design flexibility, the HP/$\overline{\text{LINE}}$ control is independent of the output mode, SE or BTL, which is controlled by the aforementioned SE/$\overline{\text{BTL}}$ pin. To allow the amplifier to switch from the LINE inputs to the HP inputs when the output switches from BTL mode to SE mode, simply connect the SE/$\overline{\text{BTL}}$ control input to the HP/$\overline{\text{LINE}}$ input.

When this input is logic high, the RHPIN and LHPIN inputs are selected. When this terminal is logic low, the RLINEIN and LLINEIN inputs are selected. This operation is also detailed in Table 3 and the trip levels for a logic low (V_{IL}) or logic high (V_{IH}) can be found in the *recommended operating conditions* table.

SHUTDOWN MODES

The TPA6011A4 employs a shutdown mode of operation designed to reduce supply current (I_{DD}) to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 20 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

Table 3. HP/$\overline{\text{LINE}}$, SE/$\overline{\text{BTL}}$, and Shutdown Functions

INPUTS(1)			AMPLIFIER STATE	
HP/$\overline{\text{LINE}}$	SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
X	X	Low	X	Mute
Low	Low	High	Line	BTL
Low	High	High	Line	SE
High	Low	High	HP	BTL
High	High	High	HP	SE

(1) Inputs should never be left unconnected.

$\overline{\text{FADE}}$ OPERATION

For design flexibility, a fade mode is provided to slowly ramp up the amplifier gain when coming out of shutdown mode and conversely ramp the gain down when going into shutdown. This mode provides a smooth transition between the active and shutdown states and virtually eliminates any pops or clicks on the outputs.

When the $\overline{\text{FADE}}$ input is a logic low, the device is placed into fade-on mode. A logic high on this pin places the amplifier in the fade-off mode. The voltage trip levels for a logic low (V_{IL}) or logic high (V_{IH}) can be found in the *recommended operating conditions* table.

When a logic low is applied to the $\overline{\text{FADE}}$ pin and a logic low is then applied on the $\overline{\text{SHUTDOWN}}$ pin, the channel gain steps down from gain step to gain step at a rate of two clock cycles per step. With a nominal internal clock frequency of 58 Hz, this equates to 34 ms (1/24 Hz) per step. The gain steps down until the lowest gain step is reached. The time it takes to reach this step depends on the gain setting prior to placing the device in shutdown. For example, if the amplifier is in the highest gain mode of 20 dB, the time it takes to ramp down the channel gain is 1.05 seconds. This number is calculated by taking the number of steps to reach the lowest gain from the highest gain, or 31 steps, and multiplying by the time per step, or 34 ms.

After the channel gain is stepped down to the lowest gain, the amplifier begins discharging the bypass capacitor from the nominal voltage of $V_{DD}/2$ to ground. This time is dependent on the value of the bypass capacitor. For a 0.47-µF capacitor that is used in the application diagram in Figure 28, the time is approximately 500 ms. This time scales linearly with the value of bypass capacitor. For example, if a 1-µF capacitor is used for bypass, the time period to discharge the capacitor to ground is twice that of the 0.47-µF capacitor, or 1 second. Figure 30 below is a waveform captured at the output during the shutdown sequence when the part is in fade-on mode. The gain is set to the highest level and the output is at V_{DD} when the amplifier is shut down.

When a logic high is placed on the $\overline{\text{SHUTDOWN}}$ pin and the $\overline{\text{FADE}}$ pin is still held low, the device begins the start-up process. The bypass capacitor will begin charging. Once the bypass voltage reaches the final value of $V_{DD}/2$, the gain increases in 2-dB steps from the lowest gain level to the gain level set by the dc voltage applied to the VOLUME, SEDIFF, and SEMAX pins.

In the fade-off mode, the amplifier stores the gain value prior to starting the shutdown sequence. The output of the amplifier immediately drops to $V_{DD}/2$ and the bypass capacitor begins a smooth discharge to ground. When shutdown is released, the bypass capacitor charges up to $V_{DD}/2$ and the channel gain returns immediately to the value stored in memory. Figure 31 below is a waveform captured at the output during the shutdown sequence when the part is in the fade-off mode. The gain is set to the highest level, and the output is at V_{DD} when the amplifier is shut down.

The power-up sequence is different from the shutdown sequence and the voltage on the $\overline{\text{FADE}}$ pin does not change the power-up sequence. Upon a power-up condition, the TPA6011A4 begins in the lowest gain setting and steps up 2 dB every 2 clock cycles until the final value is reached as determined by the dc voltage applied to the VOLUME, SEDIFF, and SEMAX pins.

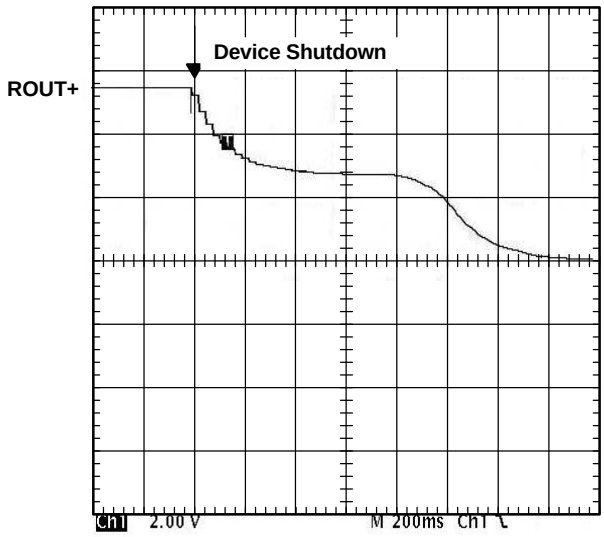


Figure 31. Shutdown Sequence in the Fade-on Mode

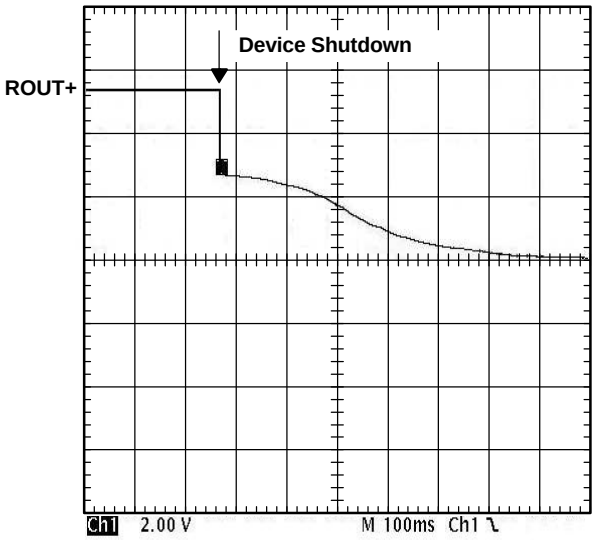


Figure 32. Shutdown Sequence in the Fade-off Mode

VOLUME, SEDIFF, AND SEMAX OPERATION

Three pins labeled VOLUME, SEDIFF, and SEMAX control the BTL volume when driving speakers and the SE volume when driving headphones. All of these pins are controlled with a dc voltage, which should not exceed V_{DD}.

When driving speakers in BTL mode, the VOLUME pin is the only pin that controls the gain. Table 1 shows the gain for the BTL mode. The voltages listed in the table are for V_{DD} = 5 V. For a different V_{DD}, the values in the table scale linearly. If V_{DD} = 4 V, multiply all the voltages in the table by 4 V/5 V, or 0.8.

The TPA6011A4 allows the user to specify a difference between BTL gain and SE gain. This is desirable to avoid any listening discomfort when plugging in headphones. When switching to SE mode, the SEDIFF and SEMAX pins control the singe-ended gain proportional to the gain set by the voltage on the VOLUME pin. When SEDIFF = 0 V, the difference between the BTL gain and the SE gain is 6 dB. Refer to the section labeled *bridged-tied load versus single-ended load* for an explanation on why the gain in BTL mode is 2x that of single-ended mode, or 6dB greater. As the voltage on the SEDIFF terminal is increased, the gain in SE mode decreases. The voltage on the SEDIFF terminal is subtracted from the voltage on the VOLUME terminal and this value is used to determine the SE gain.

Some audio systems require that the gain be limited in the single-ended mode to a level that is comfortable for headphone listening. Most volume control devices only have one terminal for setting the gain. For example, if the speaker gain is 20 dB, the gain in the headphone channel is fixed at 14 dB. This level of gain could cause discomfort to listeners and the SEMAX pin allows the designer to limit this discomfort when plugging in headphones. The SEMAX terminal controls the maximum gain for single-ended mode.

The functionality of the SEDIFF and SEMAX pin are combined to set the SE gain. A block diagram of the combined functionality is shown in Figure 33. The value obtained from the block diagram for SE_VOLUME is a dc voltage that can be used in conjunction with Table 2 to determine the SE gain. Again, the voltages listed in the table are for V_{DD} = 5 V. The values must be scaled for other values of V_{DD}.

Table 1 and Table 2 show a range of voltages for each gain step. There is a gap in the voltage between each gain step. This gap represents the hysteresis about each trip point in the internal comparator. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another. If a potentiometer is used to adjust the voltage on the control terminals, the gain increases as the potentiometer is turned in one direction and decreases as it is turned back the other direction. The trip point, where the gain

actually changes, is different depending on whether the voltage is increased or decreased as a result of the hysteresis about each trip point. The gaps in Table 1 and Table 2 can also be thought of as indeterminate states where the gain could be in the next higher gain step or the lower gain step depending on the direction the voltage is changing. If using a DAC to control the volume, set the voltage in the middle of each range to ensure that the desired gain is achieved.

A pictorial representation of the volume control can be found in Figure 34. The graph focuses on three gain steps with the trip points defined in Table 1 for BTL gain. The dotted line represents the hysteresis about each gain step.

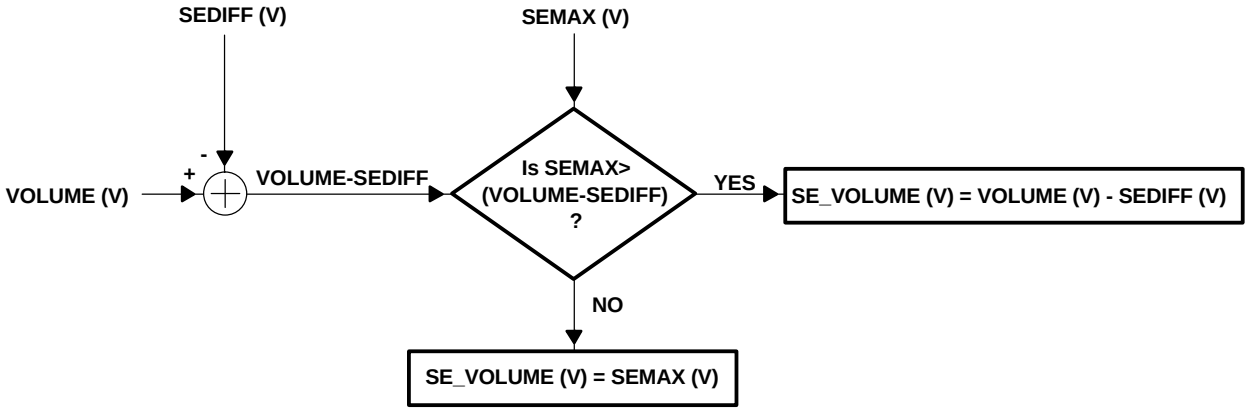


Figure 33. Block Diagram of SE Volume Control

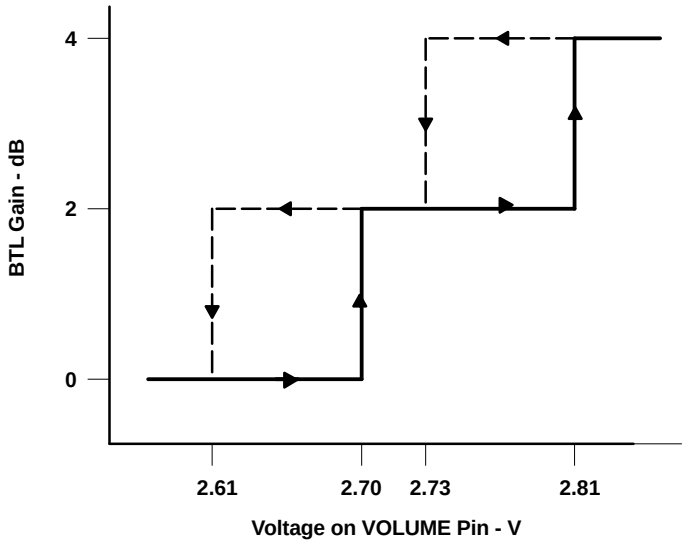


Figure 34. DC Volume Control Operation

INPUT RESISTANCE

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency also changes by over six times.

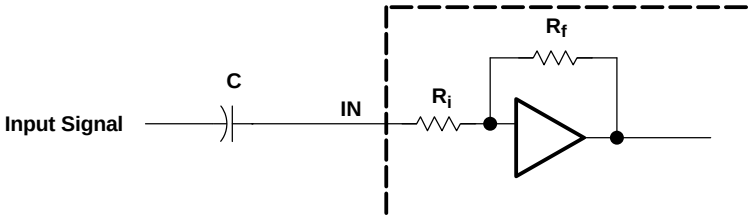


Figure 35. Resistor on Input for Cut-Off Frequency

The input resistance at each gain setting is given in Figure 26.

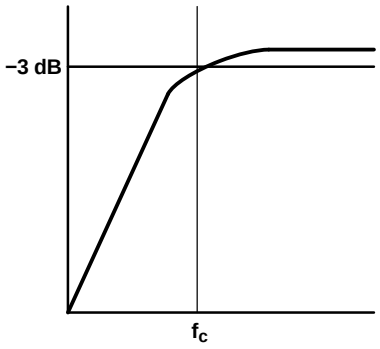
The -3-dB frequency can be calculated using Equation 1.

$$f_{-3\ dB} = \frac{1}{2\pi CR_i} \quad (1)$$

INPUT CAPACITOR, C_i

In the typical application an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (R_i) form a high-pass filter with the corner frequency determined in Equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi R_i C_i} \quad (2)$$



The value of C_i is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_i is 70 kΩ and the specification calls for a flat-bass response down to 40 Hz. Equation 2 is reconfigured as Equation 3.

$$C_i = \frac{1}{2\pi R_i f_c} \quad (3)$$

In this example, C_i is 56.8 nF, so one would likely choose a value in the range of 56 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

POWER SUPPLY DECOUPLING, $C_{(S)}$

The TPA6011A4 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

MIDRAIL BYPASS CAPACITOR, $C_{(BYP)}$

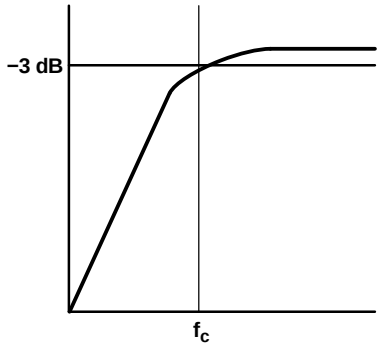
The midrail bypass capacitor ($C_{(BYP)}$) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, $C_{(BYP)}$ determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor ($C_{(BYP)}$) values of 0.47-µF to 1-µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance. For the best pop performance, choose a value for $C_{(BYP)}$ that is equal to or greater than the value chosen for C_i. This ensures that the input capacitors are charged up to the midrail voltage before $C_{(BYP)}$ is fully charged to the midrail voltage.

OUTPUT COUPLING CAPACITOR, $C_{(C)}$

In the typical single-supply SE configuration, an output coupling capacitor ($C_{(C)}$) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 4.

$$f_{c(high)} = \frac{1}{2\eta R_L C_{(C)}} \quad (4)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of $C_{(C)}$ are required to pass low frequencies into the load. Consider the example where a $C_{(C)}$ of 330 µF is chosen and loads vary from 3Ω ,4 Ω, 8 Ω, 32Ω , 10 kΩ, and 47 kΩ. Table 4 summarizes the frequency response characteristics of each configuration.

Table 4. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	$C_{(C)}$	LOWEST FREQUENCY
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 4 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

BRIDGED-TIED LOAD vs SINGLE-ENDED LOAD

Figure 36 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA6011A4 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but, initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see Equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \quad (5)$$

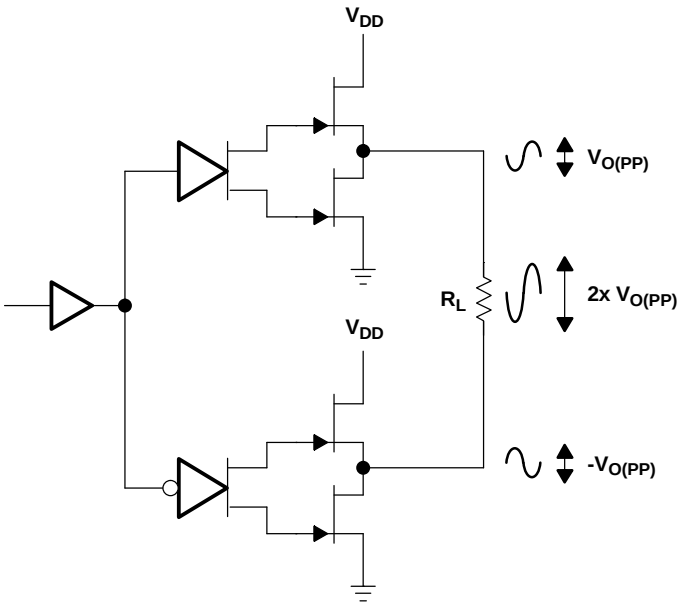


Figure 36. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 37. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF), so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance and is calculated with Equation 6.

$$f_{(c)} = \frac{1}{2\eta R_L C_C} \quad (6)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

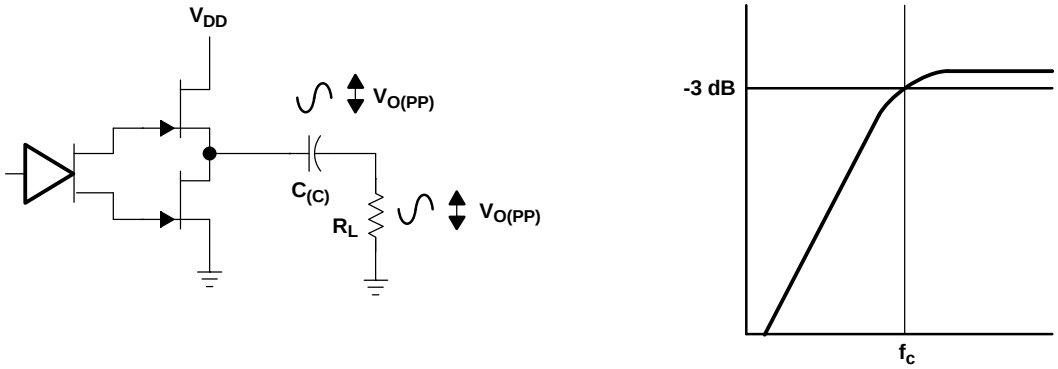


Figure 37. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *crest factor and thermal considerations* section.

SINGLE-ENDED OPERATION

In SE mode (see Figure 37), the load is driven from the primary amplifier output for each channel (OUT+).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and effectively reduces the amplifier's gain by 6 dB.

BTL AMPLIFIER EFFICIENCY

Class-AB amplifiers are inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current (I_{DD}rms) determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 38).

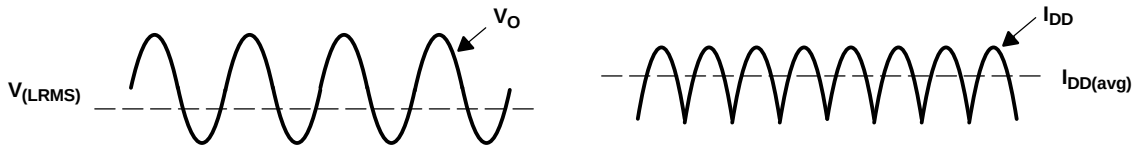


Figure 38. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\eta}\int_0^{\eta} \frac{V_P}{R_L}\sin(t)\,dt = \frac{1}{\eta} \times \frac{V_P}{R_L}\left[\cos(t)\right]_0^{\eta} = \frac{2V_P}{\eta\, R_L}$$

Therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\eta\, R_L} \tag{7}$$

substituting PL and PSUP into Equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P{}^2}{2\, R_L}}{\frac{2\, V_{DD}\, V_P}{\eta\, R_L}} \times \frac{\eta\, V_P}{4\, V_{DD}}$$

Where:

$$V_P = \sqrt{2\, P_L\, R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\sqrt{2\, P_L\, R_L}}{4\, V_{DD}} \tag{8}$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

Table 5 employs Equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 5. Efficiency vs Output Power in 5-V, 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47(1)	0.53

(1) High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

CREST FACTOR AND THERMAL CONSIDERATIONS

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the TPA6011A4 data sheet, one can see that when the TPA6011A4 is operating from a 5-V supply into a 3-Ω speaker, that 4-W peaks are available. Use equation 9 to convert watts to dB.

$$P_{dB} = 10 \text{Log} \frac{P_W}{P_{ref}} = 10 \text{Log} \frac{4\text{ W}}{1\text{ W}} = 6\text{ dB} \tag{9}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

- 6 dB - 15 dB = -9 dB (15-dB crest factor)
- 6 dB - 12 dB = -6 dB (12-dB crest factor)
- 6 dB - 9 dB = -3 dB (9-dB crest factor)
- 6 dB - 6 dB = 0 dB (6-dB crest factor)
- 6 dB - 3 dB = 3 dB (3-dB crest factor)

To convert dB back into watts use equation 10.

$$P_W = 10^{PdB/10} \times P_{ref}$$

= 63 mW (18-db crest factor)
= 125 mW (15-db crest factor)
= 250 mW (12-db crest factor)
= 500 mW (9-db crest factor)
= 1000 mW (6-db crest factor)
= 2000 mW (3-db crest factor) (10)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the worst case, which is 2 W of continuous power output with a 3-dB crest factor, against 12-dB and 15-dB applications significantly affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA6011A4 and maximum ambient temperatures is shown in Table 6.

Table 6. TPA6011A4 Power Rating, 5-V, 3-Ω Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	-3°C
4	1 W (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

Table 7. TPA6011A4 Power Rating, 5-V, 8-Ω Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5	1250 mW (3-dB crest factor)	0.55	100°C
2.5	1000 mW (4-dB crest factor)	0.62	94°C
2.5	500 mW (7-dB crest factor)	0.59	97°C
2.5	250 mW (10-dB crest factor)	0.53	102°C

The maximum dissipated power ($P_{D(max)}$) is reached at a much lower output power level for an 8-Ω load than for a 3-Ω load. As a result, this simple formula for calculating $P_{D(max)}$ may be used for an 8-Ω application.

$$P_{D(max)} \times \frac{2V_{DD}^2}{\eta^2 R_L} \tag{11}$$

However, in the case of a 3-Ω load, the $P_{D(max)}$ occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the $P_{D(max)}$ formula for a 3-Ω load.

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the PWP package is shown in the *dissipation rating table*. Use equation 12 to convert this to $\theta_{JA.}$.

$$\Theta_{JA} \times \frac{1}{\text{Derating Factor}} \times \frac{1}{0.022} \times 45°C/W \tag{12}$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel, so the dissipated power needs to be doubled for two channel operation. Givenθ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated using Equation 13. The maximum recommended junction temperature for the TPA6011A4 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$\begin{aligned} T_A \text{ Max} &= T_J \text{ Max} - \Theta_{JA} P_D \\ &= 150 - 45(0.6 \times 2) = 96°C \text{ (15-dB crest factor)} \end{aligned} \tag{13}$$

NOTE:

Internal dissipation of 0.6 W is estimated for a 2-W system with 15-dB crest factor per channel.

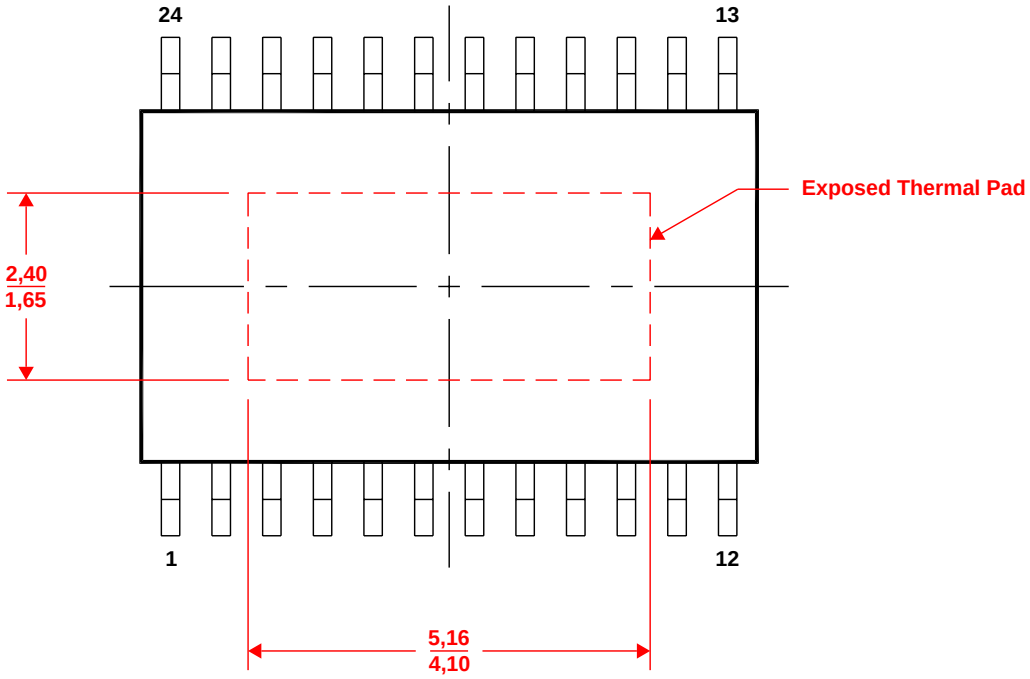
Table 6 and Table 7 show that some applications require no airflow to keep junction temperatures in the specified range. The TPA6011A4 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 6 and Table 7 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers increases the thermal performance by increasing amplifier efficiency.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD Made Easy*, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

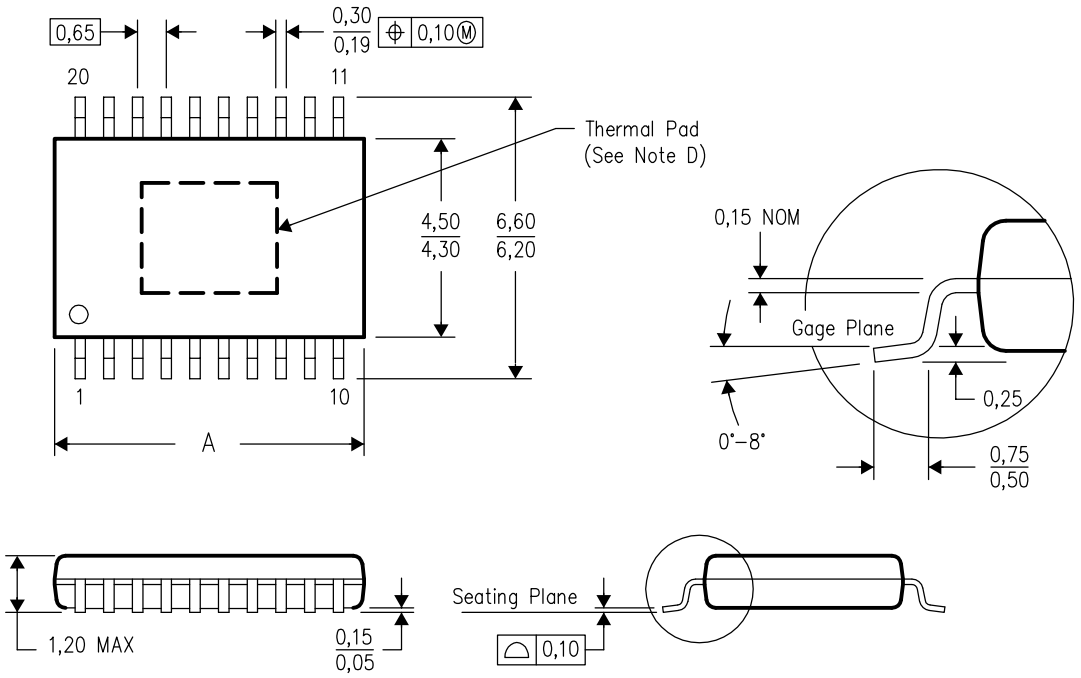
NOTE: All linear dimensions are in millimeters

PPTD030

Exposed Thermal Pad Dimensions

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/G 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

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800mA Low Dropout Positive Adjustable Regulator

FEATURES

- Dropout Voltage 1.2V at 800mA Output Current.
- Fast Transient Response.
- Line Regulation typically at 0.015%.
- Load Regulation typically at 0.1%.
- Internal Thermal and Current Limiting.
- Adjustable Output Voltage or Fixed 2.85V, 3.3V, 5V.
- Standard 3-Pin Power Packages.

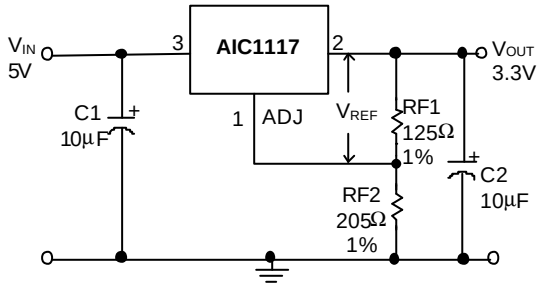
APPLICATIONS

- SCSI-2 Active Terminator.
- Post Regulator for Switching Supply.
- Battery Chargers.
- Constant-Current Regulators.
- PC Add-On Card.

DESCRIPTION

The AIC1117 is a low dropout three terminal regulator with 800mA output current capability. The output voltage is adjustable with the use of a resistor divider. For fixed output voltage versions, the output voltage is internally set at 2.85V, 3.3V or 5V. Dropout is guaranteed at a maximum of 1.3V at maximum output current. Its low dropout voltage and fast transient response make it ideal for low voltage microprocessor applications. Internal current and thermal limiting provides protection against any overload condition that would create excessive junction temperatures.

TYPICAL APPLICATION CIRCUIT



Adjustable Voltage Regulator

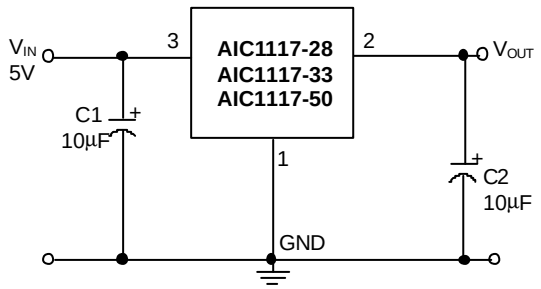
$V_{REF}=V_{OUT}-V_{ADJ}=1.25V$ (typ.)

$V_{OUT}=V_{REF} \times (1+RF2/RF1)+ I_{ADJ} \times RF2$

$I_{ADJ}=55\mu A$ (typ.)

(1) C1 needed if device is far away from filter capacitors.

(2) C2 required for stability.



Fixed Voltage Regulator

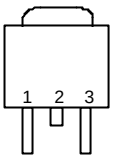
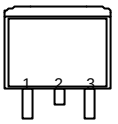
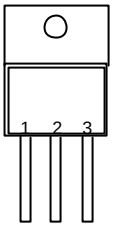
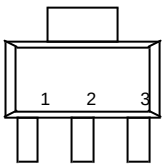
ORDERING INFORMATION

AIC1117-XXXX

PACKAGING TYPE
E: TO-252
M: TO-263
T: TO-220
Y: SOT-223

TEMPERATURE RANGE
C: 0°C~+70°C

OUTPUT VOLTAGE
DEFAULT: ADJ.
28: 2.85V
33: 3.3V
50: 5.0V

ORDER NUMBER	PIN CONFIGURATION
AIC1117CE (TO-252)	FRONT VIEW 1: ADJ (GND) 2: VOUT (TAB) 3: VIN 
AIC1117CM (TO-263)	FRONT VIEW 1: ADJ (GND) 2: VOUT (TAB) 3: VIN 
AIC1117CT (TO-220)	FRONT VIEW 1: ADJ (GND) 2: VOUT (TAB) 3: VIN 
AIC1117CY (SOT-223)	FRONT VIEW 1: ADJ (GND) 2: VOUT (TAB) 3: VIN 

ABSOLUTE MAXIMUM RATINS

VIN pin to ADJ/ GND pin 7V

Operating Junction Temperature Range ..... 0°C ~ 125°C

Storage Temperature Range ..... - 65°C ~ 150°C

Thermal Resistance (Junction to Case) TO-220 ..... 3°C /W

TO-252 .....12.5°C /W

SOT-223 .....15°C /W

Lead Temperature (Soldering) 10 sec. .....260°C

TEST CIRCUIT

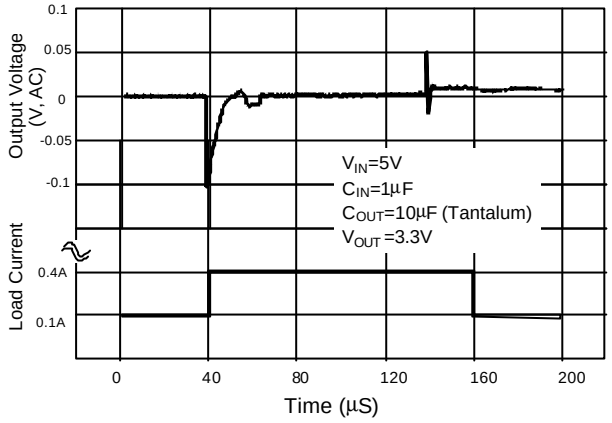
Refer to TYPICAL APPLICATION CIRCUIT.

ELECTRICAL CHARACTERISTICS (V_{IN}=5V, T_J=25°C, I_O=10mA, Unless otherwise specified)

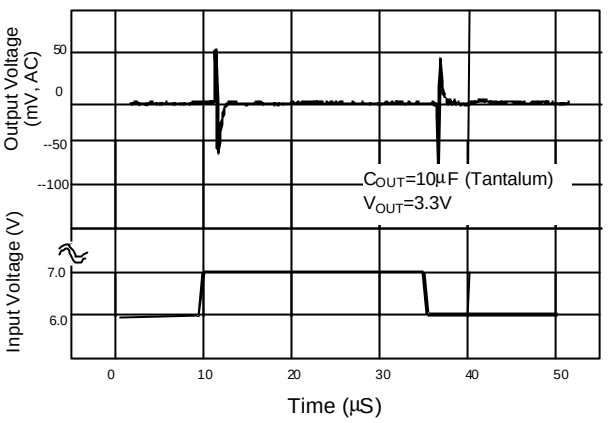
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference Voltage	AIC1117 (Adj.)				
	T_J=25°C	1.238	1.25	1.262	V
	0°C≤T_J≤125°C	1.225	1.25	1.275	
Output Voltage	AIC1117-28, V_{IN}=5V	2.82	2.85	2.88	
	AIC1117-33, V_{IN}=5V	3.26	3.30	3.33	V
	AIC1117-50, V_{IN}=7V	4.95	5.00	5.05	
Line Regulation	2.65≤V_{IN}≤7V				
	T_J=25°C		0.015	0.2	%
	0°C≤T_J≤125°C		0.035	0.2	
Load Regulation	T_J=25°C, I_O=10~800mA		0.1	0.3	%
	0°C≤T_J≤125°C		0.2	0.4	
Dropout Voltage	ΔV_{OUT}, ΔV_{REF}=1%				
	10mA≤I_O≤800mA		1.2	1.4	V
	0°C≤T_J≤125°C				
Current Limit	0°C≤T_J≤125°C	0.85			A
Adjusted Pin Current (I_{ADJ})	2.65≤V_{IN}≤7V				
	10mA≤I_O≤ 800mA		55	120	µA
	0°C≤T_J≤125°C				
Adjusted Pin Current Change (ΔI_{ADJ})	2.65≤V_{IN}≤7V				
	10mA≤I_O≤800mA		0.2	5	µA
	0°C≤T_J≤125°C				
Temperature Stability	I_O=0.5A		0.5		%
	0°C≤T_J≤125°C				
Minimum Load Current	0°C≤T_J≤125°C		5	10	mA
RMS Output Noise (% of V_{OUT})	10Hz≤f≤10KHz		0.003		%
Ripple Rejection Ratio	120Hz input ripple	60	72		dB
	C_{OUT}=25µF				

TYPICAL PERFORMANCE CHARACTERISTICS

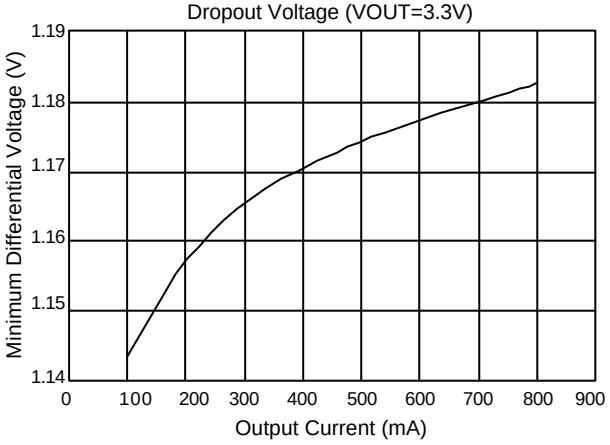
Load Transient Response



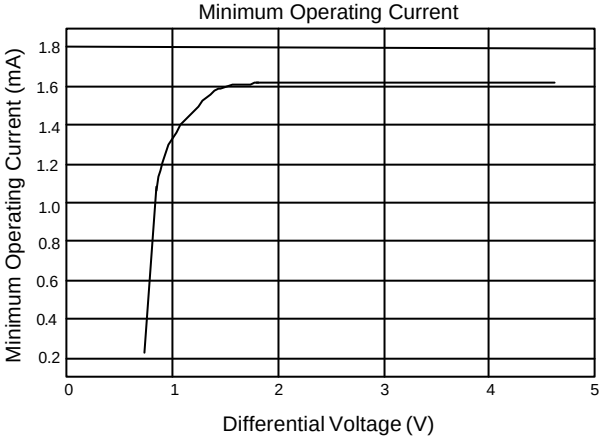
Line Transient Response



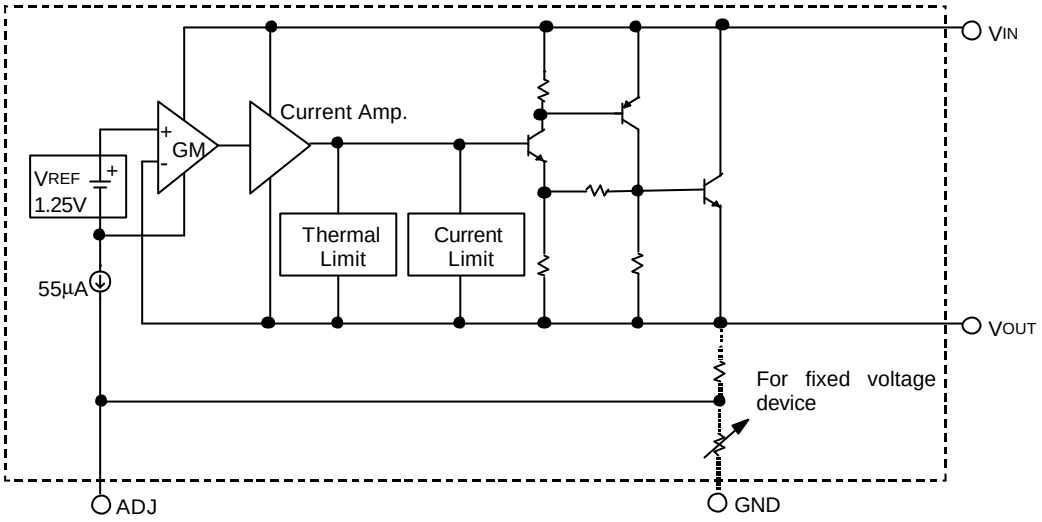
Dropout Voltage (VOUT=3.3V)



Minimum Operating Current



BLOCK DIAGRAM



PIN DESCRIPTIONS

ADJ PIN - Providing V_{REF}=1.25V (typ.) for adjustable V_{OUT}. $V_{REF}=V_{OUT}-V_{ADJ}$ and I_{ADJ}=55µA (typ.)

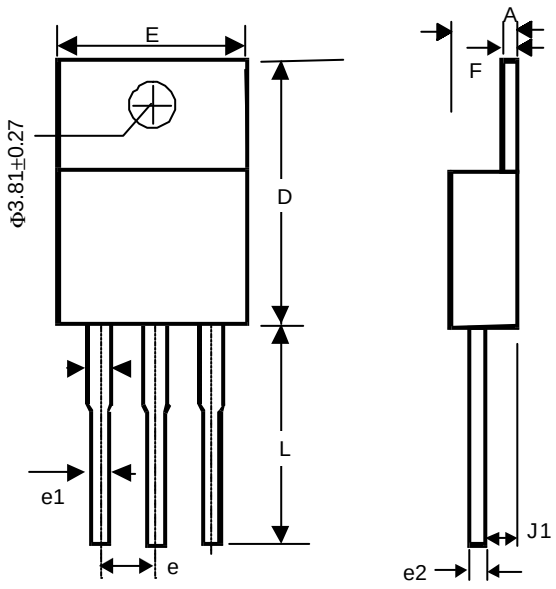
(GND PIN - Power ground.)

VOUT PIN - Adjustable output voltage.

VIN PIN - Power Input.

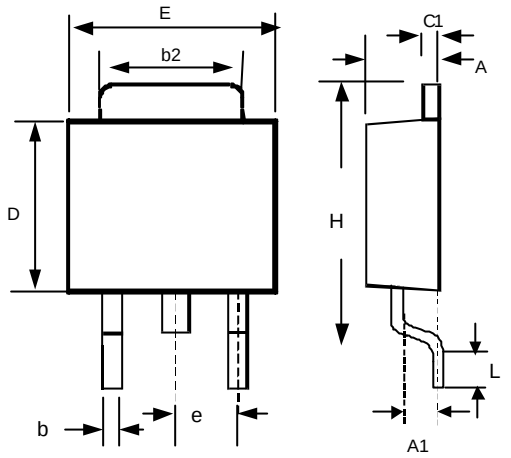
PHYSICAL DIMENSIONS

- **TO-220 (unit: mm)**



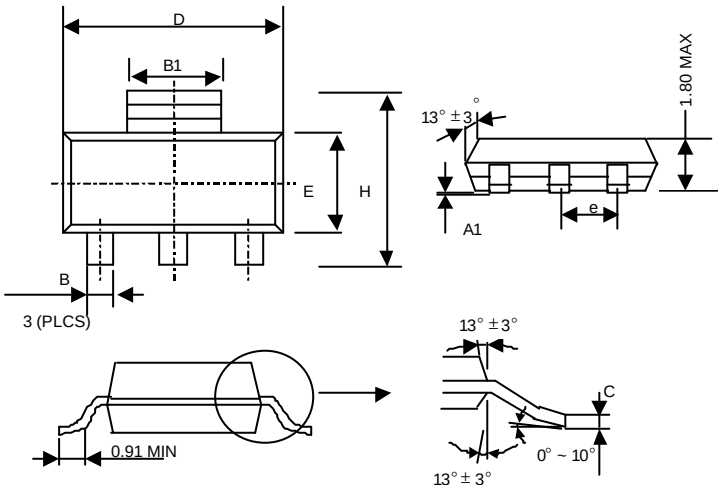
SYMBOL	MIN	MAX
A	3.56	4.82
D	14.23	16.51
E	9.66	10.66
e	2.29	2.79
e1	0.50	1.15
e2	-	1.10
F	0.51	1.39
J1	2.04	2.92
L	12.70	14.73

- **TO-252 (unit: mm)**



SYMBOL	MIN	MAX
A	2.19	2.38
A1	1.02	1.27
b	0.64	0.88
b2	5.21	5.46
C1	0.46	0.58
D	5.33	5.59
E	6.35	6.73
e	2.28 (TYP.)	
H	9.40	10.42
L	0.51	-

- **SOT-223**

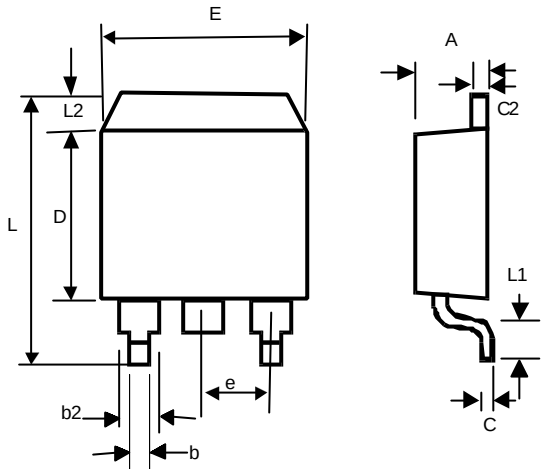


SYMBOL	MIN	MAX
A1	0.02	0.12
B	0.60	0.80
B1	2.90	3.15
C	0.24	0.35
D	6.30	6.80
E	3.30	3.70
e	2.30 (TYP.)	
H	6.70	7.30

- **SOT-223 Marking**

Part No.	Marking
AIC1117CY	AK17
AIC1117-28	AK28
AIC1117-33	AK33
AIC1117-50	AK50

- **TO-263 (unit: mm)**



SYMBOL	MIN	MAX
A	4.06	4.83
b	0.50	1.00
b2	1.14	1.40
C	-	0.7
c2	1.14	1.40
D	8.63	9.66
E	9.65	10.29
e	2.54 (TYP.)	
L	14.60	15.88
L1	2.28	2.80
L2	-	1.40