LITE ARRAY OLED (BVI) CO. LTD.

MODULE NO.: LPST096096A00-T4
DOC.REVISION: 0.0

	SIGNATURE	
PREPARED BY	Fr.li	26-Jan-05
APPROVED BY (R&D)	Wayne Zhao	27-Jan-05
APPROVED BY (Marketing)	Nick Poon	27-Jan-05

PRODUCT PREVIEW

Product Part#:	**LPST096096A00-T4**
Product Name:	**262K color OLED Module**
Revision:	**0.0**
Date:	**Jan'2005**

REVISION RECORD

Revision	Description of Revision	Revision date	Remark
0.0	Initial release	26-Jan-05	--

TABLE OF CONTENTS

1. FUNCTIONS & FEATURES

1.1. Format	: 96(RGB)*96 dots
1.2. Display mode	: Passive Matrix
1.3. Display color	: 262k color
1.4. Duty	: 1/96

2. MECHANICAL SPECIFICATIONS

2.1. Module size	: 27.70mm(W)*40.76mm(H)
2.2. Panel size	: 27.70mm(W)*27.10mm(H)
2.3. Viewing area	: 20.647mm(W)*20.652mm(H)
2.4. Active area	: 19.849mm(W)*19.846mm(H)
2.5. Dot pitch	: 0.207mm(W)*0.207mm(H)
2.6. Dot size	: 0.184mm(W)*0.181mm(H)
2.7. Thickness(with polarizer)	: 1.70mm
2.8. Weight	: TBD

3. BLOCK DIAGRAM

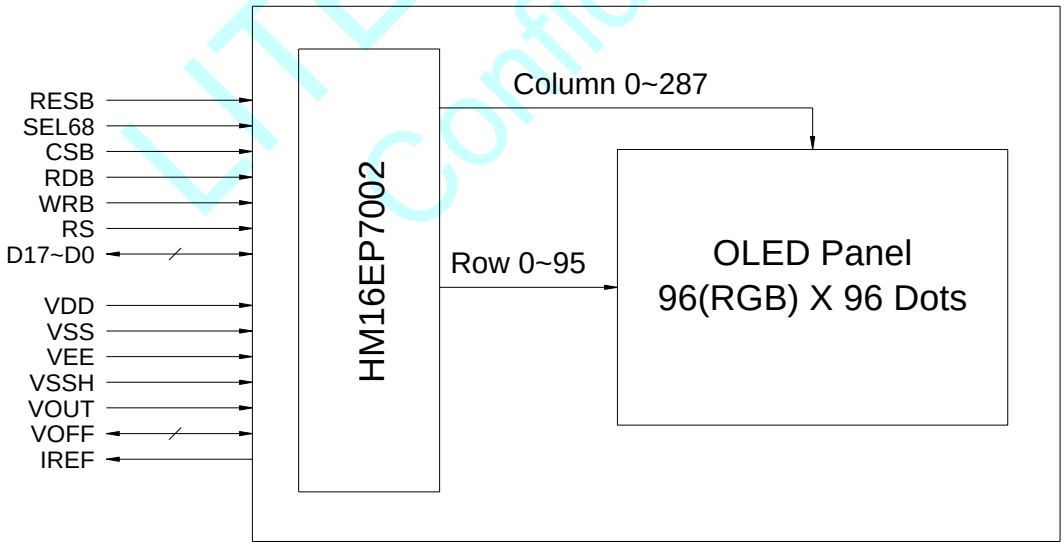


Figure 1: Block diagram

4. DIMENSIONAL OUTLINE

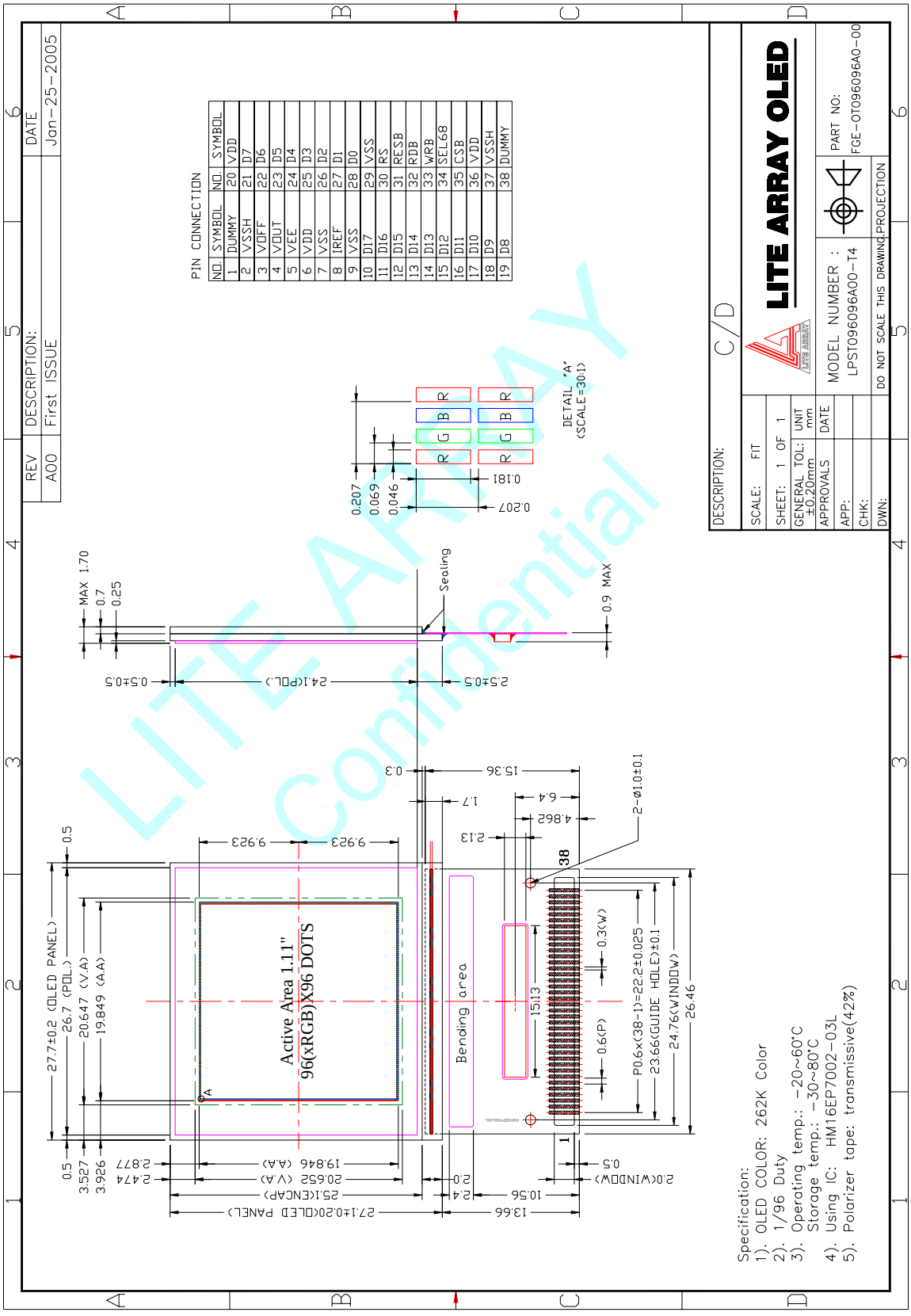


Figure 2: Dimensional outline

5. PIN DESCRIPTION

Pin no.	Symbol	Function
1,38	DUMMY	No connection
2,37	VSSH	High voltage ground pin
3	VOFF	Common driver off-state output port
4	VOUT	High voltage supply & Output pin
5	VEE	Power pin for analog
6,20,36	VDD	Power pin for logic
7,9,29	VSS	Logic ground pin
8	IREF	Reference current pot internally generated
10~19	D17~D8	When parallel interface is selected, data line is connected to CPU 16/18 data bus.
21~28	D7~D0	When parallel interface is selected, data line is connected to CPU 16/18 data bus.
30	RS	Input data selection pin “H” instruction data “L” display data
31	RESB	Reset pin Initializing when RESB=”L”
32	RDB(E)	80 series: RDB signal connection port of 80 series CPU Data bus goes to output state at RDB=”L” 68 series: Enable signal connection port of 68 series CPU Active status when this signal is at “H”
33	WRB(R/W)	80 series: WR signal connection port of 80 series CPU Active at “L” and data bus signal is taken at the rising edge of WRB 68 series: Read/Write control signal “H” read, “L” write
34	SEL68	CPU interface selection pin “L” 80 series, “H” 68 series
35	CSB	Chip selection pin Data in/out is possible when CSB=”L”

Table1: Pin Description

6. ABSOLUTE MAXIMUM RATINGS

6.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	-0.3	4.0	V
	V_{EE}	-0.3	4.0	V
Input voltage	V_{IN}	-0.3	V_{DD}+0.3	V
Operating Temperature	T_{OP}	-30	85	^{o}C
Storage Temperature	T_{STG}	-45	125	^{o}C

Table2: Absolute Maximum Ratings

Note 1: V_{DD} and V_{CC} are on the basis of "VSS = 0.0V"

Note 2: When this module is used beyond above absolute maximum ratings, permanent damage of the module may occur. For normal operation, it is desirable to use this module under the conditions according to the section of "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module will occur and the reliability of the module may deteriorate.

7. OPTICS & ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness(White)	L_{br}	Display average (With polarizer)	30	50	70	Cd/m^2
CIE (Blue)	X	With polarizer	0.11	0.16	0.21	--
	Y		0.11	0.16	0.21	--
CIE (Green)	X		0.25	0.30	0.35	--
	Y		0.58	0.63	0.68	--
CIE (Red)	X		0.58	0.63	0.68	--
	Y		0.32	0.37	0.42	
CIE (White)	X		0.24	0.29	0.34	--
	Y		0.27	0.32	0.37	--
Dark Room Contrast	CR		200	--	--	--
View Angle	A	--	>160	--	--	degree

Table 3: Optics & electrical characteristics

8. ELECTRICAL CHARACTERISTICS

8.1 DC Characteristics

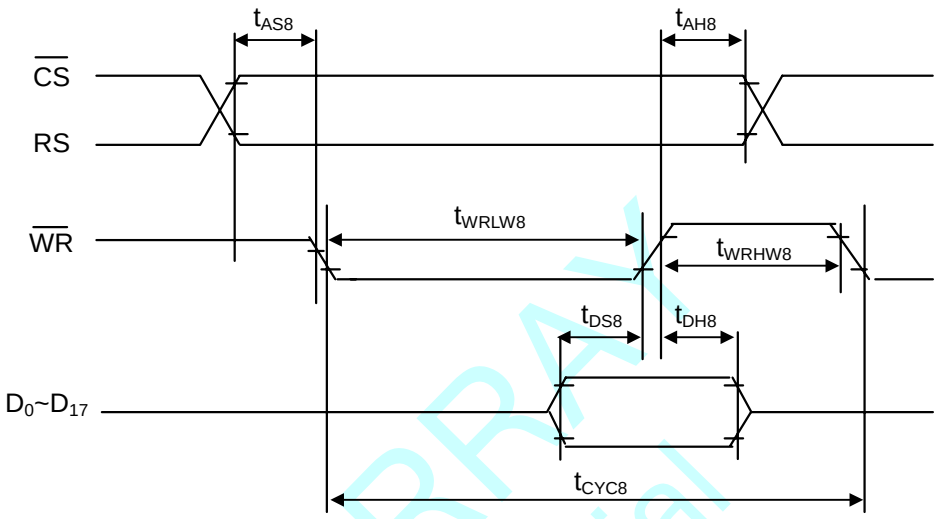
Symbol	Item	Test Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	-	2.4	-	3.3	V
V_{EE}	Supply voltage	-	2.4	-	3.3	V
V_{OUT}	Recommended operating voltage	-	9.0	-	18.0	V
V_{IH}	High level input voltage	-	$0.8V_{DD}$	-	V_{DD}	V
V_{IL}	Low level input voltage	-	0	-	$0.2V_{DD}$	V
V_{OH1}	High level output voltage	I_{OH}=-0.4mA	V_{DD}-0.4	-	-	V
V_{OL1}	Low level output voltage	I_{OL}=-0.4mA	-	-	0.4	V
V_{OH2}	High level output voltage	I_{OH}=-0.1mA	V_{DD}-0.4	-	-	
V_{OL2}	Low level output voltage	I_{OL}=-0.1mA	-	-	0.4	
I_{LI}	Input leakage current	V_I =V_{DD} or V_{SS}	-10	-	+10	μA
I_{LO}	Output leakage current	V_I =V_{DD} or V_{SS}	-10	-	+10	μA
I_{FC}	Forward current	All pixels on	-	14.0	-	mA
V_{FV}	Forward voltage	-	-	17.5	-	V
P_{wr}	Power consumption	30% ON, 50cd/m^2	-	<100	-	mW

Table 4: DC characteristics

8.2 AC Characteristics

8.2.1 System BUS Read/Write Timing (80 series CPU interface)

(Write Timing)



(VDD=2.8~3.3V, Ta=-30~+85℃)

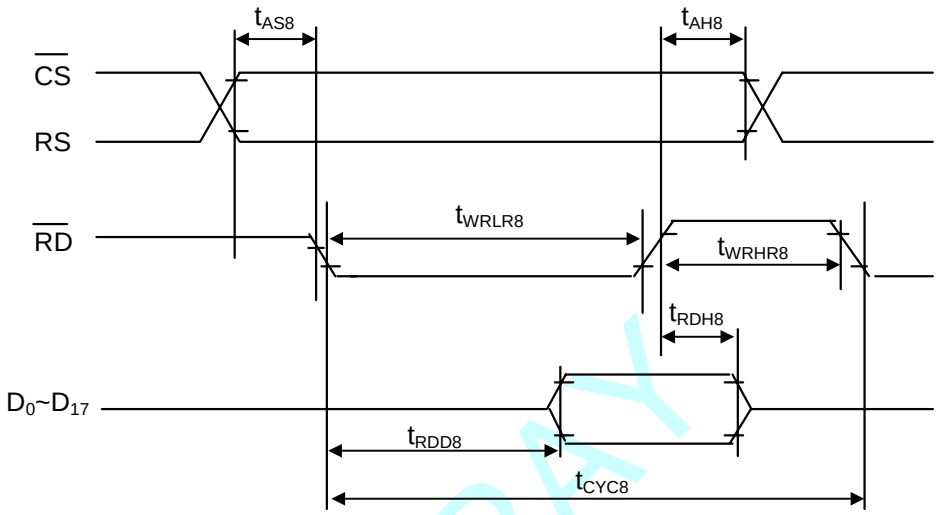
ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH8}		30		ns	CSB
Address setup timing	t_{AS8}		30		ns	RS
System cycle timing	t_{CYC8}		200		ns	WRB
Write "L" pulse width	t_{WRLW6}		45		ns	
Write "H" pulse width	t_{WRHW6}		90			
Data setup timing	t_{DS8}		30		ns	D0~D7
Data hold timing	t_{DH8}		10		ns	

(VDD=2.4~2.8V, Ta=-30~+85℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH8}		30		ns	CSB
Address setup timing	t_{AS8}		30		ns	RS
System cycle timing	t_{CYC8}		250		ns	WRB
Write "L" pulse width	t_{WRLW8}		80		ns	
Write "H" pulse width	t_{WRHW8}		160			
Data setup timing	t_{DS8}		50		ns	D0~D7
Data hold timing	t_{DH8}		10		ns	

Figure 3: Write Timing diagram for 80 series CPU Interface

(Read Timing)



(VDD=2.8~3.3V, Ta=-30~+85℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH8}		30		ns	CSB
Address setup timing	t_{AS8}		30		ns	RS
System cycle timing	t_{CYC8}		500		ns	RDB
Write "L" pulse width	t_{WRLR8}		150		ns	
Write "H" pulse width	t_{WRHR}		90			
Read data output delay time	t_{RDD8}	CL=15pF		100	ns	D0~D7
Data hold timing	t_{RDH}		0		ns	

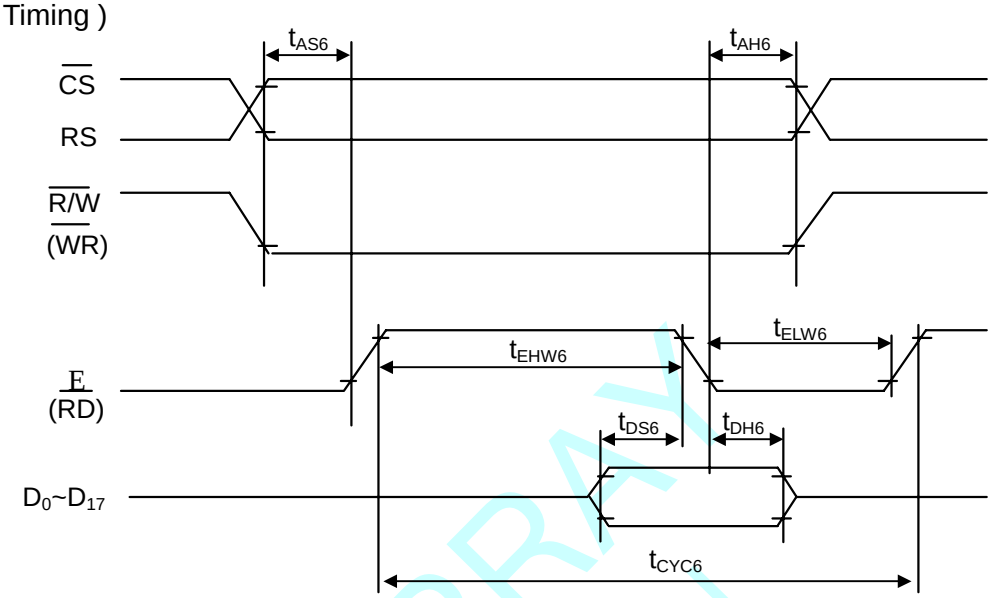
(VDD=2.4~2.8V, Ta=-30~+85℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH8}		30		ns	CSB
Address setup timing	t_{AS8}		30		ns	RS
System cycle timing	t_{CYC8}		500		ns	RDB
Write "L" pulse width	t_{WRLR8}		200		ns	
Write "H" pulse width	t_{WRHR8}		90			
Read data output delay time	t_{RDD8}	CL=15pF		100	ns	D0~D7
Data hold timing	t_{RDH8}		0		ns	

Figure 4: Read Timing diagram for 80 series CPU Interface

8.2.2 System BUS Read/Write Timing (68 series CPU interface)

(Write Timing)



(VDD=2.8~3.3V, Ta=-30~+85℃)

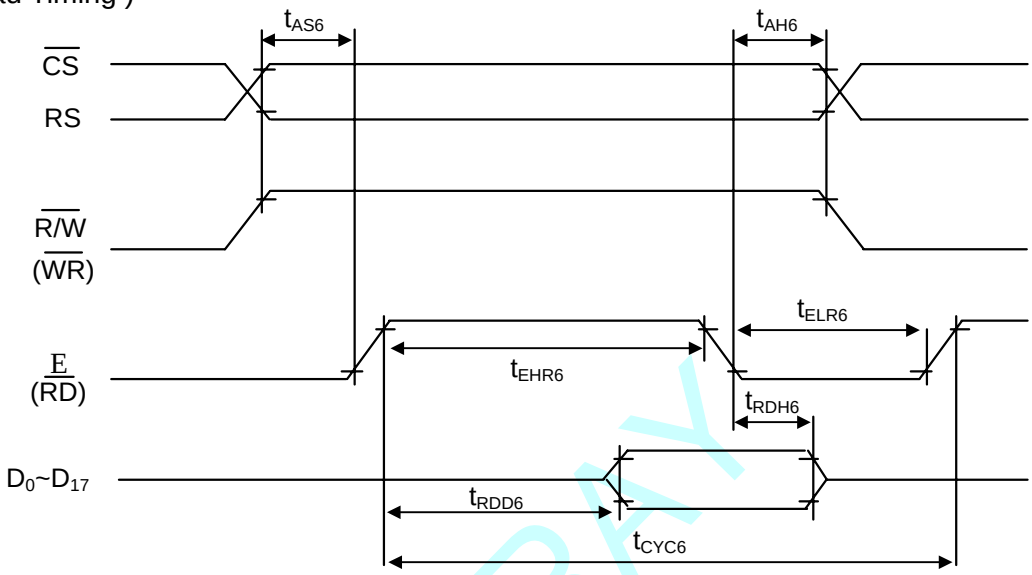
ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH6}		30		ns	CSB
Address setup timing	t_{AS6}		30		ns	RS
System cycle timing	t_{CYC6}		200		ns	E
Write "L" pulse width	t_{ELW6}		90		ns	
Write "H" pulse width	t_{EHW6}		45			
Data setup timing	t_{DS6}		40		ns	D0~D7
Data hold timing	t_{DH6}		10		ns	

(VDD=2.4~2.8V, Ta=-30~+85℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH6}		30		ns	CSB
Address setup timing	t_{AS6}		30		ns	RS
System cycle timing	t_{CYC6}		250		ns	E
Write "L" pulse width	t_{ELW6}		140		ns	
Write "H" pulse width	t_{EHW6}		70			
Data setup timing	t_{DS6}		50		ns	D0~D7
Data hold timing	t_{DH6}		10		ns	

Figure 5: Write Timing diagram for 68 series CPU Interface

(Read Timing)



(VDD=2.8~3.3V, Ta=-30~+85℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH6}		30		ns	CSB
Address setup timing	t_{AS6}		30		ns	RS
System cycle timing	t_{CYC6}		500		ns	E
Write "L" pulse width	t_{ELR6}		90		ns	
Write "H" pulse width	t_{EHR6}		180			
Read data output delay time	t_{RDD6}	CL=15pF		100	ns	D0~D7
Data hold timing	t_{RDH6}		0		ns	

(VDD=2.4~2.8V, Ta=-30~+85℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH6}		40		ns	CSB
Address setup timing	t_{AS6}		40		ns	RS
System cycle timing	t_{CYC6}		500		ns	E
Write "L" pulse width	t_{ELR6}		90		ns	
Write "H" pulse width	t_{EHR6}		200			
Read data output delay time	t_{RDD6}	CL=15pF		100	ns	D0~D7
Data hold timing	t_{RDH6}		0		ns	

Figure 6: Read Timing diagram for 68 series CPU Interface

9. CONTROL AND DISPLAY COMMAND

INSTUCTION	CODE (80 series I/F)							CODE								FUCTION
	CSB	RS	RDB	WRB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Display on/off [0H]	0	1	1	0	0	0	0	0	0	0	0	*	*	*	ON/ OFF	ON/OFF : display on/off control
Power control (1) [1H]	0	1	1	0	0	0	0	0	0	0	1	*	*	AFF	RCD	RCD : Reduced current driving AFF : Alternate Frame Frequency
RAM data mode [2H]	0	1	1	0	0	0	0	0	0	1	0	*	DF2	DF1	DF0	DF2~DF0 : Data length set
Ram access X address (lower) [3H]	0	1	1	0	0	0	0	0	0	1	1	AX3	AX2	AX1	AX0	X-address setting Of display RAM access
Ram access X address (upper) [4H]	0	1	1	0	0	0	0	0	1	0	0	*	AX6	AX5	AX4	X-address setting Of display RAM access
Ram access Y address (lower) [5H]	0	1	1	0	0	0	0	0	1	0	1	AY3	AY2	AY1	AY0	Y-address setting Of display RAM access
Ram access Y address (upper) [6H]	0	1	1	0	0	0	0	0	1	1	0	*	AY6	AY5	AY4	Y-address setting Of display RAM access
Window end X address (lower) [7H]	0	1	1	0	0	0	0	0	1	1	1	EX3	EX2	EX1	EX0	X end address under window mode
Window end X address (upper) [8H]	0	1	1	0	0	0	0	1	0	0	0	*	EX6	EX5	EX4	X end address under window mode
Window end Y address (lower) [9H]	0	1	1	0	0	0	0	1	0	0	1	EY3	EY2	EY1	EY0	Y end address under window mode
Window end Y address (upper) [AH]	0	1	1	0	0	0	0	1	0	1	0	*	EY6	EY5	EY4	Y end address under window mode
Ram access orientation [BH]	0	1	1	0	0	0	0	1	0	1	1	ARST	AR	AYI	AXI	ARST : X,Y increment mode RESET AYI : Y increment/decrement AXI : X increment/decrement AR : first X / first Y
Display control (1) [CH]	0	1	1	0	0	0	0	1	1	0	0	*	*	REV	SW AP	REV : display data positive / negative SWAP : display data swap
Display control (2) [DH]	0	1	1	0	0	0	0	1	1	0	1	*	RM	GM	BM	AM : A position masking BM : B position masking CM : C position masking
Main power control [EH]	0	1	1	0	0	0	0	1	1	1	0	AMP ON	HALT	DC ON	ACL	AMPON : on/off amplifier HALT : power save DCON : boosting circuit on ACL : reset
RE register set [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	RE flag set

INSTUCTION	CODE (80 series I/F)							CODE								FUCTION
	CSB	RS	RDB	WRB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Boosting Coefficient for main (1) [0H]	0	1	1	0	0	0	1	0	0	0	0	*	VU2	VU1	VU0	VU : Boosting voltage setting
Boosting Coefficient for main (1) [1H]	0	1	1	0	0	0	1	0	0	0	1	*	*	VS1	VS0	VS : Booster control clock setting
Panel duty & scan direction [2H]	0	1	1	0	0	0	1	0	0	1	0	*	SHIFT	DS1	DS0	SHIFT : Common shift direction set DS1,DS0 : duty ratio setting
Oscillator RF control [3H]	0	1	1	0	0	0	1	0	0	1	1	CKS	RF2	RF1	RF0	RF : control the feedback resistor of oscillator CKS : oscillation selection
Built-in pattern [4H]	0	1	1	0	0	0	1	0	1	0	0	ALLR	ALLG	ALLB	ALLON	ALL ON : Ready for all on ALL_R,G,B : RED, GREEN, BLUE
Pre_change time RED [5H]	0	1	1	0	0	0	1	0	1	0	1	PCTR3	PCTR2	PCTR1	PCTR0	Pre_charge time setting : RED
Pre_change time GREEN [6H]	0	1	1	0	0	0	1	0	1	1	0	PCTG3	PCTG2	PCTG1	PCTG0	Pre_charge time setting : GREEN
Pre_change time BLUE [7H]	0	1	1	0	0	0	1	0	1	1	1	PCTB3	PCTB2	PCTB1	PCTB0	Pre_charge time setting : BLUE
Pre_change current RED (lower) [8H]	0	1	1	0	0	0	1	1	0	0	0	PCR3	PCR2	PCR1	PCR0	Pre_charge RED current setting
Pre_change current RED (upper) [9H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PCR4	Pre_charge RED current setting
Pre_change current GREEN (lower) [AH]	0	1	1	0	0	0	1	1	0	1	0	PCG3	PCG2	PCG1	PCG0	Pre_charge GREEN current setting
Pre_change current GREEN (upper) [BH]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PCG4	Pre_charge GREEN current setting
Pre_change current BLUE (lower) [CH]	0	1	1	0	0	0	1	1	1	0	0	PCB3	PCB2	PCB1	PCB0	Pre_charge BLUE current setting
Pre_change current BLUE (upper) [DH]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PCB4	Pre_charge BLUE current setting
Address set for internal Register reading [EH]	0	1	1	0	0	0	1	1	1	1	0	*	Address for register reading			Address set for internal register reading out
RE register set [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	RE flag set

INSTUCTION	CODE (80 series I/F)							CODE								FUCTION
	CSB	RS	RDB	WRB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Driving current RED (lower) [0H]	0	1	1	0	0	1	0	0	0	0	0	DC R3	DC R2	DC R1	DC R0	Driving RED current setting
Driving current RED (upper) [1H]	0	1	1	0	0	1	0	0	0	0	1	*	DC R6	DC R5	DC R4	Driving RED current setting
Driving current GREEN (Low er) [2H]	0	1	1	0	0	1	0	0	0	1	0	DC G3	DC G2	DC G1	DC G0	Driving GREEN current setting
Driving current GREEN (upper) [3H]	0	1	1	0	0	1	0	0	0	1	1	*	DC G6	DC G5	DC G4	Driving GREEN current setting
Driving current BLUE (lower) [4H]	0	1	1	0	0	1	0	0	1	0	0	DC B3	DC B2	DC B1	DC B0	Driving BLUE current setting
Driving current BLUE (upper) [5H]	0	1	1	0	0	1	0	0	1	0	1	*	DC B6	DC B5	DC B4	Driving BLUE current setting
VOFF voltage [6H]	0	1	1	0	0	1	0	0	1	1	0	*	*	VO1	VO0	VO : VOFF voltage selection
Scan start line (lower) [7H]	0	1	1	0	0	1	0	0	1	1	1	SC3	SC2	SC1	SC0	Common Driver display size start line point
Scan start line (upper) [8H]	0	1	1	0	0	1	0	1	0	0	0	*	SC6	SC5	SC4	Common Driver display size start line point
Scan end line (lower) [9H]	0	1	1	0	0	1	0	1	0	0	1	EC3	EC2	EC1	EC0	Common Driver display size end line point
Scan end line (upper) [AH]	0	1	1	0	0	1	0	1	0	1	0	*	EC6	EC5	EC4	Common Driver display size end line point
Segment start line (lower) [BH]	0	1	1	0	0	1	0	1	0	1	1	SS3	SS2	SS1	SS0	Segment Driver display size start line point
Segment start line (upper) [CH]	0	1	1	0	0	1	0	1	1	0	0	*	SS6	SS5	SS4	Segment Driver display size start line point
Segment end line (lower) [DH]	0	1	1	0	0	1	0	1	1	0	1	ES3	ES2	ES1	ES0	Segment Driver display size end line point
Segment end line (upper) [EH]	0	1	1	0	0	1	0	1	1	1	0	*	ES6	ES5	ES4	Segment Driver display size end line point
RE register set [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	RE flag set

INSTUCTION	CODE (80 series I/F)							CODE								FUCTION
	CSB	RS	RDB	WRB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Address start line (lower) [0H]	0	1	1	0	0	1	1	0	0	0	0	AR3	AR2	AR1	AR0	Display ram start line addressing setting
Address start line (upper) [1H]	0	1	1	0	0	1	1	0	0	0	1	*	AR6	AR5	AR4	Display ram start line addressing setting
Addressing start Common (lower) [2H]	0	1	1	0	0	1	1	0	0	1	0	AC3	AC2	AC1	AC0	Common display start line addressing setting
Addressing start Common (upper) [3H]	0	1	1	0	0	1	1	0	0	1	1	*	AC6	AC5	AC4	Common display start line addressing setting
Screen saver mode [4H]	0	1	1	0	0	1	1	0	1	0	0	SCS3	SCS2	SCS1	SCS0	SCS3 : Moving window block saver SCS2 : ON/OFF saver SCS1 : Fade IN/OUT saver SCS0 : Display segment saver
Screen saver speed [5H]	0	1	1	0	0	1	1	0	1	0	1	ASS3	ASS2	ASS1	ASS0	ASS3~ASS0 : Auto Scroll Speed
Vertical Scroll Set [6H]	0	1	1	0	0	1	1	0	1	1	0	MBC	FSC	SHH	ALD	MBC : Moving block control FSC : Fade screen saver control SHH : Horizontal SHIFT ALD : Auto scroll line Direction
Horizontal Scroll Set [7H]	0	1	1	0	0	1	1	0	1	1	1	*	SWH	ASL	HE	SWH : Horizontal SWAP ASL : Auto Scroll Line address HE : Horizontal Enable
* [8H]	0	1	1	0	0	1	1	1	0	0	0	*	*	*	*	*
* [9H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	*	*
* [AH]	0	1	1	0	0	1	1	1	0	1	0	*	*	*	*	*
* [BH]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	*	*
Pre_charge full time set [CH]	0	1	1	0	0	1	1	1	1	0	0	PF3	PF2	PF1	PF0	Pre_charge full time setting
TEST 1 [DH]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	*	*
TEST 2 [EH]	0	1	1	0	0	1	1	1	1	1	0	*	*	*	*	*
RE register set [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	RE flag set

INSTUCTION	CODE (80 series I/F)							CODE								FUCTION
	CSB	RS	RDB	WRB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Saver X start address (lower) [0H]	0	1	1	0	1	0	1	0	0	0	0	XS3	XS2	XS1	XS0	Moving window block X start address setting
Saver X start address (upper) [1H]	0	1	1	0	1	0	1	0	0	0	1	*	XS6	XS5	XS4	Moving window block X start address setting
Saver Y start address (lower) [2H]	0	1	1	0	1	0	1	0	0	1	0	YS3	YS2	YS1	YS0	Moving window block Y start address setting
Saver Y start address (upper) [3H]	0	1	1	0	1	0	1	0	0	1	1	*	YS6	YS5	YS4	Moving window block Y start address setting
Saver X end address (lower) [4H]	0	1	1	0	1	0	1	0	1	0	0	XE3	XE2	XE1	XE0	Moving window block X end address setting
Saver X end address (upper) [5H]	0	1	1	0	1	0	1	0	1	0	1	*	XE6	XE5	XE4	Moving window block X end address setting
Saver Y end address (lower) [6H]	0	1	1	0	1	0	1	0	1	1	0	YE3	YE2	YE1	YE0	Moving window block Y end address setting
Saver Y end address (upper) [7H]	0	1	1	0	1	0	1	0	1	1	1	*	YE6	YE5	YE4	Moving window block Y end address setting
* [8H]	0	1	1	0	1	0	1	1	0	0	0	*	*	*	*	*
* [9H]	0	1	1	0	1	0	1	1	0	0	1	*	*	*	*	*
* [AH]	0	1	1	0	1	0	1	1	0	1	0	*	*	*	*	*
* [BH]	0	1	1	0	1	0	1	1	0	1	1	*	*	*	*	*
* [CH]	0	1	1	0	1	0	1	1	1	0	0	*	*	*	*	*
* [DH]	0	1	1	0	1	0	1	1	1	0	1	*	*	*	*	*
* [EH]	0	1	1	0	1	0	1	1	1	1	0	*	*	*	*	*
RE register set [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	RE flag set

Note
1) * mark is don't care.
2) The contents in [ ] mark are the address for reading the internal register.

Table 5: Control and Display Command Table

10. REFERENCE APPLICATION CIRCUIT

This is an example for the application circuit for using LT1930 DC/DC converter. Users can choose their own DC/DC voltage converter.

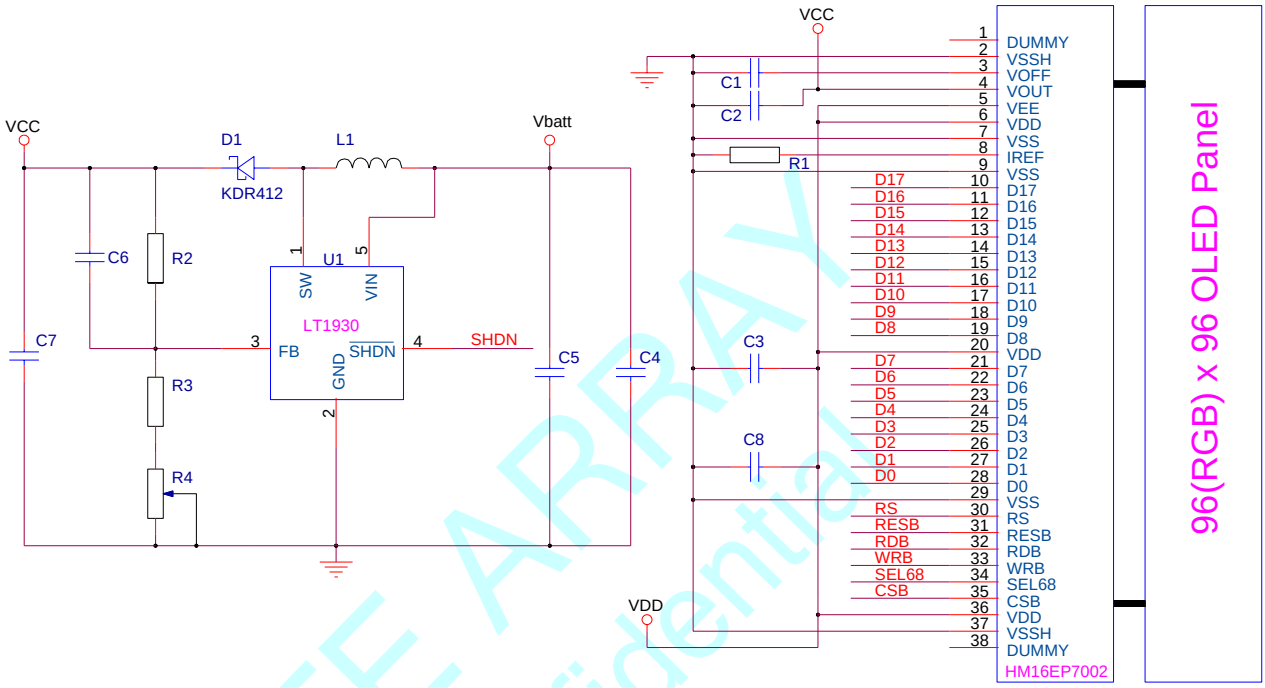


Figure 7: Reference Application Circuit

Notes:

- MPU interface: 68 /80 series parallel interface. It is pin selectable by SEL68.

	68 series parallel interface	80 series parallel interface
SEL68	1	0

- U1: LT1930 DC/DC Converter
- SHDN can be connected to MCU or VDD for alternative solution.

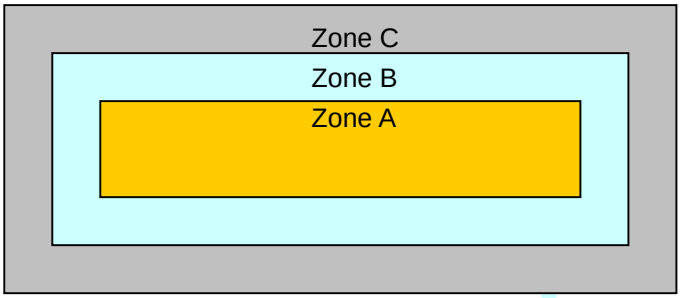
Below table is the component list for the application circuit.

Item	Description
HM16EP7002	OLED Driver IC (*Hynix*)
U1	DC/DC Converter – LT1930 Step-up(*Linear*)
L1	Inductor – 10µH, 500mA, 20%
D1	Schottky Diode – 20V, 500mA
R1	Resistor – 96kΩ, 1%
R2	Resistor – 115kΩ, 1%
R3	Resistor – 8.2kΩ, 1%
R4	Semifixed Resistor – 10kΩ
C2, C4, C8	Capacitor – 0.1µF, 25V
C1, C3, C5, C7	Capacitor – 4.7µF, 20V
C6	Capacitor – 10pF, 50V

Table 7: Component list for the reference application circuit

11. QUALITY SPECIFICATIONS

11.1 Quality guaranty of Zone

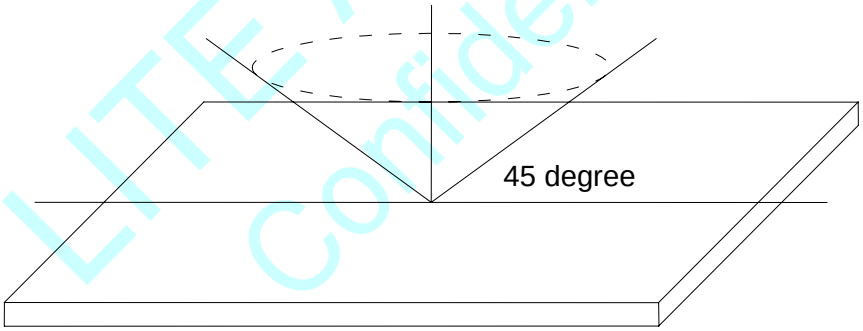


Zone A: Active Area
Zone B: Viewing Area
Zone C: Appearance or other module organization of Zone B

11.2 Inspection Condition

Temperature: 20~30℃
Humidity: 40~70%RH
Pressure: 86~106kPa

Functional and Appearance tests shall be performed when the module is turned ON and OFF respectively, allowing a distance of 30cm or more. The viewing angle for a visual check shall not exceed 45 degrees from the vertical in each direction: forward, backward, right and left (See the sketch below). A sample shall be subject to visual observations under the fluorescent lamp of 40watts.



11.3 AQL

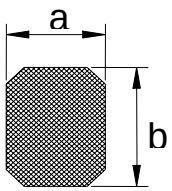
Defect type	Sampling procedures	AQL
Major	MIL-STD-105D Inspection level Ⅰ normal inspection single sample inspection	0.65
Minor	MIL-STD-105D Inspection level Ⅰ normal inspection single sample inspection	1.5

***Major defect**
A major defect refers to the defect, which is considered to substantial degradation to the usability for product application.

***Minor defect**
A minor defect refers to the defect, which is not considered to be substantial degradation for product application, or the defect, which deviate from the existing standards, and it is almost unrelated to the effective use of the product or its operation.

11.4 Inspection standards

The size of foreign object or black spot shall be defined as follows



D (mm) = (a + b) / 2 [When changing square, length of a side]

1) Major

Zone	Item	Judgment
A. B (turn on)	Non display	No non display is allowed
	Irregular operating	No irregular operation is allowed
	Short	No shorts are allowed
	Open	Any segments or common patterns that don't active are rejected.

2) Minor

2-1) Alien substance, Blemish

Zone	D size (mm)	Judgment
A.B (turn on)	D ≤ 0.10	Pass
	0.10 < D ≤ 0.15	2
	0.15 < D ≤ 0.20	1
	0.20 < D	0

2-2) Scratch on Polarizer

Zone	Width (W, mm)	Length (L, mm)	Judgment
A.B (turn on)	W≤0.03	Pass	Pass
	0.03<W≤0.05	L≤2.0	Pass
		L>2.0	1
	0.05<W≤0.08	L>1.0	1
		L≤1.0	Pass
	0.08<W	(*)	(*)

2-3) Polarizer Bubble

Zone	D size (diameter, mm)	Judgment
A.B (turn on)	D ≤ 0.20	PASS
	0.20 < D ≤ 0.50	3
	0.50 < D ≤ 0.80	2
	0.80 < D	FAIL

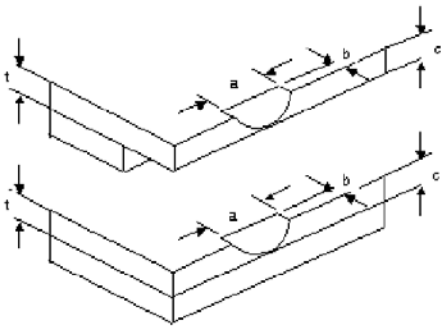
2-4) White/Dark Spot (Spot/Line type)

Zone	D size (mm)	Judgment
A.B (turn on)	D ≤ 0.15	PASS
	0.15 < D ≤ 0.20	3
	0.20 < D ≤ 0.30	2
	0.30 < D	FAIL

Zone	Width (W, mm)	Length (L, mm)	Judgment
A.B (turn on)	0.03<W ≤ 0.04	10<L	5
	0.04<W ≤ 0.06	5.0<L ≤ 10	3
	0.06<W ≤ 0.07	1.0<L ≤ 5.0	2
	0.07<W ≤ 0.09	L ≤ 1.0	1

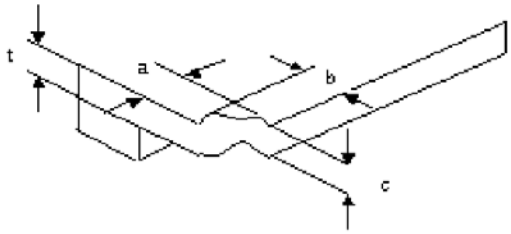
3) CRACKS

①General crack(unit : mm)

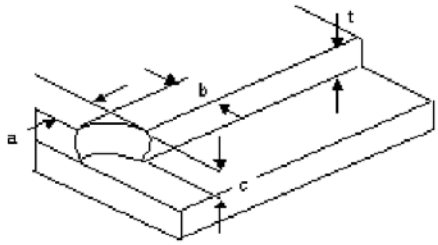


a ≤ 1/6 panel length
b ≤ 1
c ≤ t

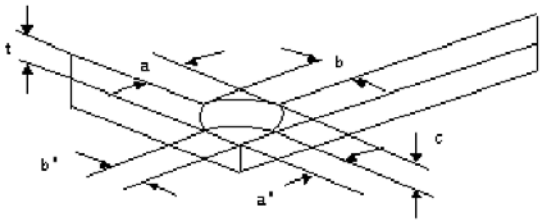
②Corner crack(unit :mm)



a ≤ 2.5	NO EXPOSURE ANY CONDUCTIVE MATERAL
b ≤ 2.5	
c ≤ t	

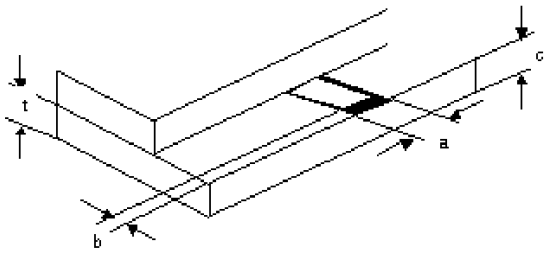


a ≤ 0.7	NO EXPOSURE ANY CONDUCTIVE MATERAL
b ≤ 0.7	
c ≤ t	



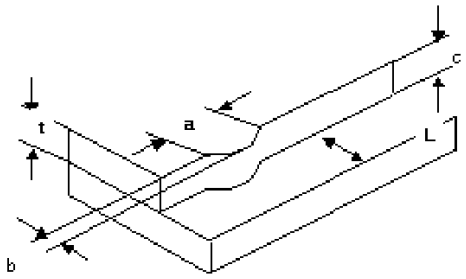
a ≤ 1.3	a ' ≤ a
b ≤ 1.3	b ' ≤ b
c ≤ t	

③Electrode pad crack (unit : mm)



a ≤ 1/6 panel length
b ≤ 1/6 pad length
c ≤ t

④Glass chip remain (unit : mm)



a ≤ 1/6 panel length
b ≤ 1/10 pad length
c ≤ t

⑤Future crack (unit: mm)

NO TOLERATION ANY PROGRESSING CRACK

11.5 Reliability test condition

Operating life time (30% ON, 50cd/ m_2) : Longer than 10,000 hours
Reliability characteristics shall meet following requirements

No.	ITEM	CONDITION	TEST TIME	CRITERION
1	High Humidity Storage	60±2℃,90±5%RH	96 Hrs	Brightness: over 50% of initial value. Color coordination: within ±0.05 of initial value.
2	High Humidity Operation	60±2℃,90±5%RH	96 Hrs	
3	High Temperature Storage	80±2℃	96 Hrs	
4	High Temperature Operation	60±2℃	96 Hrs	
5	Low Temperature Storage	-30±2℃	96 Hrs	
6	Low Temperature Operation	-20±2℃	96Hrs	
7	Thermal shock	-30℃(30min) →80℃(30min) 5Cycles, Transient time = 10 min (Turn off) -20℃(30min) → 70℃(30min) 5 Cycles Transient time = 10 min (Turn on)		Appearance or E/T inspection: follows working specification.
8	Vibration test (Packaging state)	1.Operating time: 2hrs exposure in each direction (X, Y, Z) 2. Frequency (1min): 10 to 55Hz 3. Amplitude: 2mm		There isn't crack and broken on soldering part.
9	Drop test (Packaging state)	1. Direction: 1 corner, 3 edges, 6 faces, drop once for each direction 2. 3 times height 1.8m or 5 times height 1.5m from concrete surface		There isn't crack and broken on soldering part.
10	ESD	150Pf, 330Ω,±8kV 10times, air discharge		After testing, cosmetic and electrical defects should not happen. Total current consumption should be double of initial value.