LITE ARRAY OLED (BVI) CO. LTD.

MODULE NO.: LPSF096064A01-T3
DOC.REVISION: 1.0

	SIGNATURE	
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APPROVED BY (R&D)	Wayne Zhao	9-Sep-05
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PRODUCT PREVIEW

Product Part#:	**LPSF096064A01-T3**
Product Name:	**65K color OLED Module**
Revision:	**1.0**
Date:	**Sep'2005**

REVISION RECORD

Revision	Description of Revision	Revision date	Remark
0.0	Initial release	8-Sep-05	--

TABLE OF CONTENTS

1. FUNCTIONS & FEATURES

1.1. Format	: 96(BGR)*64 dots
1.2. Display mode	: Passive Matrix
1.3. Display color	: 65k color
1.4. Duty	: 1/64

2. MECHANICAL SPECIFICATIONS

2.1. Module size	: 26.66mm(W)*33.17mm(H)
2.2. Panel size	: 26.66mm(W)*20.38mm(H)
2.3. Active area	: 20.135mm(W)*13.415mm(H)
2.4. Dot pitch	: 0.210mm(W)*0.210mm(H)
2.5. Dot size	: 0.185mm(W)*0.185mm(H)
2.6. Thickness(with polarizer)	: 1.66mm
2.7. Weight	: TBD

3. BLOCK DIAGRAM

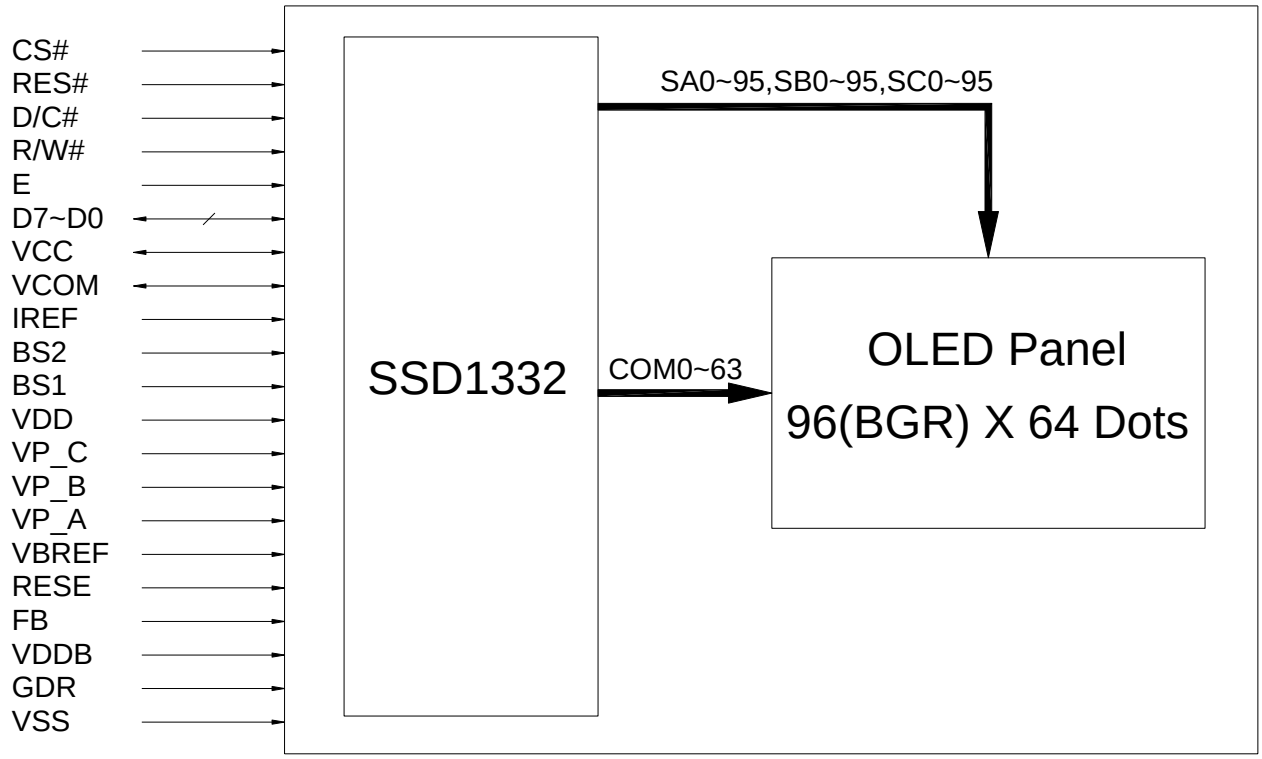


Figure 1. Block diagram

4. DIMENSIONAL OUTLINE

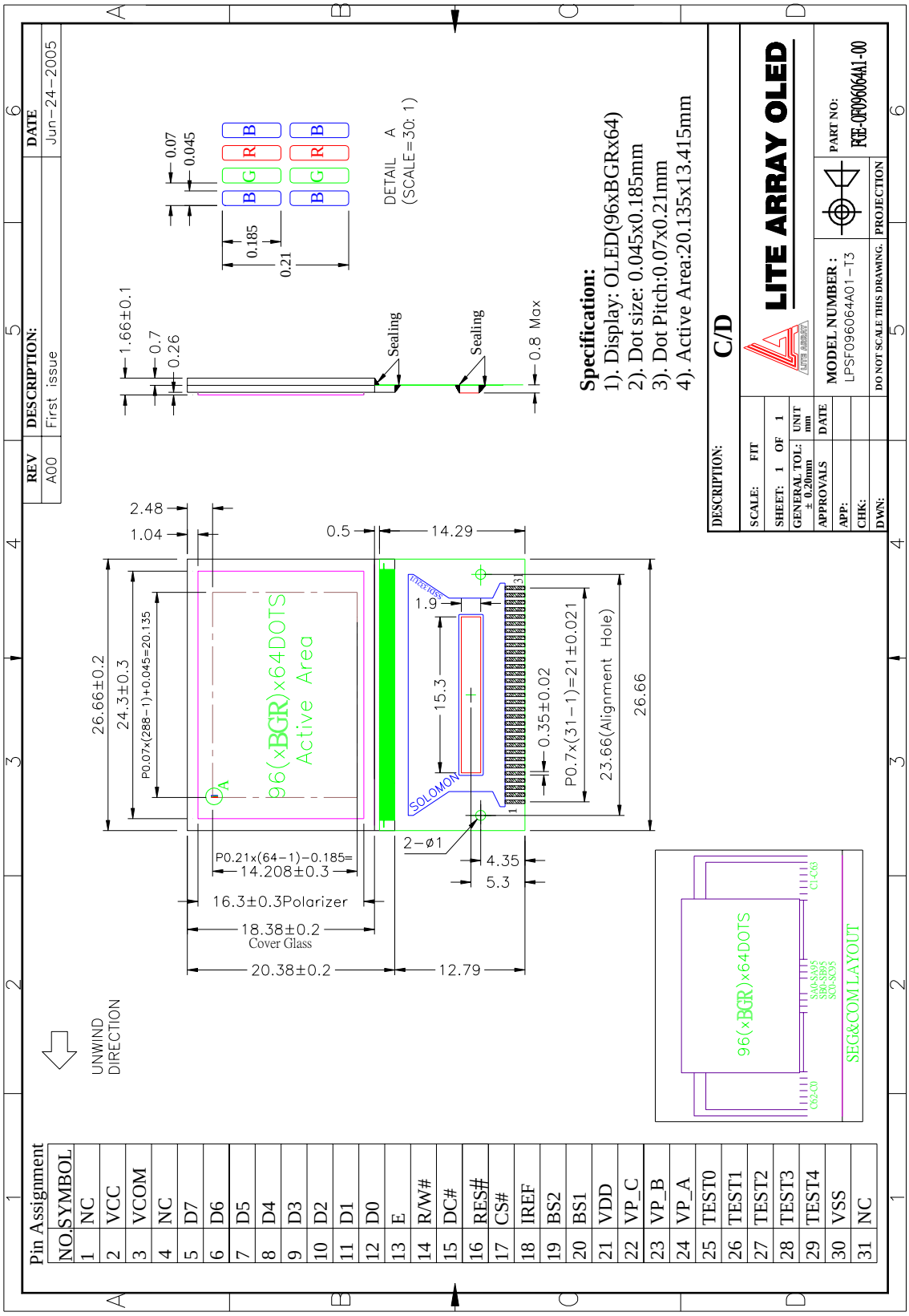


Figure 2. Dimensional outline

5. PIN DESCRIPTION

<table>
<tr><th>Pin no.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1,4,31</td><td>NC</td><td>These are reserved pins and should not be connected. Do not group or short NC pins.</td></tr>
<tr><td>2</td><td>VCC</td><td>Supply voltage for OLED
This is the most positive voltage supply pin of the chip. It is supplied either by external high voltage source or internal booster.</td></tr>
<tr><td>3</td><td>VCOMH</td><td>This pin is the input pin for the voltage output high level for COM signals. It can be supplied externally or internally. When VCOMH is generated internally, a capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>5~12</td><td>D7~D0</td><td>These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial interface mode is selected, D1 will be the serial data input and D0 will be the serial clock input.</td></tr>
<tr><td>13</td><td>E(RD#)</td><td>This pin is MCU interface input.
• When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected.
• When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and the chip is selected.
• When serial interface is selected, this pin E(RD#) must be connected to VSS.</td></tr>
<tr><td>14</td><td>R/W(WR#)</td><td>This pin is MCU interface input.
• When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.
• When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the chip is selected.
• When serial interface is selected, this pin RW#(WR#) must be connected to VSS.</td></tr>
<tr><td>15</td><td>D/C#</td><td>This pin is Data/Command control pin.
• When the pin is pulled high, the data at D7-D0 is treated as display data.
• When the pin is pulled low, the data at D7-D0 will be transferred to the command register.</td></tr>
<tr><td>16</td><td>RES#</td><td>This pin is reset signal input.
When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>17</td><td>CS#</td><td>This pin is the chip select input.
The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>18</td><td>IREF</td><td>This pin is the segment output current reference pin.
A resistor should be connected between this pin and VSS.</td></tr>
<tr><td>19,20</td><td>BS2, BS1</td><td>These input pins are used to configure MCU interface selection by appropriate logic setting, which is described in the following table:
<table>
<tr><th></th><th>6800-parallel interface (8 bit)</th><th>8080-parallel interface (8 bit)</th></tr>
<tr><td>BS1</td><td>0</td><td>1</td></tr>
<tr><td>BS2</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
</table>

Pin no.	Symbol	Function
21	VDD	Power Supply pin for logic operation of the driver. It must be connected to external source.
22,23,24	VP_C VP_B VP_A	These pins are the pre-charge driving voltages for OLED driving segment pins SA0-SA95 (Red), SB0-SB95 (Green) and SC0-SC95 (Blue) respectively. They can be supplied externally or internally generated by VP circuit. When internal VP is used, VP_A, VP_B, VP_C pins should be left open.
25,26,27 28,29	TEST0~ TEST4	No connection.
30	VSS	Ground pin. It must be connected to external ground.

Table1: Pin Description

6. ABSOLUTE MAXIMUM RATINGS

6.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage	V_{DD}	-0.3	4.0	V	1
	V_{CC}	0	18	V	1
	V_{REF}	0	18	V	1
Supply Voltage/Output voltage	V_{COMH}	0	18	V	1
SEG/COM output voltage	-	0	18	V	1
Input voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V	1
Operating Temperature	T_{OP}	-20	70	^{o}C	--
Storage Temperature	T_{STG}	-40	80	^{o}C	--

Table2: Absolute Maximum Ratings

Note 1: Voltage Reference To V_{SS}.

7. OPTICS & ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (White)	L_{br}	Display average (With polarizer)	55	75	--	Cd/m^2
CIE (Blue)	X	With polarizer	0.12	0.16	0.20	--
	Y		0.18	0.22	0.26	--
CIE (Green)	X		0.23	0.27	0.31	--
	Y		0.52	0.56	0.60	--
CIE (Red)	X		0.57	0.61	0.65	--
	Y		0.34	0.38	0.42	
CIE (White)	X		0.23	0.28	0.33	--
	Y		0.30	0.35	0.40	--
Dark Room Contrast	CR		100	--	--	NC
View Angle	A	--	>160	--	--	Degree

Table 3: Optics & electrical characteristics

Condition:

(1) Brightness =75Cd/m^2. Pixel On =100%,V_{DD}=3.3V, V_{CC}=17V, Ta=25℃, R_{ref}=1.2MΩ. MasterCurrentControl=07H, SetContrastForColorA=64H, SetContrastForColorB=3CH, SetContrastForColorC=64H.

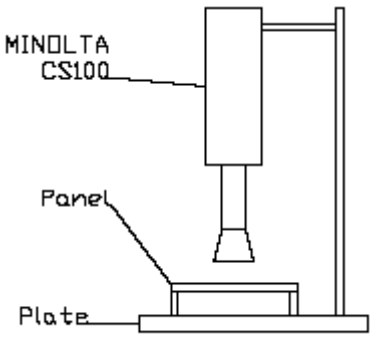
(2) Contrast Ratio=Brightness of the selected spot (White pattern area)/brightness of the unselected spot (Black pattern area)

(3) The elapsed time that the brightness is decreased to the half of initial value, when operated continuously.

(4) Test Command: Display OFF command.

(5) All pixels on

Tester: MINOLTA CS100 Color Analyzer



8. ELECTRICAL CHARACTERISTICS

8.1 DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage		14	17	17.5	V
V_{DD}	Logic Supply Voltage		2.4	2.7	3.5	V
V_{OH}	High Logic Output Level	Iout =300uA, 3.3MHz	$0.9V_{DD}$	-	V_{DD}	V
V_{OL}	Low Logic Output Level	Iout =300uA, 3.3MHz	0	-	$0.1V_{DD}$	V
V_{IH}	High Logic Input Level	Iout =300uA, 3.3MHz	$0.8V_{DD}$	-	V_{DD}	V
V_{IL}	Low Logic Input Level	Iout =300uA, 3.3MHz	0	-	$0.2V_{DD}$	V
I_{SLEEP}	Sleep Mode Current	VDD=2.7V, Display OFF, NO Panel attached	-	--	5	uA
I_{CC}	V_{CC} Supply Current	V_{DD}=2.7V, V_{CC}=11V Display ON Contrast =FF, No panel attached	-	770	-	uA
I_{DD}	V_{DD} Supply Current	V_{DD}=2.7V, V_{CC}=11V Display ON Contrast =FF, No panel attached	-	170		uA
Ifc	Forward current	All pixel on	-	12	-	mA
Pwr	Power consumption	Display off mode	-	3.0	--	mW
		Normal Type	-	--	222	mW

Table 4: DC characteristics

8.2 AC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD}=2.4TO3.5V,Ta=25 ^{o}C)

Symbol	Parameter	Test Condition	Min	Typ.	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	V_{DD}=2.7V	--	0.97	--	MH_Z
F_{FRM}	Frame Frequency for 64 MUX Mode	96RGB x 64 Graphic Display Mode, Display ON, Internal Oscillator Enabled	--	F_{OSC} X1/(D* K*64)	--	H_Z

Table 5: AC characteristics

D: divide ratio (POR=1)
K: number of display clocks (POR=136, i.e.phase1 dclk+phase2 dclk+phase3 dclk=4+7+125)

8.2 Characteristics

8.2.1 6800-Series MPU Parallel Interface Timing Characteristics

(V_{DD}-V_{SS}=2.4 to 3.5V, T_{OP}=-40 to 85℃)

Symbol	Parameter	Min	Max	Unit
t_{cycle}	Clock cycle time	300	--	ns
t_{AS}	Address Setup Time	0	--	ns
t_{AH}	Address Hold Time	0	--	ns
t_{DSW}	Write Data Setup Time	40	--	ns
t_{DHW}	Write Data Hold Time	15	--	ns
t_{DHR}	Read Data Hold Time	20	--	ns
t_{OH}	Output Disable Time	--	70	ns
t_{ACC}	Access Time	--	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-- --	ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-- --	ns ns
t_R	Rise time	--	15	ns
t_F	Fall time	--	15	ns

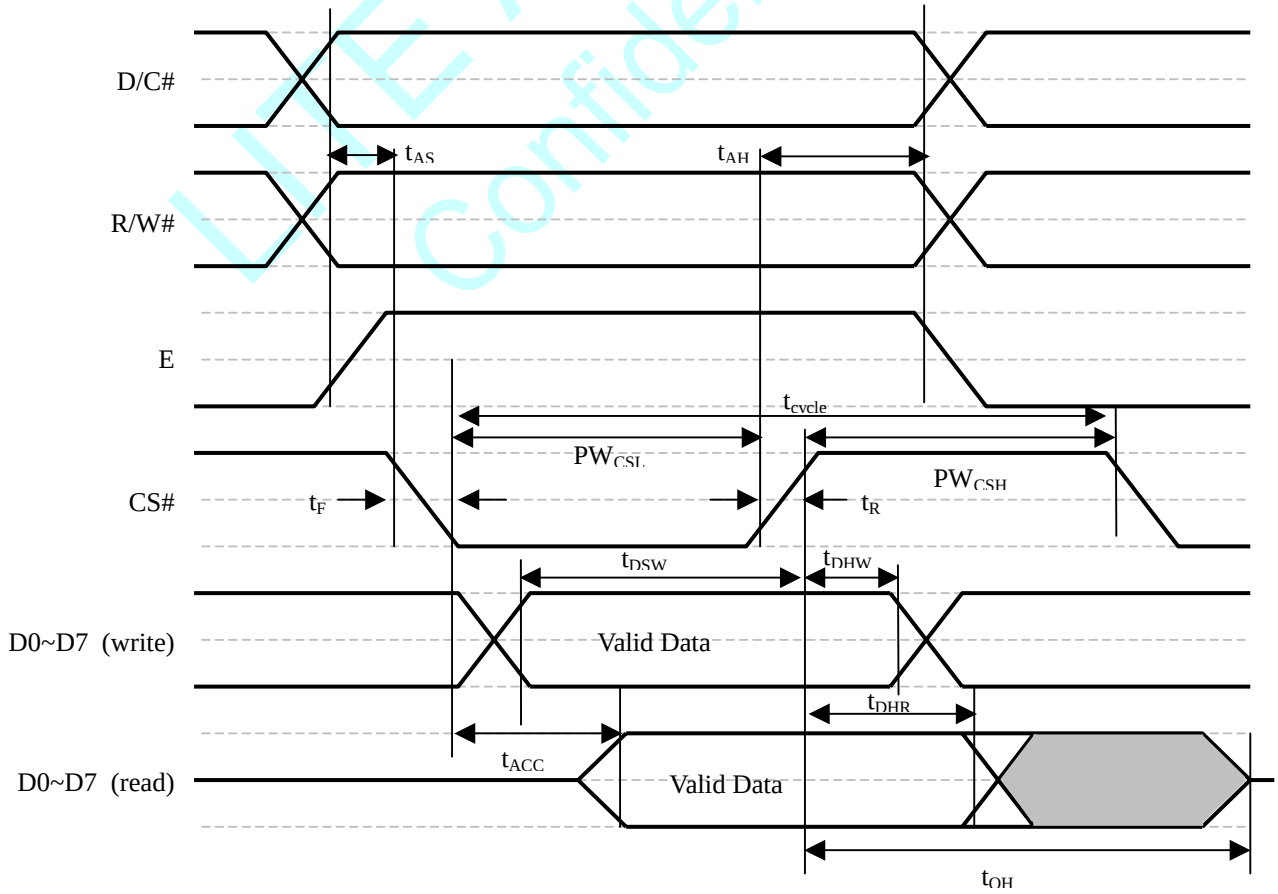


Figure 3: Timing diagram for 6800-series MPU parallel interface

8.2.2 8080-Series MPU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Max	Unit
t_{cycle}	Clock cycle time	300	--	ns
t_{AS}	Address Setup Time	0	--	ns
t_{AH}	Address Hold Time	0	--	ns
t_{DSW}	Write Data Setup Time	40	--	ns
t_{DHW}	Write Data Hold Time	15	--	ns
t_{DHR}	Read Data Hold Time	20	--	ns
t_{OH}	Output Disable Time	--	70	ns
t_{ACC}	Access Time	--	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-- --	ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-- --	ns ns
t_R	Rise time	--	15	ns
t_F	Fall time	--	15	ns

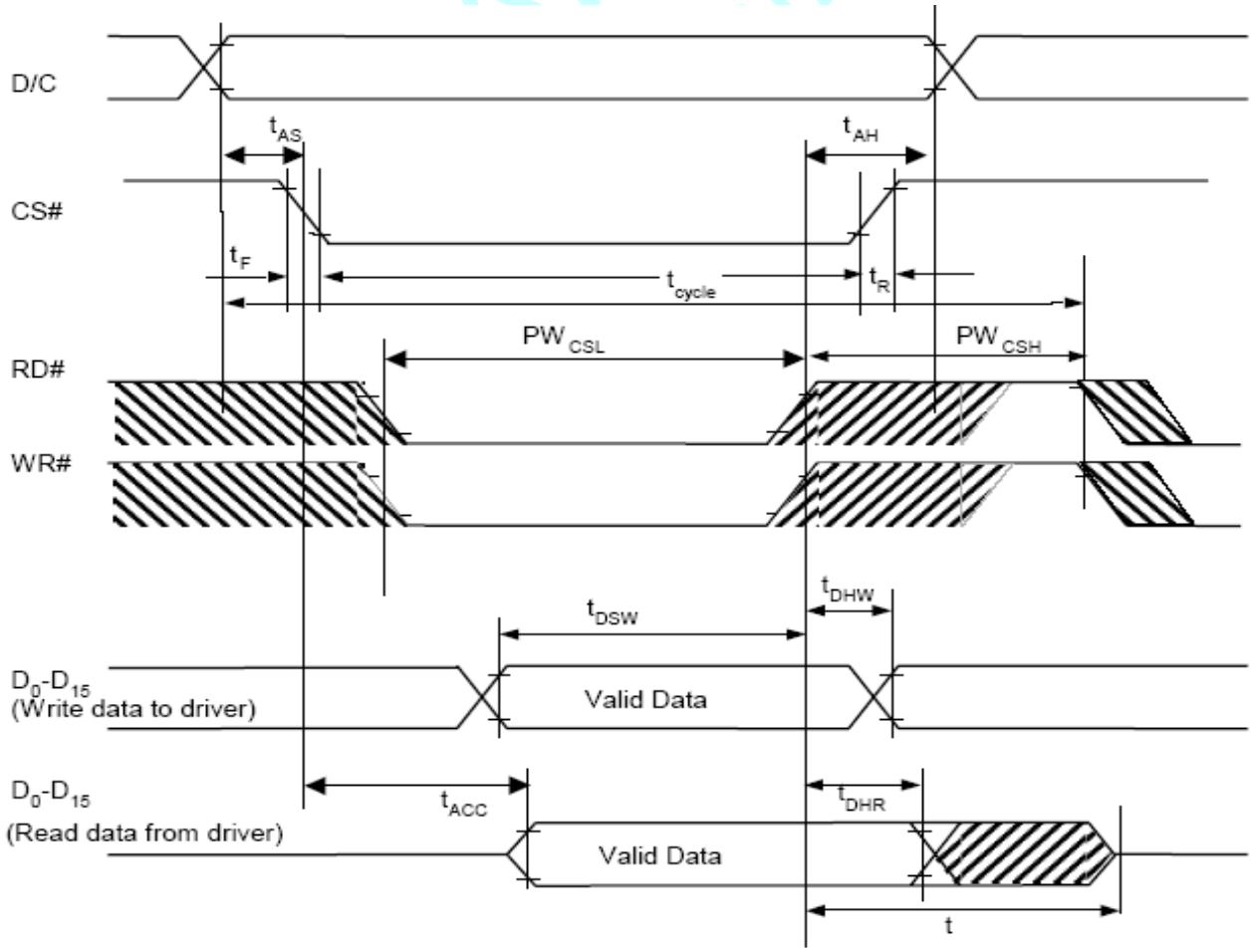


Figure4: Timing diagram for 8080-series MPU parallel interface

9. CONTROL AND DISPLAY COMMAND

9.1 Configuration Command Table

(To write commands to command registers, the MCU interface pins are set as: D/C = 0, R/W(WR#) = 0, E(RD#)=1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0	15 A[6:0] B[6:0]	0 * *	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	A[6:0] sets the column start address from 0-95, POR=00d. B[6:0] sets the column end address from 0-95 POR=95d.
0 0 0	75 A[5:0] B[5:0]	0 * *	1 * *	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	A[5:0] sets the row start address from 0-63, POR=00d. B[5:0] sets the row end address from 0-63, POR=63d.
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast for Color A (Segment Pins :SA0 – SA95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. POR = 80H
0 0	82 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Contrast for Color B (Segment Pins :SB0 – SB95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. POR = 80H
0 0	83 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Contrast for Color C (Segment Pins :SC0 – SC95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. POR = 80H
0 0	87 A[3:0]	1 *	0 *	0 *	0 *	0 A_3	1 A_2	1 A_1	1 A_0	Master Current Control	Set A[3:0] from 0000, 0001… to 1111 to adjust the master current attenuation factor from 1/16, 2/16… to 16/16. POR =1111b,for no attenuation.
0 0	A0 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Set Re-map & Data Format	A[0]=0, Horizontal address increment (POR) A[0]=1, Vertical address increment A[1]=0, Column address 0 is mapped to SEG0 (POR) A[1]=1, Column address 95 is mapped to SEG0 A[4]=0, Scan from COM 0 to COM [N –1] A[4]=1, Scan from COM [N-1] to COM0. Where N is the Multiplex ratio. A[5]=0, Disable COM Split Odd Even (POR) A[5]=1, Enable COM Split Odd Even A[7:6]=00; 256 color format =01; 65k color format(POR)
0 0	A1 A[5:0]	1 *	0 *	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display RAM display start line register from 0-63. Display start line register is reset to 00H after POR.
0 0	A2 A[5:0]	1 *	0 *	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by COM from 0-63. The value is reset to 00H after POR.
0	A4~A7	1	0	1	0	0	1	X_1	X_0	Set Display Mode	A4h=Normal Display (POR) A5h=Entire Display On, all pixels turn on at GS level 63 A6h=Entire Display Off, all pixels turn off A7h=Inverse Display
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-64MUX, POR=63d (64MUX) A[5:0]=0-14d (invalid entry)
0 0	AD A[7:0]	1 1	0 0	1 0	0 0	1 1	1 A_2	0 A_1	1 A_0	Set Master Configuration	A[0]=0, Select external VCC supply at Display ON A[0]=1, Select internal booster at Display ON (POR) A[1]=0, Select external VCOMH voltage supply at Display ON A[1]=1, Select internal VCOMH regulator at Display ON (POR) A[2]=0, Select External VP voltage supply A[2]=1, Select Internal VP (POR)
0	AE~AF	1	0	1	0	X_3	1	1	1	Set Display On/Off	AEh=Display off (POR) AFh=Display on

0 0	B0 A[7:0]	1 0	0 0	1 0	1 A_4	0 0	0 0	0 A_1	0 0	Set Power Save	A[7:0]=00 (POR) A[7:0]=12, power saving mode
0 0	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Phase 1 and 2 period adjustment	A[3:0] Phase 1 period in 1~16 DCLK clocks [POR=4h] A[7:4] Phase 2 period in 1~16 DCLK clocks [POR=7h]
0 0	B3 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Display Clock Divider/ Oscillator Frequency	A[3:0] [DIVIDER, POR=0] DCLK is generated from CLK divided by DIVIDER +1 (i.e., 1 to 16) A[7:4] Fosc frequency Frequency increases as level increases
0 0 0 0 0 0 0 0	B8 A[7:0]--PW1 B[7:0]--PW3 C[7:0]--PW5 : : : AE[7:0]--PW61 AF[7:0]--PW63	1 A_7 B_7 C_7 AE_7 AF_7	0 A_6 B_6 C_6 AE_6 AF_6	1 A_5 B_5 C_5 AE_5 AF_5	1 A_4 B_4 C_4 AE_4 AF_4	1 A_3 B_3 C_3 AE_3 AF_3	0 A_2 B_2 C_2 AE_2 AF_2	0 A_1 B_1 C_1 AE_1 AF_1	0 A_0 B_0 C_0 AE_0 AF_0	Set Gray Scale Table	The next 32 bytes of command set the current drive pulse width of gray scale level GS1, GS3, GS5 …GS63 as below: A[7:0]=PW1, POR=1, it equals 1 DCLK clock B[7:0]=PW3, POR=5, it equals 3 DCLK clocks C[7:0]=PW5, POR= 9 : : : AE[7:0]=PW61, POR=121 AF[7:0]=PW63, POR=125, it equals 125 DCLK clocks Note: GS0 has no pre-charge and current drive stages. For GS2 GS4…GS62, they are derived by driver itself with: PWn = (PWn-1+PWn+1)/2 Max pulse width is 125
0	B9	1	0	1	1	1	0	0	1	Enable Linear Gray Scale Table	Enable build-in linear gray scale table (POR=Enable) PW1=1,PW2=3,PW3=5 … PW61=121,PW62=123,PW63=125
0 0	BB ~ BD A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	1 A_3	X_2 A_2	X_1 A_1	X_0 A_0	VPA, VPB, VPC level setting for Color A,B,C	011b for Color A, 100b for Color B, 101b for Color C A[7:0] 00000000 0.43*Vref 00111111 0.83*Vref 01111111 1.0*Vref 1xxxxxxx connects to VCOMH (POR)
0 0	BE A[6:0]	1 *	0 A_6	1 A_5	1 A_4	1 A_3	1 A_2	1 A_1	0 A_0	Set VCOMH	A[6:0] 0000000 0.43*Vref 0111111 0.83*Vref (POR) 1111111 1.0*Vref
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

Table 6: Configuration Command

9.2 Graphic Acceleration Command Set Table

(To write commands to command registers, the MCU interface pins are set as: D/C = 0, R/W(WR#)=0, E(RD#)=1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	21	0	0	1	0	0	0	0	1		A[6:0] : Column Address of Start
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[5:0] : Row Address of Start
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		C[6:0] : Column Address of End
0	C[6:0]	*	C_6	C_5	C_4	C_3	C_2	C_1	C_0	Draw Line	D[5:0] : Row Address of End
0	D[5:0]	*	*	D_5	D_4	D_3	D_2	D_1	D_0		E[5:1] : Color C of the line
0	E[5:1]	*	*	E_5	E_4	E_3	E_2	E_1	*		F[5:0] : Color B of the line
0	F[5:0]	*	*	F_5	F_4	F_3	F_2	F_1	F_0		G[5:1] : Color A of the line
0	G[5:1]	*	*	G_5	G_4	G_3	G_2	G_1	*		
0	22	0	0	1	0	0	0	1	0		A[6:0] : Column Address of Start
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[5:0] : Row Address of Start
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		C[6:0] : Column Address of End
0	C[6:0]	*	C_6	C_5	C_4	C_3	C_2	C_1	C_0		D[5:0] : Row Address of End
0	D[5:0]	*	*	D_5	D_4	D_3	D_2	D_1	D_0		E[5:1] : Color C of the line
0	E[5:1]	*	*	E_5	E_4	E_3	E_2	E_1	*	Drawing Rectangle	F[5:0] : Color B of the line
0	F[5:0]	*	*	F_5	F_4	F_3	F_2	F_1	F_0		G[5:1] : Color A of the line
0	G[5:1]	*	*	G_5	G_4	G_3	G_2	G_1	*		H[5:1] : Color C of the fill area
0	H[5:1]	*	*	H_5	H_4	H_3	H_2	H_1	*		I[5:0] : Color B of the fill area
0	I[5:0]	*	*	I_5	I_4	I_3	I_2	I_1	I0		J[5:1] : Color A of the fill area
0	J[5:1]	*	*	J_5	J_4	J_3	J_2	J_1	*		
0	23	0	0	1	0	0	0	1	1		A[6:0] : Column Address of Start
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[5:0] : Row Address of Start
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		C[6:0] : Column Address of End
0	C[6:0]	*	C_6	C_5	C_4	C_3	C_2	C_1	C_0	Copy	D[5:0] : Row Address of End
0	D[5:0]	*	*	D_5	D_4	D_3	D_2	D_1	D_0		E[6:0] : Column Address of New Start
0	E[6:0]	*	E_6	E_5	E_4	E_3	E_2	E_1	E_0		F[5:0] : Row Address of New Start
0	F[5:0]	*	*	F_5	F_4	F_3	F_2	F_1	F_0		
0	24	0	0	1	0	0	1	0	0		A[6:0] : Column Address of Start
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[5:0] : Row Address of Start
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		C[6:0] : Column Address of End
0	C[6:0]	*	C_6	C_5	C_4	C_3	C_2	C_1	C_0		D[5:0] : Row Address of End
0	D[5:0]	*	*	D_5	D_4	D_3	D_2	D_1	D_0	Dim Window	The effect of dim window: GS15~GS0 no change GS19~GS16 become GS4 GS23~GS20 become GS5 ... GS63~GS60 become GS15
0	25	0	0	1	0	0	1	0	1		A[6:0] : Column Address of Start
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[5:0] : Row Address of Start
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0	Clear Window	C[6:0] : Column Address of End
0	C[6:0]	*	C_6	C_5	C_4	C_3	C_2	C_1	C_0		D[5:0] : Row Address of End
0	D[5:0]	*	*	D_5	D_4	D_3	D_2	D_1	D_0		
0	26	0	0	1	0	0	1	1	0		A0 0 : Disable Fill for Draw Rectangle Command (POR) 1 : Enable Fill for Draw Rectangle Command A[3:1] 000 : Reserved values A4 0 : Disable reverse copy (POR) 1 : Enable reverse during copy command.
0	A[4:0]	*	*	*	A_4	0	0	0	A_0	Fill Enable / Disable	

Table 7: Graphic Acceleration Command Set Table

9.3 Read Command Table

(D/C=0, R/W (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read *	D_7 : "1" for Command lock D_6 : "1" for display OFF / "0" for display ON D_5 : Reserve D_4 : Reserve D_3 : Reserve D_2 : Reserve D_1 : Reserve D_0 : Reserve

Table 8: Read Command Table

Note:
1.Remark "*" stands for "Don't Care"
2.Patterns other than that given in Command Table are prohibited to enter to the chip as a command; otherwise, unexpected result will occur.

10. REFERENCE APPLICATION CIRCUIT

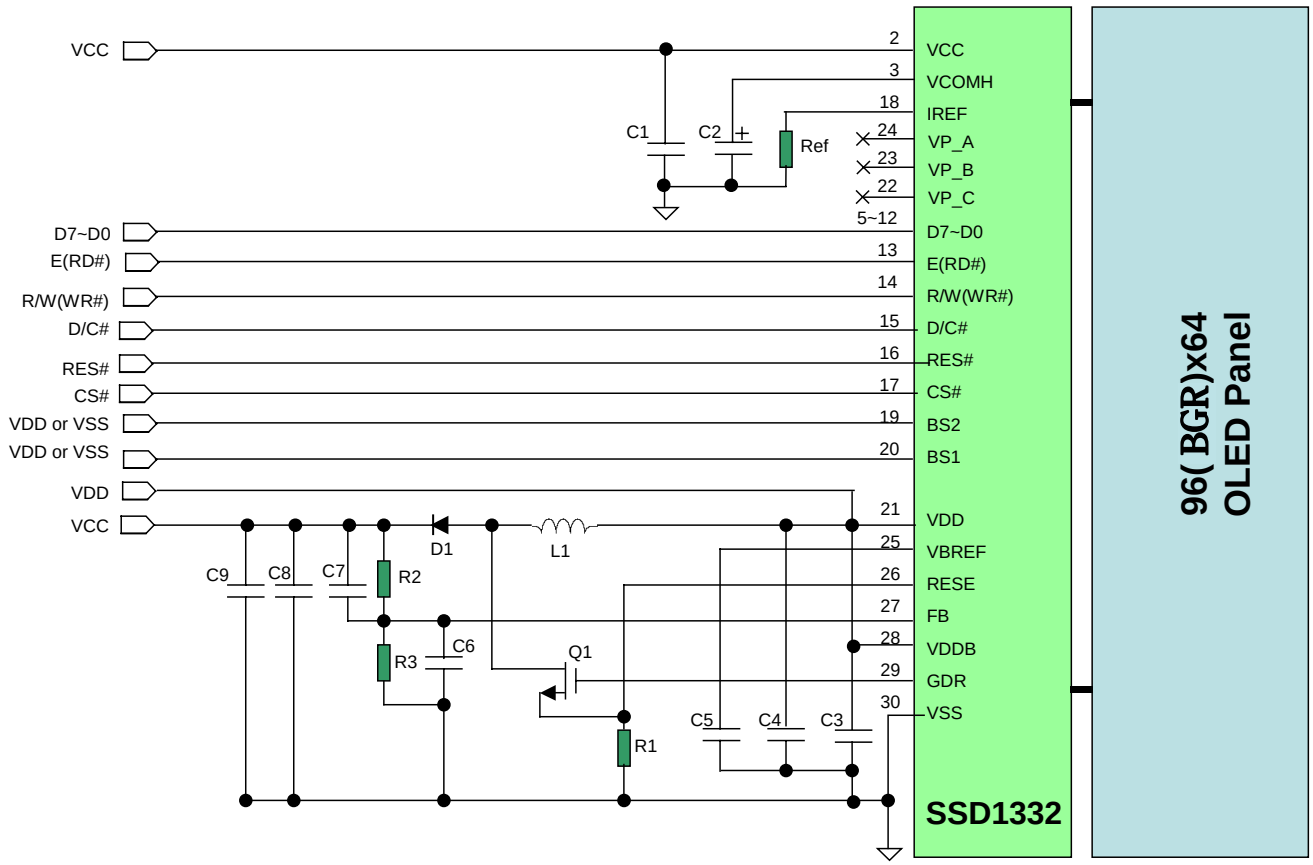


Figure 5: Reference Application Circuit (using internal DC/DC voltage converter)

Notes:

- MPU interface: 8-bit 6800-series/8080-series parallel interface. It is pin selectable by BS1 and BS2.

	6800-series parallel interface	8080-series parallel interface
BS1	0	1
BS2	1	1

- L1, D1, Q1 and C4 should be grouped closed together on PCB layout
- R2, R3, C5 and C6 should be grouped closed together on PCB layout
- The VCC output voltage level is adjusted by R2 and R3, the formula is:

  VCC = 1.2 x (R2+R3)/R3

  The value of (R2+R3) should be between 500k to 1M ohm.

Below table is the component list for the application circuit.

Item	Description
SSD1332	OLED Driver IC (*Solomon*)
Q1	MOSFET – N-FET with low R_{DS}(on) and low Vth voltage, eg, MGSF1N02Lt1 (*On Semi*)
L1	Inductor – 22µH, 2A
D1	Schottky diode – 2A, 25V, eg, 1N5822
Ref	Resistor – 1%, 1/2W (see remark)
R1	Resistor – 1.2Ω , 1%, 1/2W
R2, R3	Resistor – 1%, 1/10W
C1	Capacitor – 1µF~2.2µF, 16V
C2	Tantalum Capacitor – 1µF~2.2µF, 16V
C3	Capacitor – 0.1 ~ 1µF, 16V
C4	Capacitor – 1 ~ 10µF, 16V
C5	Capacitor – 1µF, 16V
C6	Capacitor – 10nF, 16V
C7	Capacitor – 15nF, 16V
C8	Capacitor – 22µF, 25V, Low ESR
C9	Capacitor – 1µF, 16V

Table 9: Component list for the internal DC-DC voltage converter application

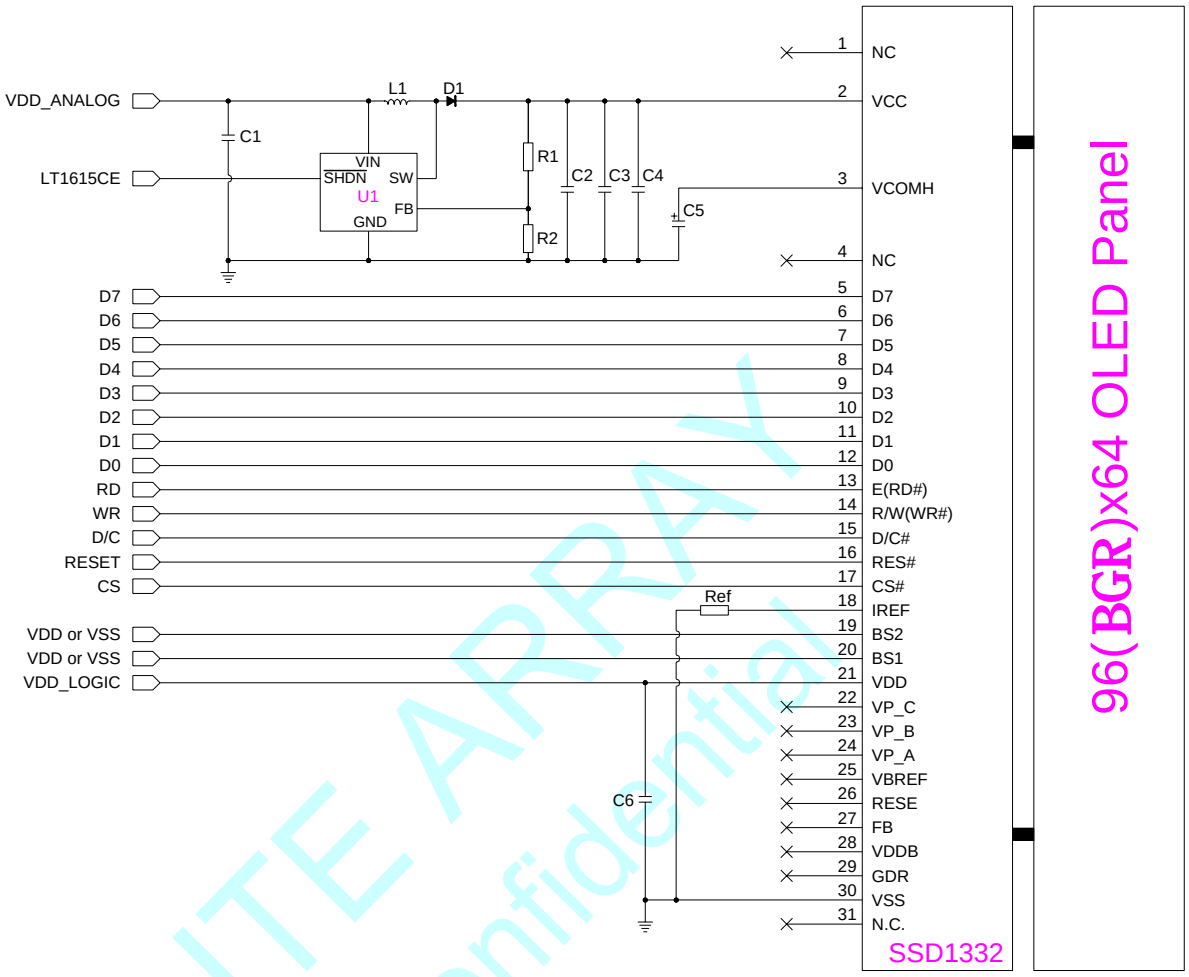


Figure 6: Reference Application Circuit (using external DC/DC voltage converter)

Notes:

- MPU interface: 8-bit 6800-series/8080-series parallel interface. It is pin selectable by BS1 and BS2.

	6800-series parallel interface	8080-series parallel interface
BS1	0	1
BS2	1	1

- U1: LT1615 DC/DC Converter
- LT1615CE can be connected to MCU or VDD for alternative solution.
- VCC = 1.23 x (R1 + R2)/R2

Below table is the component list for the application circuit.

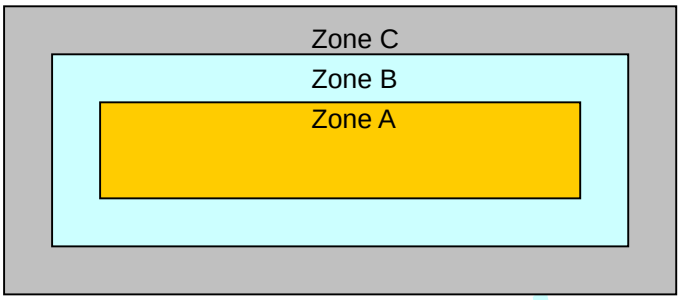
Item	Description
SSD1332	OLED Driver IC (*Solomon*)
U1	DC/DC Converter – LT1615 Step-up(*Linear*)
L1	Inductor – 10µH, 2A
D1	Schottky Diode – 20V, 1A, eg. MBRS120T3
R1	Resistor – 1MΩ , 1%, 1/4W
R2	Resistor – 150kΩ , 1%, 1/4W
Ref	Resistor – 910kΩ, 1% (see remark)
C1,C6	Capacitor – 4.7µF, 6.3V, Low ESR
C2,C3	Capacitor – 4.7µF, 16V, Low ESR
C4	Capacitor – 0.1µF, 16V, Low ESR
C5	Tantalum Capacitor – 1µF ~2.2µF, 16V, Low ESR

Table 10: Component list for the external DC-DC voltage converter application circuit

Remark:
Ref = (Voltage at IREF pin – VSS)/I_{REF}; Voltage at I_{REF} pin = VCC - VDD
For example, VDD = 3.0V, VCC = 12V, I_{REF} = 10µA
Ref = (12-3)/10^{-6} = about 910kΩ

11. QUALITY SPECIFICATIONS

11.1 Quality guaranty of Zone

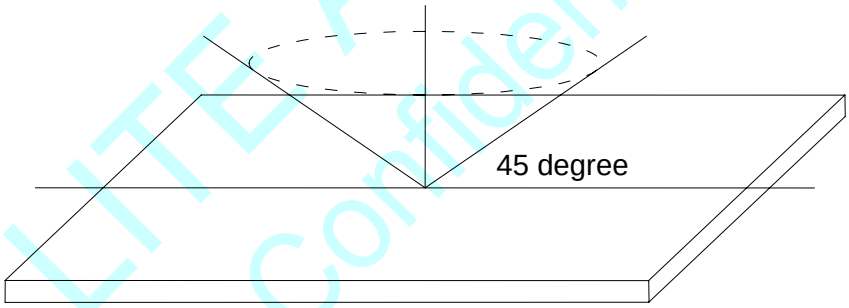


Zone A: Active Area
Zone B: Viewing Area
Zone C: Appearance or other module organization of Zone B

11.2 Inspection Condition

Temperature: 20±15℃
Humidity: 60±20%RH
Pressure: 860~1060hPa

Functional and Appearance tests shall be performed when the module is turned ON and OFF respectively, allowing a distance of 30cm or more. The viewing angle for a visual check shall not exceed 45 degrees from the vertical in each direction: forward, backward, right and left (See the sketch below). A sample shall be subject to visual observations under the fluorescent lamp of 40watts.



11.3 AQL

Major 0.65; Minor 1.0

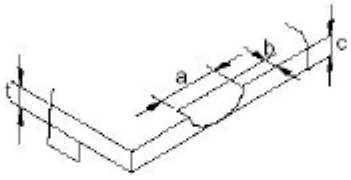
***Major defect**
A major defect refers to the defect, which is considered to substantial degradation to the usability for product application.

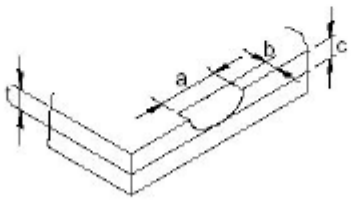
***Minor defect**
A minor defect refers to the defect, which is not considered to be substantial degradation for product application, or the defect, which deviate from the existing standards, and it is almost unrelated to the effective use of the product or its operation.

11.4 Electrical Characteristics

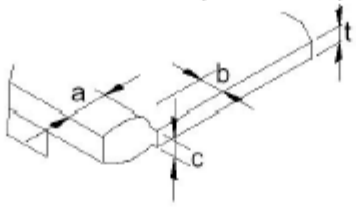
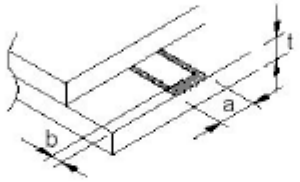
No	Item	Criterion	AQL
1	Non operational	No-Go	Major
2	Luminance	According to specification	Major
3	CIE coordinates	According to specification	Major
4	Contrast irregularity	Non detectable by the eye	Major
5	Power consumption	According to specification	Major

11.5 Appearance Defect

<table>
<tr><th>No</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>1</td><td>Outer dimensions</td><td>According to drawing</td><td>Minor</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">Black spots, foreign matter, white spots and scratches</td><td>1.
<table>
<tr><th>Average diameter(mm)：D</th><th>Number of pieces permitted</th></tr>
<tr><td>D＜0.1</td><td>Ignore</td></tr>
<tr><td>0.1＜D＜0.2</td><td>5</td></tr>
<tr><td>0.2＜D＜0.3</td><td>2</td></tr>
<tr><td>0.3＜D</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
Number of total pieces is set to within 5 pieces
Set as：average diameter
D=(long diameter + short diameter)/2</td><td rowspan="2">Minor</td></tr>
<tr><td>2.
<table>
<tr><th>Width(mm) W</th><th>Length(mm) L</th><th>Number of pieces permitted</th></tr>
<tr><td>W＜0.03</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.03＜W＜0.08</td><td>L＜3</td><td>6</td></tr>
<tr><td>0.08＜W</td><td>-----</td><td>None</td></tr>
<tr><td>beyond A.A.</td><td>-----</td><td>Ignore</td></tr>
</table></td></tr>
<tr><td>3</td><td>Cracks</td><td>1. General crack (unit：mm)




a=NC, b≦1, c=NC
It is not permitted to break runner</td><td>Minor</td></tr>
</table>

		2. Corner crack (unit：mm)  (1)Pad a≦1, b≦1, c=NC (2)Except for pad a≦1.5, b≦1.5, c=NC No conductive wire exposure is permitted	Minor
		3. Pin crack  a=NC, b≦0.5	Minor
		4. Future crack  Any possible future crack is not permitted	Minor
4	Pattern check (turn on)	Display normally	Major

<table>
<tr>
<td>5</td>
<td>Polarizer</td>
<td>1. Bubble
<table>
<tr><th>Average diameter (mm) : D</th><th>Number of pieces permitted</th></tr>
<tr><td>D < 0.2</td><td>Ignore</td></tr>
<tr><td>0.2 < D < 0.5</td><td>2</td></tr>
<tr><td>0.5 < D</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
2. Scratch
<table>
<tr><th>Average diameter (mm) : D</th><th>Number of pieces permitted</th></tr>
<tr><td>D < 0.2</td><td>Ignore</td></tr>
<tr><td>0.2 < D < 0.3</td><td>2</td></tr>
<tr><td>0.3 < D</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
<table>
<tr><th>Width(mm) W</th><th>Length(mm) L</th><th>Number of pieces permitted</th></tr>
<tr><td>W < 0.03</td><td>-----</td><td>Ignore</td></tr>
<tr><td>0.03 < W < 0.08</td><td>L < 4</td><td>4</td></tr>
<tr><td>beyond A.A.</td><td>-----</td><td>Ignore</td></tr>
</table>
</td>
<td>Minor</td>
</tr>
</table>

11.5 Reliability test condition

Operating life time (30% ON, 50cd/ m_2): Longer than 10,000 hours
Reliability characteristics shall meet following requirements

No.	ITEM	CONDITION	TEST TIME	Notes
1	High Humidity Storage	60℃,90%RH	120 Hrs	5
2	High Humidity Operation	50℃,90%RH	96 Hrs	
3	High Temperature Storage	60℃	120 Hrs	
4	High Temperature Operation	70℃	70 Hrs	
6	Low Temperature Operation	-20℃	70Hrs	
7	Thermal shock	-40℃(30min) →25℃(5min) → 85℃(30min) → 25℃(5min) 20 Cycles		5

Note 1: Unless otherwise specified, tests will be not conducted under functioning state.
Note 2: It should be checked at the actual driving condition under the high temperature.
Note 3: No dew condensation to be observed.
Note 4: The function test shall be conducted after 4 hours storage at the normal temperature and humidity after removed from the test chamber.

Note 5: The function test is OK.

Note 6: No addition to the defect.

Luminance: >50% of initial value.