Title	***Reference Design Report for a 5 W Charger Using LNK616PG***
Specification	85-265 VAC Input; 5 V, 1 A Output
Application	Low-cost Charger or Adapter
Author	Applications Engineering Department
Document Number	RDR-158
Date	November 25, 2008
Revision	1.1

Summary and Features

- Revolutionary control concept provides very low cost, low part-count solution
  - Primary-side control eliminates secondary-side control and optocoupler
  - Provides ±5% constant voltage (CV) and ±10% constant current (CC) accuracy including output cable drop compensation for 26 AWG (0.49 Ω) or 24 AWG (0.3 Ω) cables
  - Over-temperature protection – tight tolerance (±5%) with hysteretic recovery for safe PCB temperatures under all conditions
  - Auto-restart output short circuit and open-loop protection
  - Extended pin creepage distance for reliable operation in humid environments – >3.2 mm at package
- EcoSmart® – Easily meets all current international energy efficiency standards – China (CECP) / CEC / ENERGY STAR 2 / EU CoC
  - No-load consumption <50 mW at 230 VAC
  - Ultra-low leakage current: <5 µA at 265 VAC input (no Y capacitor required)
  - Design easily passes EN550022 and CISPR-22 Class B EMI testing with >10 dB margin
- Meets IEC 61000-4-5 Class 3 AC line surge
- Meets IEC 61000-4-2 ESD withstand (contact and air discharge to ±15 kV)

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a 5 W constant voltage/constant current (CV/CC) universal-input power supply for cell phone or similar charger applications. This reference design is based on the LinkSwitch-II family product LNK616PG.

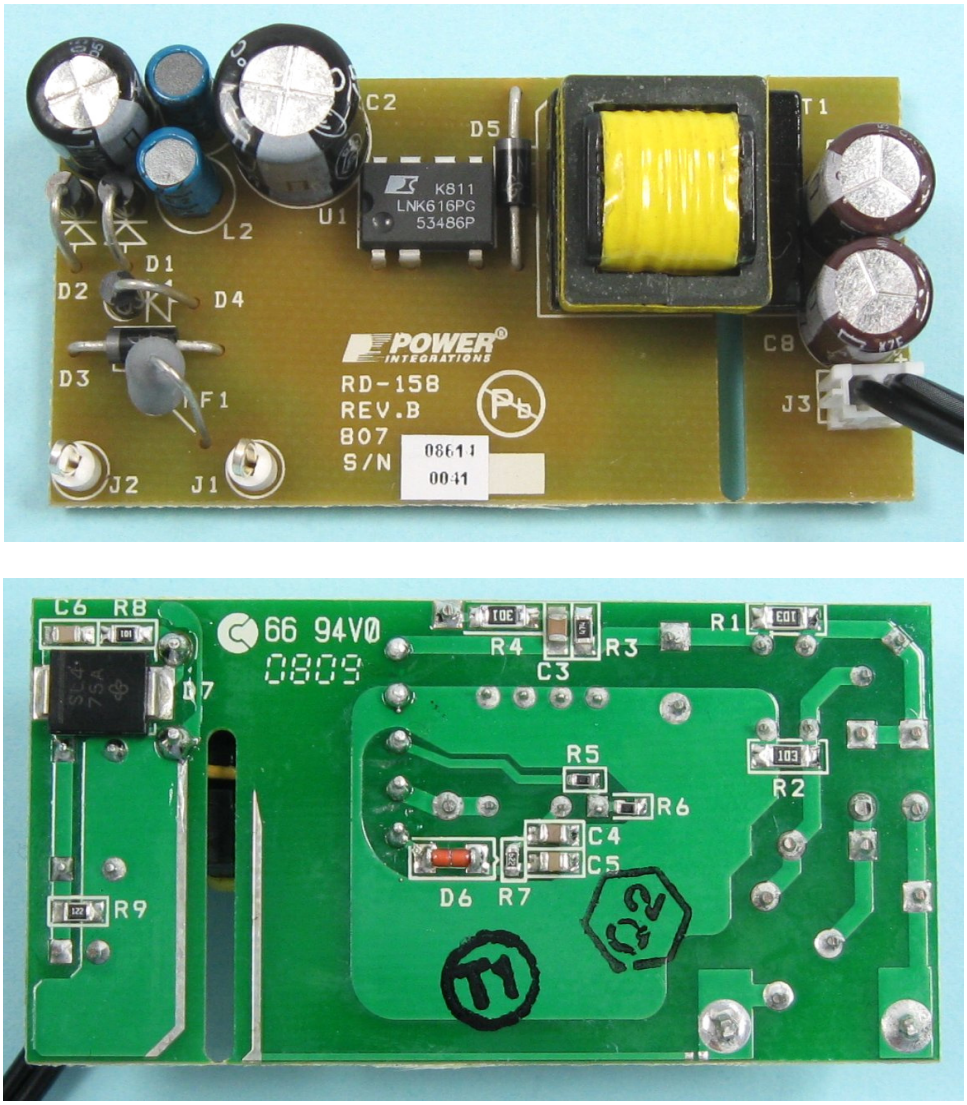

Figure 1 – RD-158 Board Photograph (top and bottom views).

The LNK616PG was developed to cost effectively replace all existing solutions in low-power charger and adapter applications. Its core controller is optimized for CV/CC charging applications with minimal external parts count and very tight control of both the output voltage and current, without the use of an optocoupler. The LNK616PG has an integrated 700 V switching MOSFET and ON/OFF control function which together deliver high efficiency under all load conditions and low no-load energy consumption. Both the operating efficiency and no-load performance exceed all current international energy efficiency standards.

The LNK616PG monolithically integrates the 700 V power MOSFET switch and controller. A unique ON/OFF control scheme provides CV regulation. The IC also incorporates both output cable voltage-drop compensation and tight regulation over a wide temperature range for enhanced CV control. The switching frequency is modulated to regulate the output current for a linear CC characteristic.

The LNK616PG controller consists of an oscillator, a feedback (sense and logic) circuit, a 5.8 V regulator, BYPASS pin programming functions, over-temperature protection, frequency jittering, a current-limit circuit, leading-edge blanking, a frequency controller for CC regulation, and an ON/OFF state machine for CV control.

The LNK616PG also provides a sophisticated range of protection features including auto-restart for control loop component open/short circuit faults and output short circuit conditions. Accurate hysteretic thermal shutdown ensures safe average PCB temperatures under all conditions.

The IC package provides extended creepage distance between high and low voltage pins (both at the package and PCB), which is required in highly humid environments to prevent arcing and to further improve reliability.

The LNK616PG can be configured to either be self-biased from the high-voltage DRAIN pin, or to receive an optional external bias supply. When configured to be self-biased, the very low IC current consumption ensures a worst-case no-load power consumption of less than 175 mW at 265 VAC, well within the 300 mW European Union CoC limit. When fed from an optional bias supply (as in this design), the no-load power consumption reduces to <50 mW.

The EE16 transformer bobbin in this design provides extended creepage to meet safety spacing requirements.

This document contains the power supply specifications, schematic, bill of materials, transformer specifications, and typical performance characteristics for this reference design.

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power	P_{NL}			50	mW	Measured at V_{IN} = 230 VAC
Output						All measured at end of cable
Output Voltage	V_{OUT}	4.75	5.00	5.25	V	±5%
Output Ripple Voltage	V_{RIPPLE}		150		mV	20 MHz bandwidth
Output Current	I_{OUT}	900	1000	1100	mA	±10%
Output Cable Resistance	R_{CBL}		0.3		Ω	6 ft, 24 AWG
Output Power	P_{OUT}		5		W	
Name plate output rating						
Name plate Voltage	V_{NP}		5		V	
Nameplate Current	I_{NP}		900		mA	
Nameplate Power	P_{NP}		4.5		W	
Efficiency						
Average Active Mode	η		74		%	115 VAC / 230 VAC, 25 °C
Required average efficiency per Energy Star EPS v1.1 / CEC 2008	$\eta_{ESV1.1}$	64	Measured per Energy Star "Test Method for Calculating the Energy Efficiency of Single-Voltage External AC-DC and AC-AC Power Supplies (August 11, 2004)".			
Required average efficiency per Energy Star EPS v2 April, 2008	η_{ESV2}	67	η_{ESV1}:(0.09 ln(P_{NP})+0.5 η_{ESV2}:(0.075 ln(P_{NP})+0.561			
Environmental						
Conducted EMI	Meets CISPR22B / EN55022B					>10 dB margin
Safety	Designed to meet IEC950, UL1950 Class II					
Line Surge Differential Common Mode		 1 2			 kV kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
ESD		-15		15	kV	Contact and air discharge to IEC 61000-4-2
Ambient Temperature	T_{AMB}	0		40	°C	Case external, free convection, sea level

3 Schematic

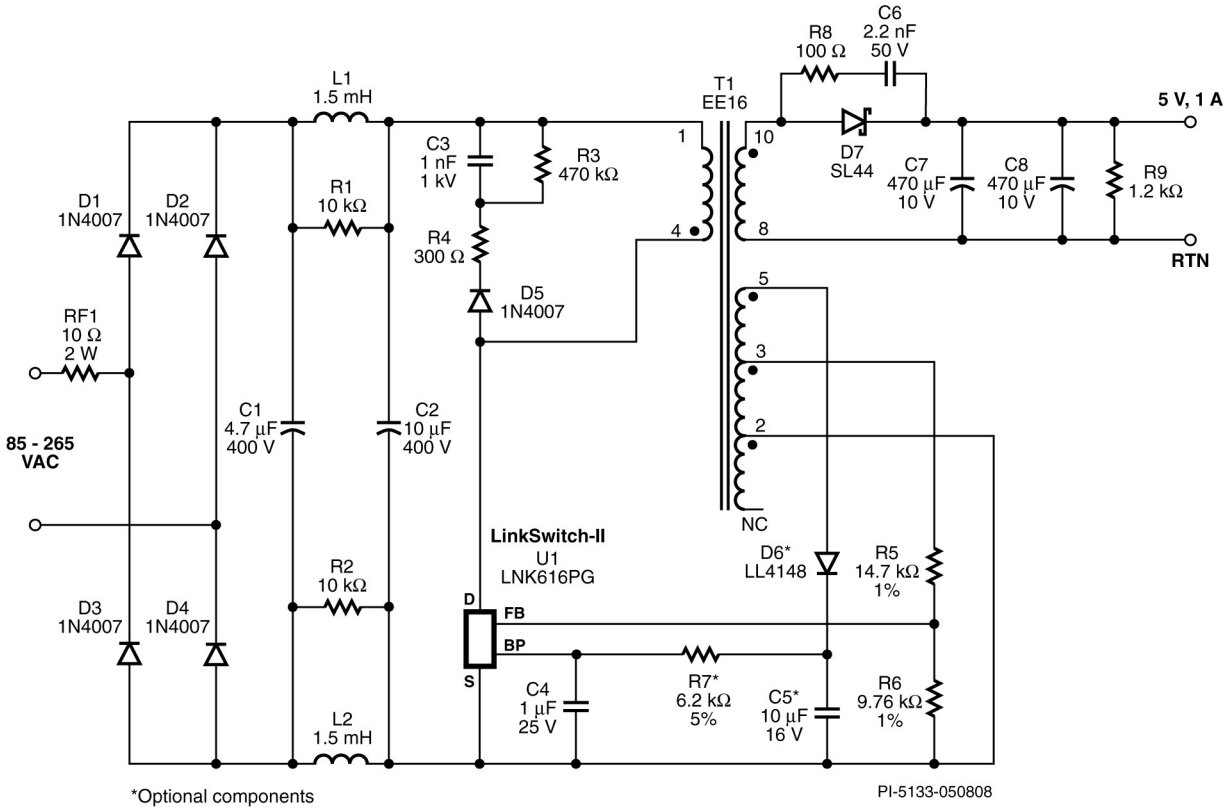

Figure 2 – RD158 Circuit Schematic.

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4 Circuit Description

This circuit uses the LNK616PG in a primary-side regulated flyback power-supply configuration.

4.1 Input Filter

The AC input power is rectified by diodes D1 through D4. The rectified DC is filtered by the bulk storage capacitors C1 and C2. Inductors L1 and L2, with capacitors C1 and C2, form pi (π) filters to attenuate conducted differential-mode EMI noise. This configuration, along with Power Integrations' transformer E-shield™ technology, allows this design to meet EMI standard EN55022 class B with good margin and without a Y capacitor. The transformer construction also gives very good EMI repeatability. Fusible resistor RF1 provides protection against catastrophic failure. It should be rated to withstand the instantaneous dissipation when the supply is first connected to the AC input (while the input capacitors charge) at VAC_{MAX}. This means choosing either an over-sized metal-film or a wire-wound type. This design uses a wire-wound resistor for RF1.

4.2 LNK616PG Primary

The LNK616PG device (U1) incorporates the power switching device, oscillator, CV/CC control engine, and startup and protection functions all on one IC. Its integrated 700 V MOSFET allows sufficient voltage margins in universal input AC applications, including extended line swells. The device is self-powered from the BYPASS pin via the decoupling capacitor C4. The value of C4 also programs the cable-drop voltage compensation. In this case, a 1 µF capacitor gives the 350 mV (7% of V_{NO}) compensation needed for the nominal 24-AWG cable, with 0.3 Ω impedance, used in this design. The optional bias circuit consisting of D6, C5, and R7 increases efficiency and reduces no-load input power.

The rectified and filtered input voltage is applied to one end of the transformer (T1) primary winding. The other side of the transformer's primary winding is driven by the internal MOSFET of U1. An RCD-R clamp consisting of D5, R3, R4, and C3 limits drain-voltage spikes caused by leakage inductance. Resistor R4 has a relatively large value to prevent any excessive ringing on the drain voltage waveform caused by the leakage inductance. Excessive ringing can increase output ripple by introducing an error in the sampled output voltage. IC U1 samples the feedback winding each cycle, 2.5 µs after turn-off of its internal MOSFET.

4.3 Output Rectification and Filtering

Transformer T1's secondary is rectified by D7, a Schottky barrier-type diode (chosen for higher efficiency), and filtered by C7 and C8. In this application, C7 and C8 have sufficiently low ESR characteristics to allow meeting the output voltage ripple requirement without adding an LC post filter. Resistor R8 and capacitor C6 dampen high-frequency ringing and reduce the voltage stress on D7.

In designs where lower average efficiency is acceptable (by 3% to 4%) D7 may be replaced by a PN-junction to lower cost. In this case, ensure R5 and R6 are re-adjusted as necessary to keep the output voltage centered.

4.4 Output Regulation

The LNK616PG regulates output using ON/OFF control for CV regulation, and frequency control for CC regulation. The output voltage is sensed by a bias winding on the transformer. The feedback resistors (R5 and R6) were selected using standard 1% resistor values to center both the nominal output voltage and constant current regulation thresholds. Resistor R9 provides a minimum load to maintain output regulation when the output is unloaded.

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5 PCB Layout

Notable layout design points are:

1 A spark gap and associated slot in the PCB between the primary and secondary allows successful ESD testing up to ±15 kV.
   - The preferential arcing point routes the energy from ESD discharges back to the AC input, away from the transformer and primary circuitry.
   - The trace connected to the AC input side of the spark gap is spaced away from the rest of the board and its components to prevent arc discharges to other sections of the circuit.

2 The drain trace length has been minimized to reduce EMI.

3 Clamp and output diode loop areas are minimized to reduce EMI.

4 The AC input is located away from switching nodes to minimize noise coupling that may bypass input filtering.

5 Place C4 (the bypass capacitor) as close as possible to the BYPASS pin on U1.

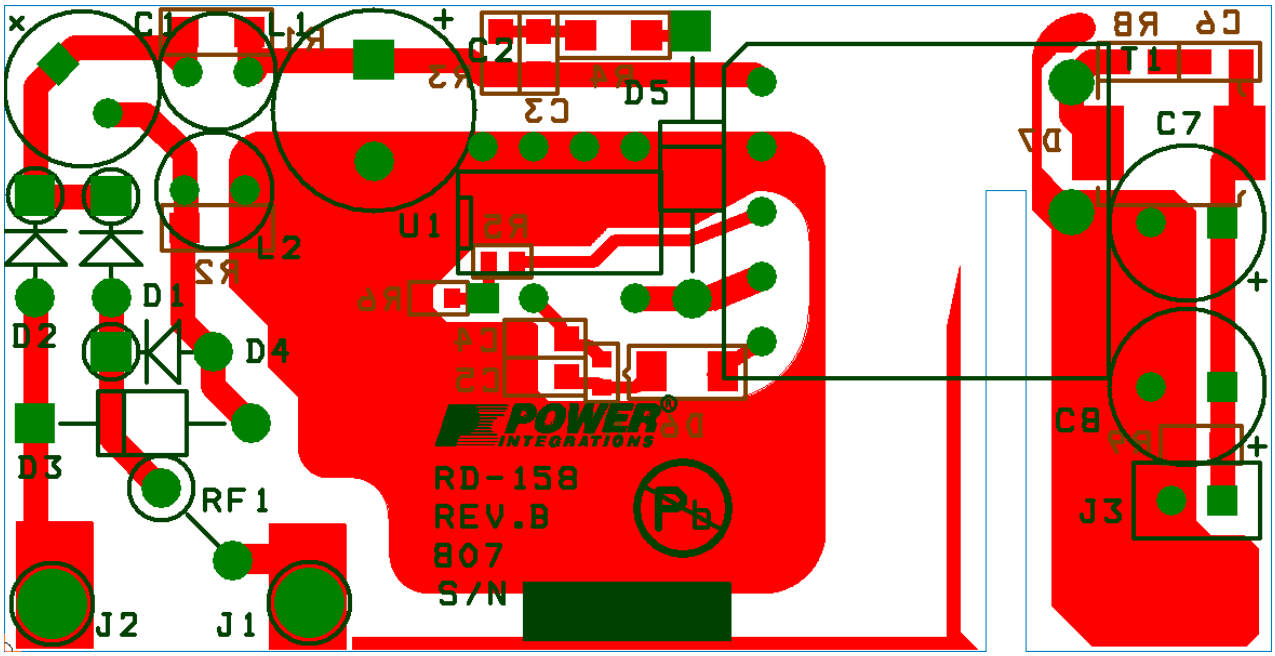

Figure 3 – Printed Circuit Layout.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg	Mfg Part Number
1	1	C1	4.7 µF, 400 V, Electrolytic, (8 x 11.5)	Taicon Corporation	TAQ2G4R7MK0811MLL3
2	1	C2	10 µF, 400 V, Electrolytic, Low ESR, 79 mA, (10 x 12.5)	Ltec	TYD2GM100G13O
3	1	C3	1 nF, 1000 V, Ceramic, X7R, 0805	Kemet	C0805C102KDRACTU
4	1	C4	1 µF, 25 V, Ceramic, X7R, 0805	Panasonic	ECJ-2FB1E105K
5	1	C5	10 µF, 16 V, Ceramic, X5R, 0805	Murata	GRM21BR61C106KE15L
6	1	C6	2.2 nF, 50 V, Ceramic, X7R, 0805	Panasonic	ECJ-2VB1H222K
7	2	C7 C8	470 µF, 10 V, Electrolytic, Very Low ESR, 72 mOhm, (8 x 11.5)	Nippon Chemi-Con	EKZE100ELL471MHB5D
8	5	D1 D2 D3 D4 D5	1000 V, 1 A, Rectifier, DO-41	Vishay	1N4007-E3/54
9	1	D6	75 V, 0.15 A, Fast Switching, 4 ns, MELF	Diode Inc.	LL4148-13
10	1	D7	40 V, 4 A, Schottky, SMD, DO-214AB	Vishay	SL44-E3/57T
11	2	J1 J2	Test Point, WHT,THRU-HOLE MOUNT	Keystone	5012
12	1	J3	6 ft, 24 AWG, 2.1 mm connector (custom)	CUI Inc	CA-2184
13	2	L1 L2	1.5 mH, 0.18 A, 5.5 x 10.5 mm	Tokin	SBC1-152-181
14	2	R1 R2	10 kΩ, 5%, 1/4 W, Metal Film, 1206	Panasonic	ERJ-8GEYJ103V
15	1	R3	470 kΩ, 5%, 1/8 W, Metal Film, 0805	Panasonic	ERJ-6GEYJ474V
16	1	R4	300 Ω, 5%, 1/4 W, Metal Film, 1206	Panasonic	ERJ-8GEYJ301V
17	1	R5	14.7 kΩ, 1%, 1/16 W, Metal Film, 0603	Panasonic	ERJ-3EKF1472V
18	1	R6	9.76 kΩ, 1%, 1/16 W, Metal Film, 0603	Panasonic	ERJ-3EKF9761V
19	1	R7	6.2 kΩ, 5%, 1/10 W, Metal Film, 0603	Panasonic	ERJ-3GEYJ622V
20	1	R8	100 Ω, 5%, 1/8 W, Metal Film, 0805	Panasonic	ERJ-6GEYJ101V
21	1	R9	1.2 kΩ, 5%, 1/8 W, Metal Film, 0805	Panasonic	ERJ-6GEYJ122V
22	1	RF1	10 Ω, 2 W, Fusible/Flame Proof Wire Wound	Vitrohm	CRF253-4 10R
23	1	T1	Custom Transformer, EE16, 10pins; per Power Integrations' RD-158 Transformer Specification	Santronics Ice Components Precision, Inc	SNXR1346 TP07161 019-6120-00R
24	1	U1	LinkSwitch-II, LNK616PG, CV/CC, DIP-8C	Power Integrations	LNK616PG
25	1	J3	Plastic housing for cable assembly	JST Sales America Inc.	HER-2

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7 Transformer Specification

7.1 Electrical Diagram

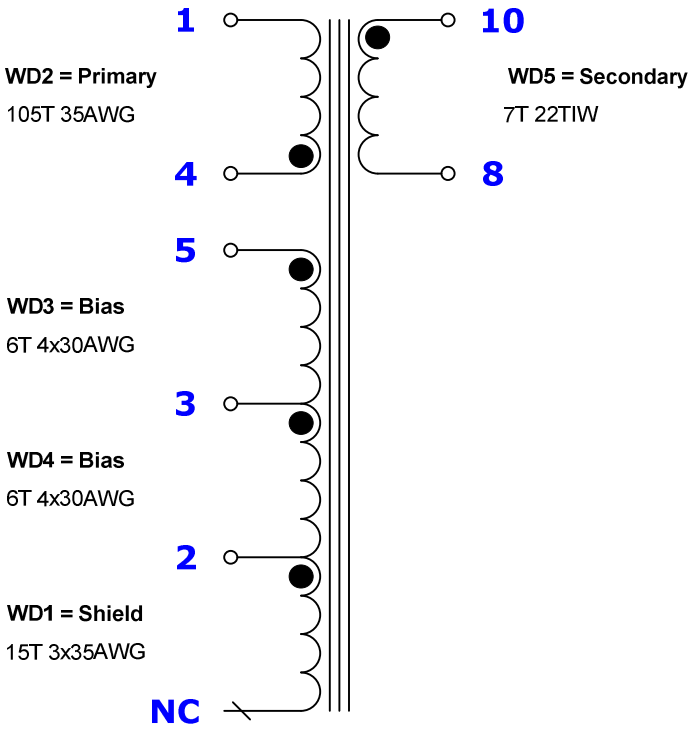

Figure 4 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	60 seconds, 60 Hz, from Pins 1-5 to Pins 6-10	3000 VAC
Primary Inductance	Pins 1-4, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	1.074 mH, ±10%
Resonant Frequency	Pins 1-4, all other windings open	1000 kHz (min)
Primary Leakage Inductance	Pins 1-4, with Pins 8-10 shorted, measured at 100 kHz, 0.4 V_{RMS}	95 µH (max)

7.3 Materials

Item	Description
[1]	Core: EE16, NC-2H or equivalent, gapped for ALG of 88.55 nH/T^2
[2]	Bobbin: EE16, Horizontal, 10 pins, (5/5). See attached drawing
[3]	Magnet Wire: #35 AWG, for the Shield and the Primary Winding
[4]	Magnet Wire: #30 AWG, for the Bias Winding
[5]	Triple Insulated Wire: #22 AWG, for the Secondary Winding
[6]	Margin tape: 1.0 mm wide
[7]	Tape: 3M 1298 Polyester film, 2.0 mils thick, 8.0 mm wide
[8]	Tape: 3M Polyester film, 2.0 mils thick, 7.0 mm wide
[9]	Varnish

7.4 Transformer Build Diagram

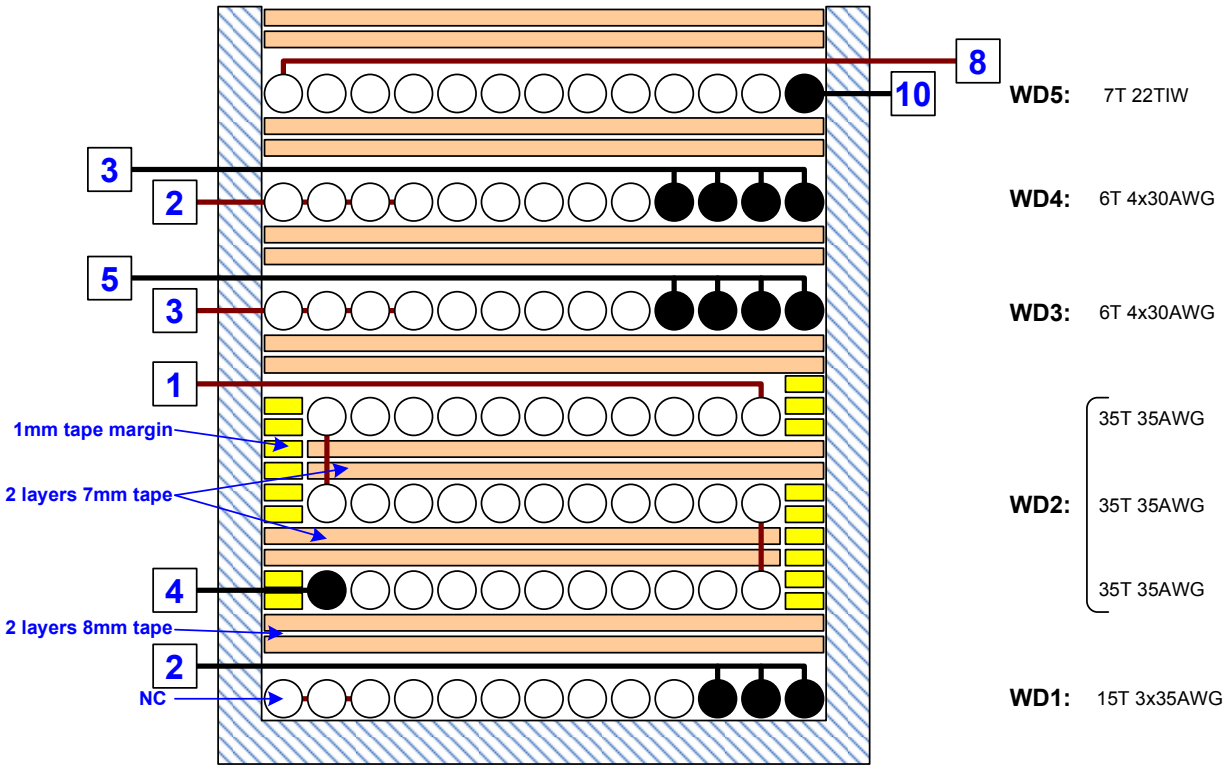

Figure 5 – Transformer Build Diagram.

The highlighted 1 mm tape margin (in yellow above) was added to improve consistency in EMI performance in production. The spacing of the first two layers of the primary winding improves the effect of the subsequent shield windings and makes the transformer design less sensitive to winding variations. However, if the transformer can be manufactured consistently to comply with EMI performance specifications without the extra margin tape, omit the margin tape to reduce transformer cost and increase the wire gauge of the primary winding so that each layer fills the bobbin window width in 35 turns.

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7.5 Transformer Construction

Bobbin Preparation	Primary side of the bobbin is placed on the left hand side, and secondary side of the bobbin is placed on the right hand side.
WD1 Shield	Temporarily hang the start end of the wires of item [3] on pin 7, wind 15 tri-filar turns from right to left with tight tension and evenly. The maximum allowed gap between the winding and the left and right lateral walls of the bobbin must be less than 0.5 mm (20 mils). Cut the end of the wire and bring the start end of the wire across the bobbin to the left to terminate at pin 2.
Insulation	2 layers of tape item [7].
WD2 Primary	Apply 1 mm margin tape on both side of bobbin to match the height of one layer of primary winding on the left side, and two layers of primary winding on the right side. Start at pin 4, wind 35 turns of item [3] from left to right with tight tension, and apply 2 layers tape item [8] and 1 mm margin tape to match another two layers of primary on the left side. Continue winding 35 turns of item [3] from right to left, repeat 2 layers tape item [8] and 1 mm margin tape on the left side, continue wind another 35 turns of item [3] from left to right, at the last turn bring the wire back to the left to terminate at pin 1.
Insulation	2 layers of tape item [7].
WD3 1st half Bias	Temporarily hang the start end of the wires on pin 6, wind 6 quad-filar turns of item [4] from right to left uniformly, terminate the end of the wires at pin 3, bring the start end of the wires across the bobbin to the left side to terminate at pin 5.
Insulation	2 layers of tape item [7].
WD4 2nd half Bias	Temporarily hang the start end of the wires of item [4] on pin 6, wind 6 quad-filar turns of item [4] from right to left uniformly, terminate the end of the wires at pin 2, bring the start end of the wires across the bobbin to the left side to terminate at pin 3.
Insulation	2 layers of tape item [7].
WD5 Secondary	Start pin 10, wind 7 turns of item [5] from right to left uniformly, at the last turn bring the wire across the bobbin to the right side to terminate at pin 8. Cut three pins from the secondary side: 6, 7, and 9.
Insulation	2 layers of tape item [7].
Finish	Grind the core to get 1.074mH. Secure the core with tape. Dip vanish [9].

Note:

1. **Tape between adjacent primary winding layers reduces primary capacitance and losses.**

8 Design Spreadsheet

RD-158 Power Integrations	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-II_040108_Rev1-0.xls; LinkSwitch-II Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			V	Minimum AC Input Voltage
VACMAX	265			V	Maximum AC Input Voltage
fL	50			Hz	AC Mains Frequency
VO	5			V	Output Voltage (at continuous power)
IO	1			A	Power Supply Output Current (corresponding to peak power)
Power			5.00	W	Continuous Output Power
n			0.70		Efficiency Estimate at output terminals. Under 0.7 if no better data available
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	ms	Bridge Rectifier Conduction Time Estimate
Add Bias Winding	YES		YES		Choose Yes to add a Bias winding to power the LinkSwitch-II.
CIN	14.7			uF	Input Capacitance
ENTER LinkSwitch-II VARIABLES					
Chosen Device	**LNK616**		LNK616		Chosen LinkSwitch-II device
Package	**PG**		PG		Select package (PG, GG or DG)
ILIMITMIN			0.39	A	Minimum Current Limit
ILIMITTYP			0.41	A	Typical Current Limit
ILIMITMAX			0.45	A	Maximum Current Limit
FS	67.25		67.25	kHz	Typical Device Switching Frequency at maximum power
VOR			82.50	V	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10.00	V	LinkSwitch-II on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop
KP			2.31		Ensure KDP > 1.3 for discontinuous mode operation
FEEDBACK WINDING PARAMETERS					
NFB			6.00		Feedback winding turns
VFLY			4.71	V	Flyback Voltage
VFOR			5.00	V	Forward voltage
BIAS WINDING PARAMETERS					
VB	9		9.00	V	Bias Winding Voltage. Ensure that VB > VFLY. Bias winding is assumed to be AC-STACKED on top of Feedback winding
NB			6.00		Bias Winding number of turns

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DESIGN PARAMETERS				
DCON	4.5	4.50	us	Output diode conduction time
TON		4.31	us	LinkSwitch-II On-time (calculated at minimum inductance)
RUPPER		12.88	k-ohm	Upper resistor in Feedback resistor divider
RLOWER		9.16	k-ohm	Lower resistor in resistor divider

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				
Core Type				
Core	**EE16**	EE16		Enter Transformer Core. Based on the output power the recommended core sizes are EE19 or EE22
Bobbin		EE16_BOBBIN		Generic EE16_BOBBIN
AE		19.20	mm^2	Core Effective Cross Sectional Area
LE		35.00	mm^2	Core Effective Path Length
AL		1140.00	nH/turn ^2	Ungapped Core Effective Inductance
BW		8.60	mm	Bobbin Physical Winding Width
M		0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L		3.00		Number of Primary Layers
NS		7.00		Number of Secondary Turns. To adjust Secondary number of turns change DCON

DC INPUT VOLTAGE PARAMETERS				
VMIN		87.45	V	Minimum DC bus voltage
VMAX		374.77	V	Maximum DC bus voltage

CURRENT WAVEFORM SHAPE PARAMETERS			
DMAX	0.29		Maximum duty cycle measured at VMIN
IAVG	0.09	A	Input Average current
IP	0.39	A	Peak primary current
IR	0.39	A	primary ripple current
IRMS	0.14	A	Primary RMS current

TRANSFORMER PRIMARY DESIGN PARAMETERS				
LPMIN		966.73	uH	Minimum Primary Inductance
LPTYP		1074.14	uH	Typical Primary inductance
LP_TOLERANCE		10.00		Tolerance in primary inductance
NP		105.00		Primary number of turns. To adjust Primary number of turns change BM_TARGET
ALG		87.68	nH/turn ^2	Gapped Core Effective Inductance
BM_TARGET	2200	2200.00	Gauss	Target Flux Density
BM		2184.51	Gauss	Maximum Operating Flux Density (calculated at nominal inductance), BM < 2500 is recommended
BP		2643.26	Gauss	Peak Operating Flux Density (calculated at maximum inductance and max current limit), BP < 3000 is recommended
BAC		1092.26	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur		165.37		Relative Permeability of Ungapped Core
LG		0.25	mm	Gap Length (LG > 0.1 mm)
BWE		25.80	mm	Effective Bobbin Width
OD		0.25	mm	Maximum Primary Wire Diameter including insulation
INS		0.05		Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.20	mm	Bare conductor diameter
AWG		33.00		Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		50.80		Bare conductor effective area in circular mils
CMA		362.53		Primary Winding Current Capacity (200 < CMA < 500)

TRANSFORMER SECONDARY DESIGN PARAMETERS			
Lumped parameters			
ISP	5.84	A	Peak Secondary Current
ISRMS	2.16	A	Secondary RMS Current
IRIPPLE	1.92	A	Output Capacitor RMS Ripple Current
CMS	432.77		Secondary Bare Conductor minimum circular mils
AWGS	23.00		Secondary Wire Gauge (Rounded up to next larger standard AWG value)

VOLTAGE STRESS PARAMETERS			
VDRAIN	568.02	V	Maximum Drain Voltage Estimate (Assumes 20% Zener clamp tolerance and an additional 10% temperature tolerance)
PIVS	29.98	V	Output Rectifier Maximum Peak Inverse Voltage

Note: Different spreadsheet revisions may give slightly different spreadsheet values.

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9 Performance Data

All measurements were taken at room temperature unless otherwise specified, with 60 Hz input frequency. Measurements were taken at the end of a 6 ft, 0.3 Ω, 24 AWG output cable.

9.1 Efficiency

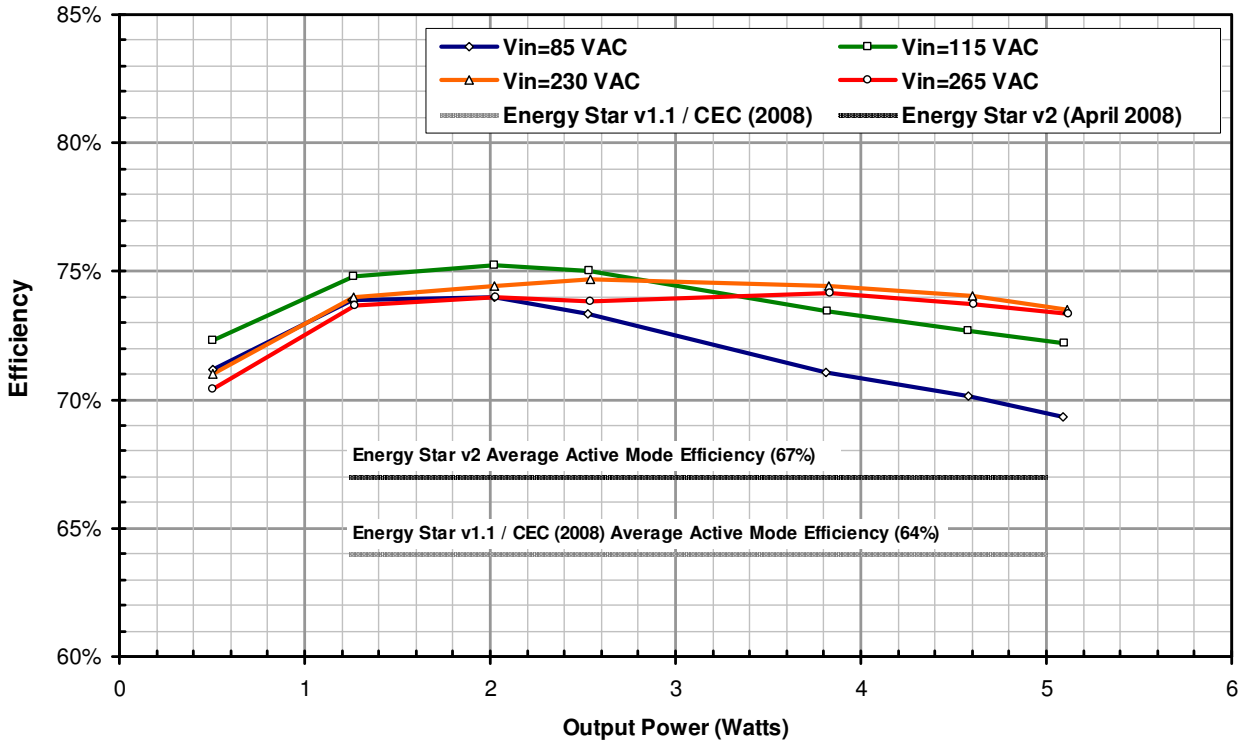

Figure 6 – Efficiency vs. Output Power.

9.2 Active Mode CEC Measurement Data

The power supply passes both Energy Star v1.1 and v2 (April 2008) limits.

% of Full Load	Efficiency (%)	
	115 VAC	230 VAC
25	74.8	74.0
50	75.0	74.7
75	73.5	74.4
100	72.2	73.5
Average	**73.9%**	**74.2%**
Energy Star v1.1	**64%**	**64%**
Energy Star v2	**67%**	**67%**

Figure 7 – Average Active Mode Efficiency.

9.2.1 Energy Star v1.1 / CEC (2008)

As part of the U. S. Energy Independence and Security Act of 2007 all single-output adapters, including those provided with products for sale in the USA after July 1, 2008, must meet the Energy Star v1.1 specification for minimum active-mode efficiency and no-load input power. Note that battery chargers are exempt from these requirements except in the state of California, where they must also be compliant.

Minimum active-mode efficiency is defined as the average efficiency at 25%, 50%, 75%, and 100% of rated output power with the limit based on the nameplate output power:

Nameplate Output (P_{NP})	Minimum Efficiency in Active Mode of Operation
< 1 W	$0.5 \times P_{NP}$
≥ 1 W to ≤ 49 W	$0.09 \times \ln(P_{NP}) + 0.5$ [ln = natural log]
> 49 W	0.84

Nameplate Output (P_{NP})	Maximum No-load Input Power
All	≤ 0.5 W

For single-input voltage adapters the measurement is made at the rated (single) nominal input voltage only (either 115 VAC or 230 VAC). For universal input adapters, the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard, the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the CEC/Energy Star v1.1 standard.

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9.2.2 Energy Star v2 (April 2008)

The Energy Star v2 specification (planned to take effect Nov 1, 2008) increases the previously stated requirements.

Standard Models

Nameplate Output (P_{NP})	Minimum Efficiency in Active Mode of Operation (Rounded to Hundreds)
≤ 1 W	≥ 0.48 × P_{NP} + 0.14
> 1 W to ≤ 49 W	≥ 0.0626 × ln (P_{NP}) + 0.622 [ln = natural log]
> 49 W	0.87

Nameplate Output (P_{NP})	Maximum No-load Input Power
0 to <50 W	≤ 0.3 W
≥50 to ≤250 W	≤ 0.5 W

Low-voltage Models

A low-voltage model is an external power supply (EPS) with a nameplate output voltage of less than 6 V and a nameplate output current greater than or equal to 550 mA.

Nameplate Output (P_{NP})	Minimum Efficiency in Active Mode of Operation (Rounded to Hundreds)
≤1 W	≥ 0.497 × P_{NP} + 0.067
>1 W to ≤49 W	≥ 0.075 × ln (P_{NP}) + 0.561 [ln = natural log]
>49 W	≥ 0.86

Nameplate Output (P_{NP})	Maximum No-load Input Power
0 to <50 W	≤ 0.3 W
≥50 to ≤250 W	≤ 0.5 W

For the latest up-to-date information, please visit the PI Green Room at *www.powerint.com*.

9.3 No-Load Input Power

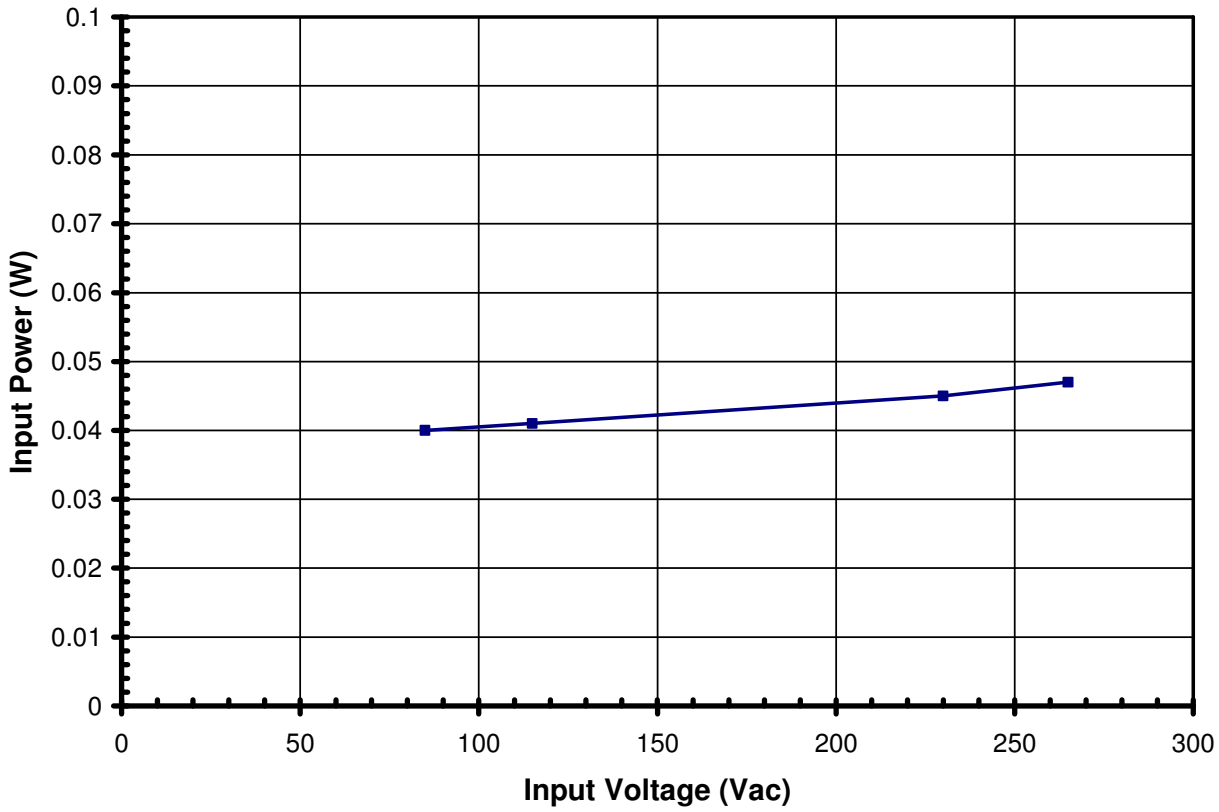

Figure 8 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz. (To achieve no-load of less than 30 mW, remove the preload resistor (R9) and replace it with a 6.2 V clamp diode).

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9.4 Regulation

9.4.1 Load, Line and Temperature

The output characteristic was tested at the end of a 6’ output cable. The DC resistance of the cable was approximately 0.3 Ω.

The measurements were made with the supply inside a sealed plastic enclosure which was then placed within a cardboard box. The cardboard box ensures air flow from the thermal chamber does not affect the test. The ambient temperature inside the cardboard box was monitored, and the temperature of the thermal chamber was adjusted to maintain the desired temperature.

The unit was allowed to thermally stabilize for 30 minutes, unloaded, at each measurement temperature prior to data being recorded.

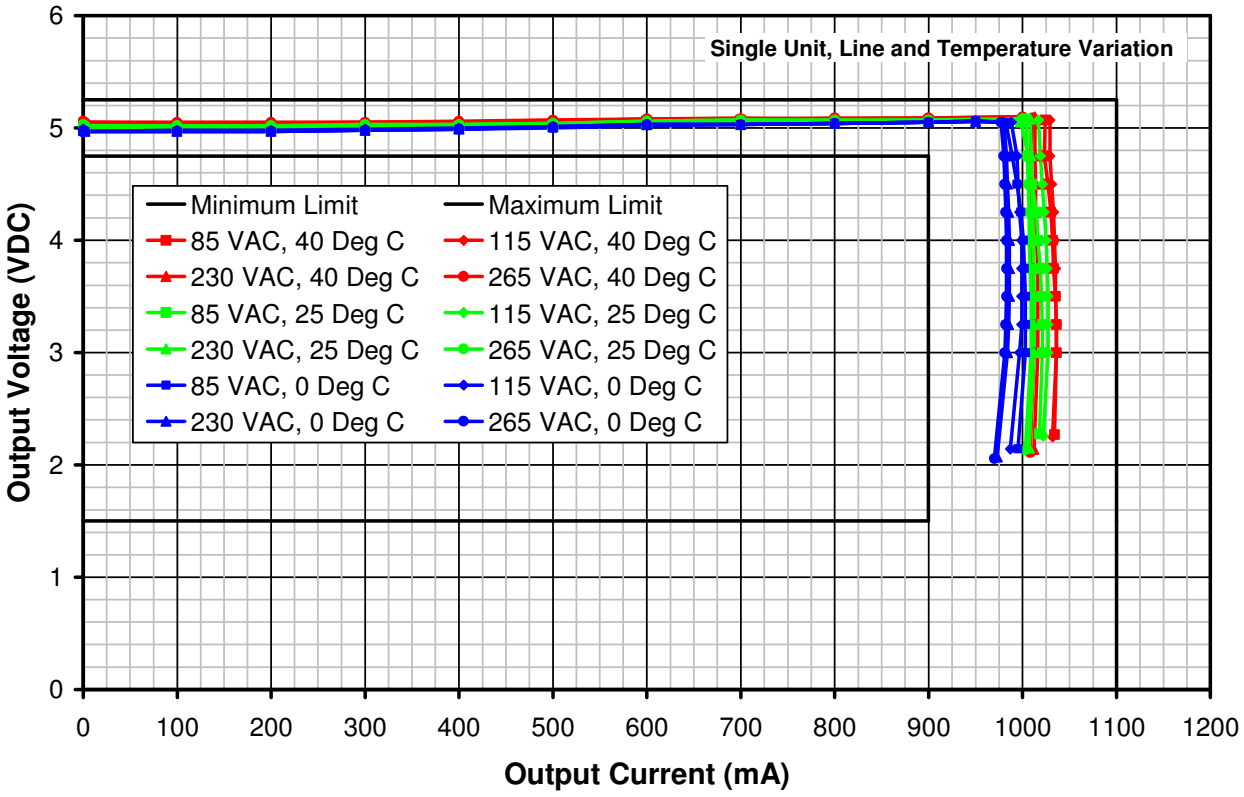

Figure 9 – Composite Output Regulation Across Load, Line, and Temperature.

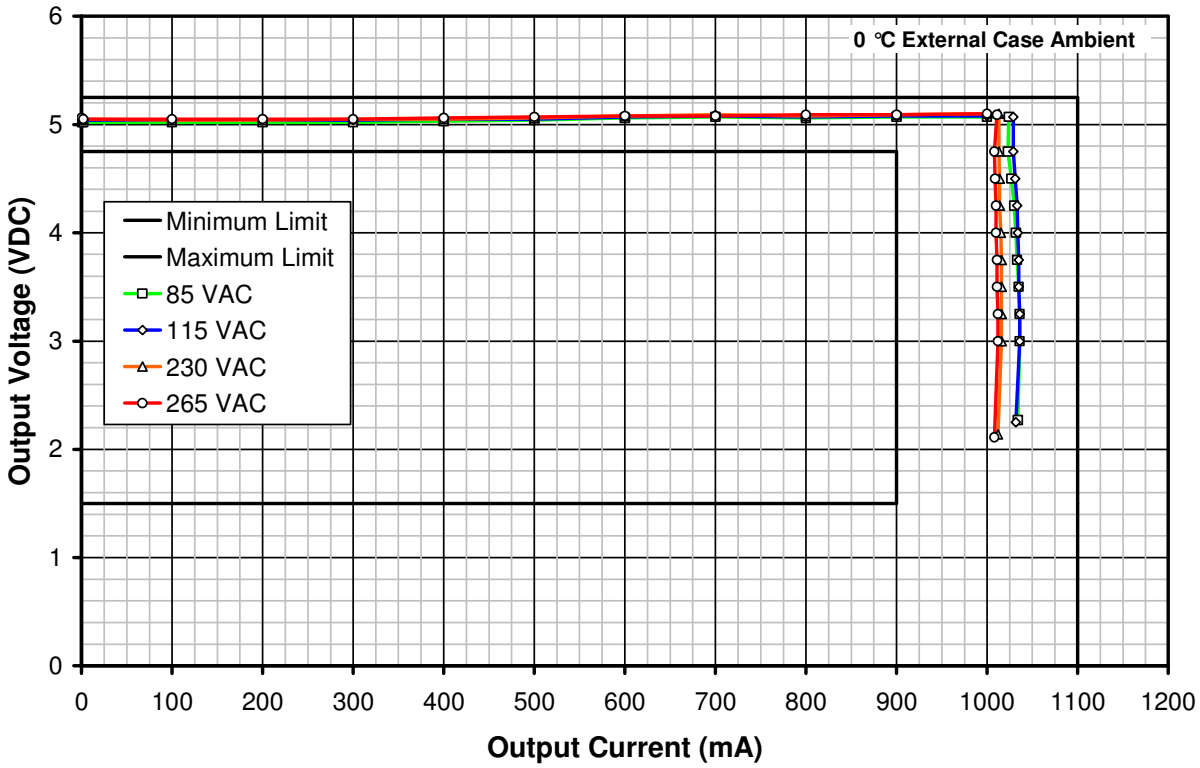

Figure 10 – Typical CV/CC Characteristic Over Line at 0 °C.

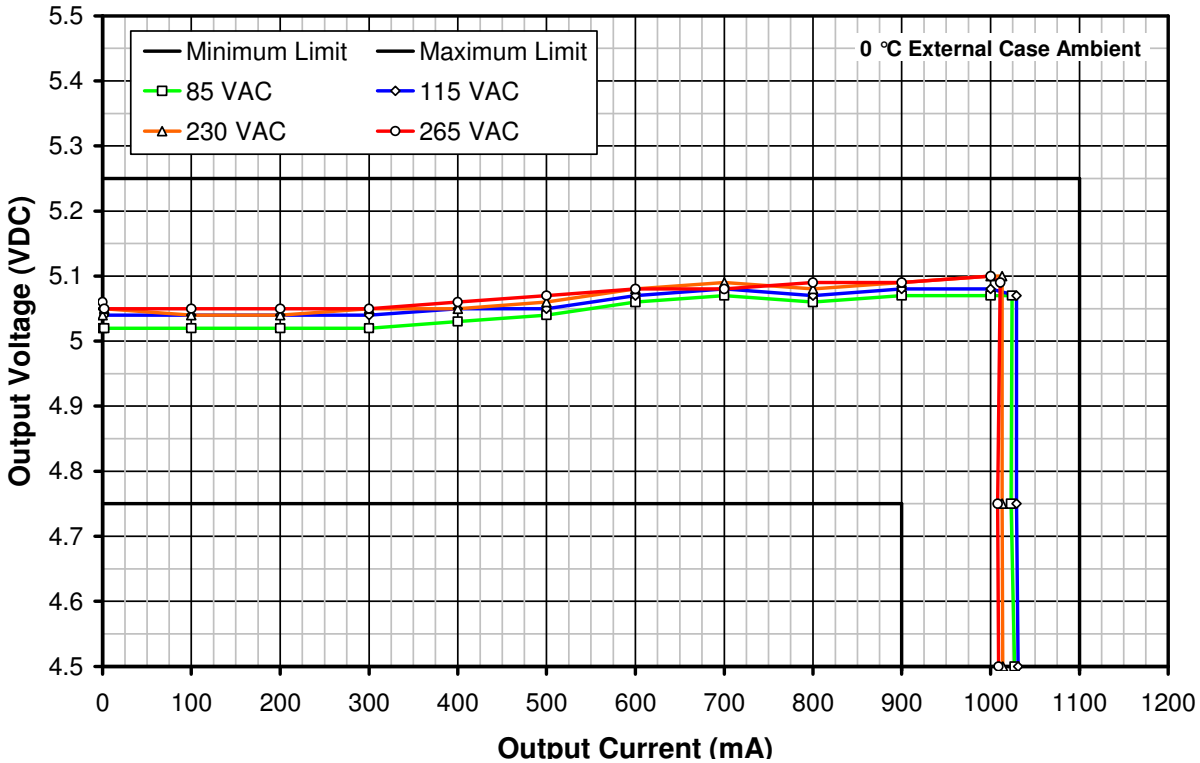

Figure 11 – Typical CV/CC Characteristic Over Line at 0 °C. Expanded View, Illustrating Effect of Cable Drop Compensation.

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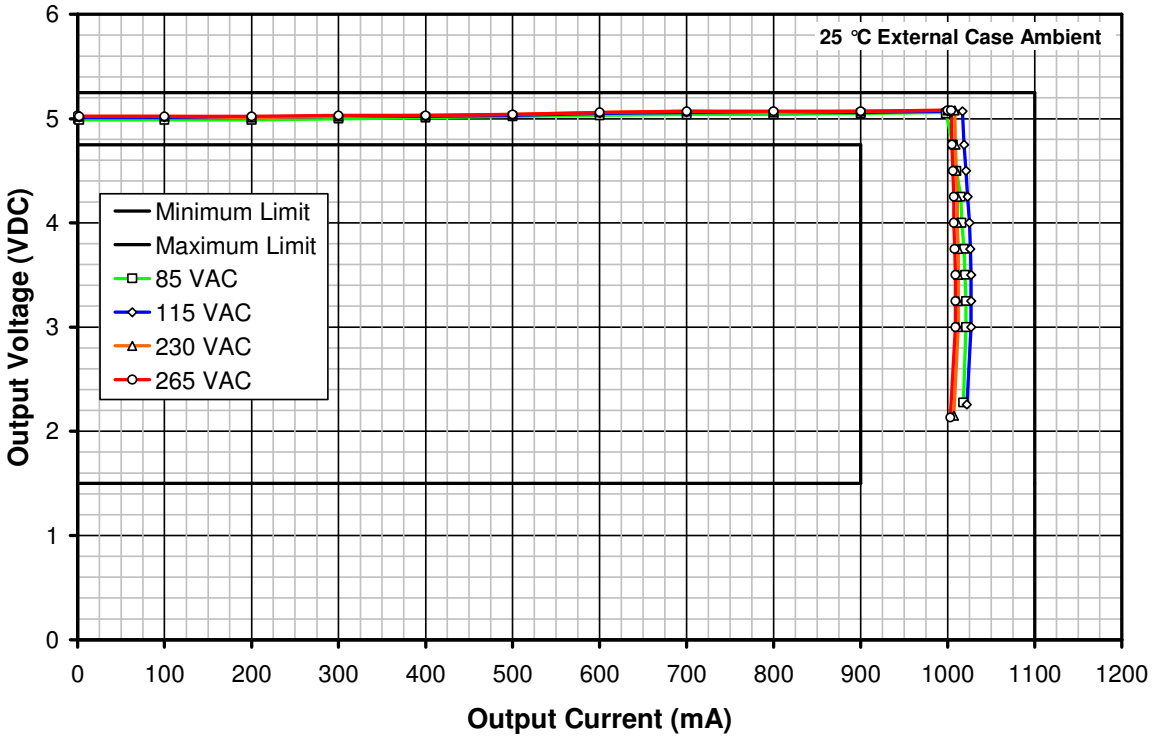

Figure 12 – Typical CV/CC Characteristic Over Line at 25 °C.

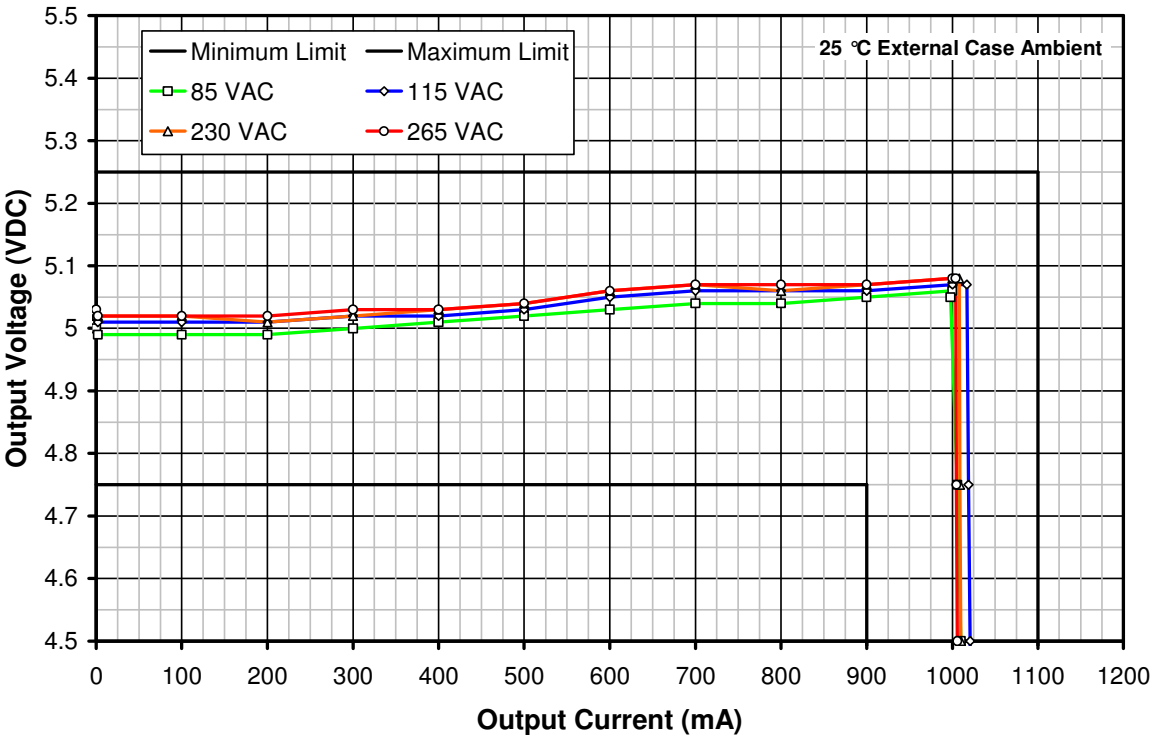

Figure 13 – Typical CV/CC Characteristic Over Line at 25 °C. Expanded View Illustrating Effect of Cable Drop Compensation.

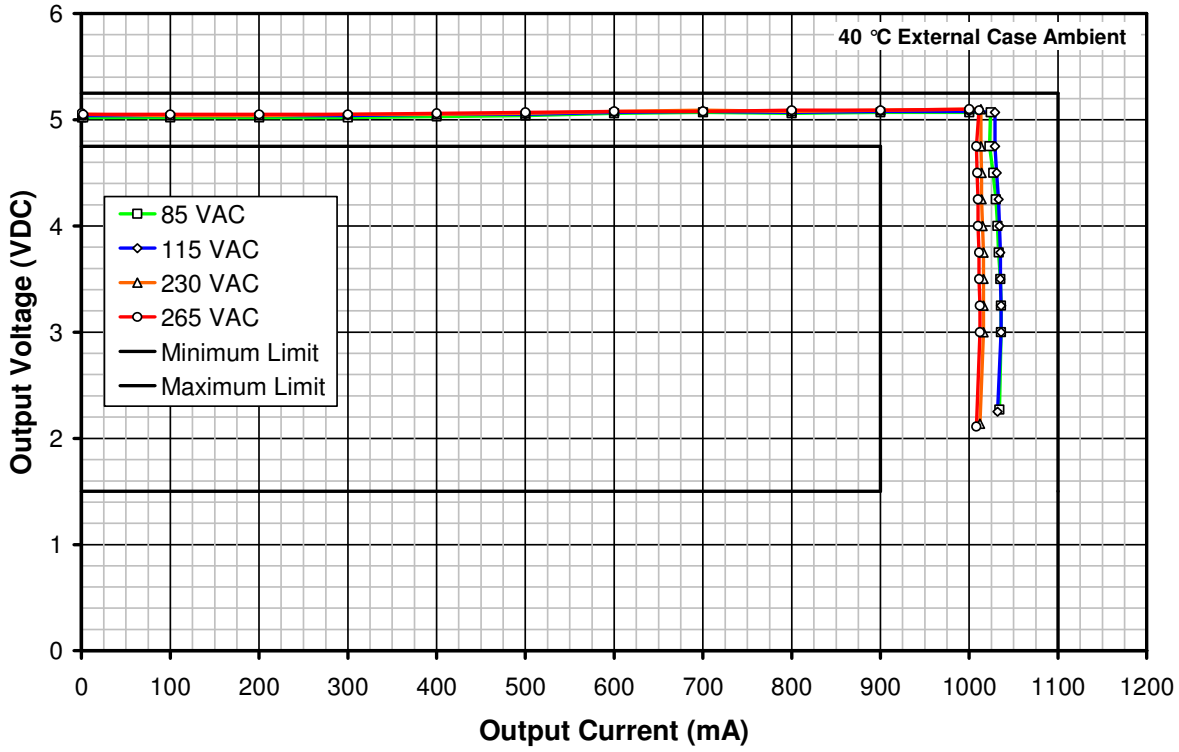

Figure 14 – Typical CV/CC Characteristic Over Line at 40 ℃.

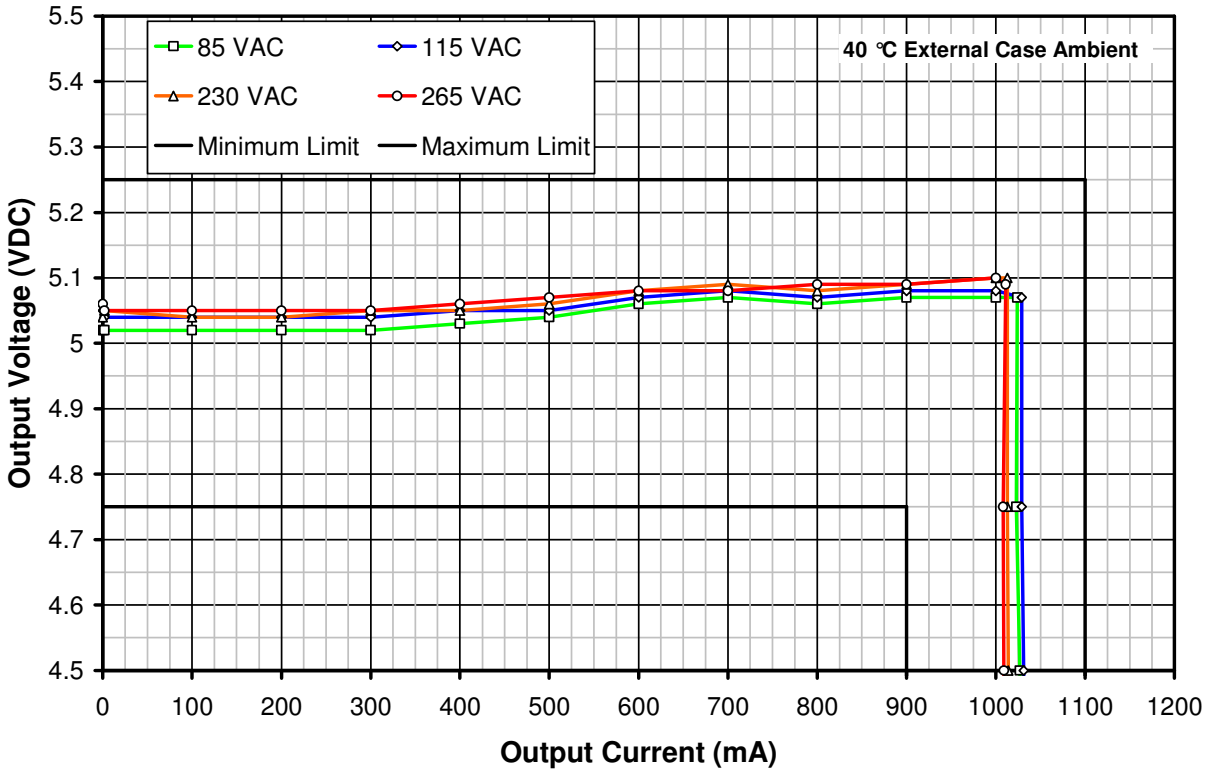

Figure 15 – Typical CV/CC Characteristic Over Line at 40 ℃. Expanded View Illustrating Effect of Cable Drop Compensation.

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10 Thermal Performance

10.1 Operating Temperature Survey

Thermal performance was measured inside an enclosure at full load with no airflow. A thermocouple was attached to U1's source pin.

Item	85 VAC	115 VAC	175 VAC	230 VAC	265 VAC
Ambient	40 ^{0}C	40 ^{0}C	40 ^{0}C	40 ^{0}C	40 ^{0}C
U1 Source Pin	97 ^{0}C	90.7 ^{0}C	89.3 ^{0}C	90.6 ^{0}C	93.1 ^{0}C

11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

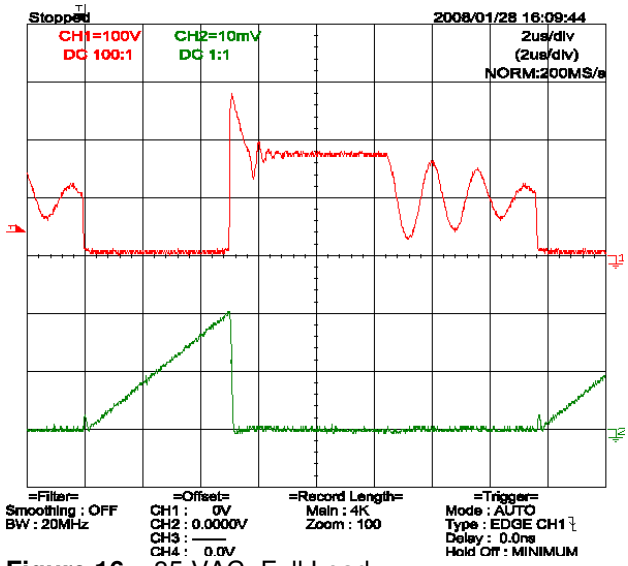

Figure 16 – 85 VAC, Full Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 200 mA / div, 2 us / div.

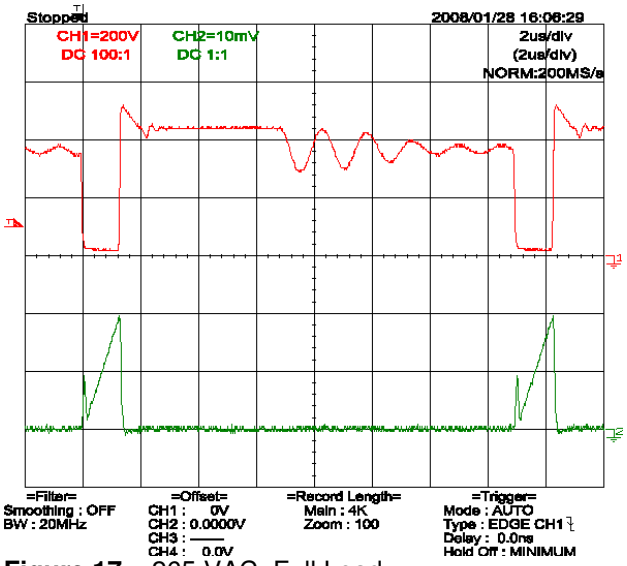

Figure 17 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 200 mA / div, 2 us / div.

11.2 Output Voltage Start-up Profile

11.2.1 No-Load Output Voltage Start-up Characteristic

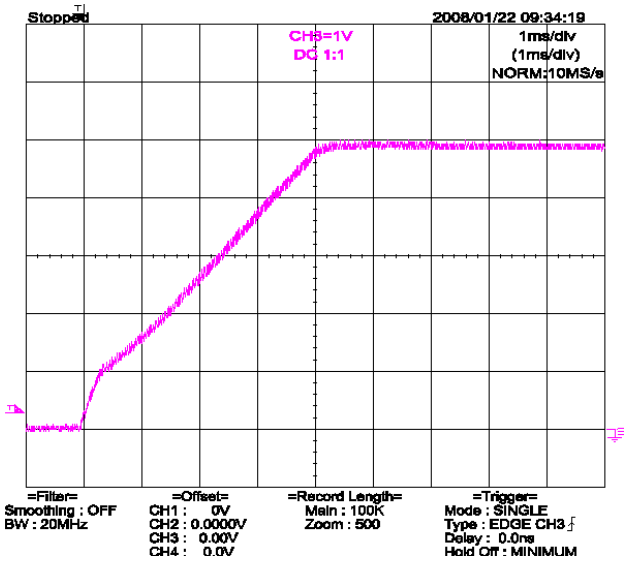

Figure 18 – Start-up Profile (No Load),
115 VAC, 1 V, 1 ms / div.

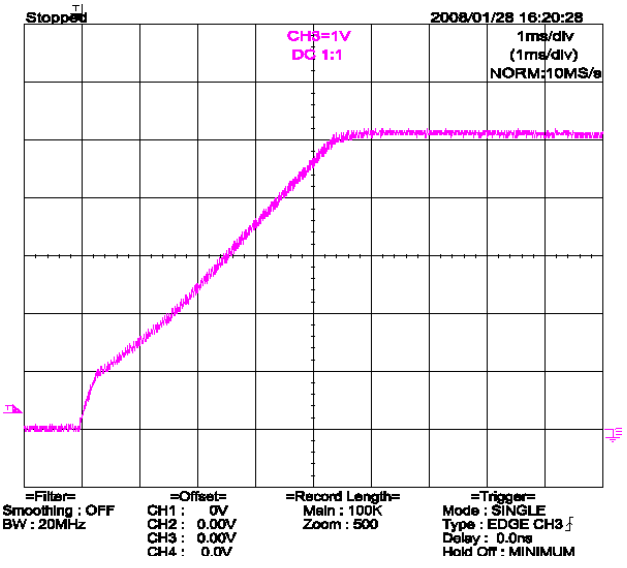

Figure 19 – Start-up Profile (No Load),
230 VAC, 1 V, 1 ms / div.

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11.2.2 Output Voltage Start-up Characteristic - Resistive Load (5 Ω)

The voltage was measured at the load.

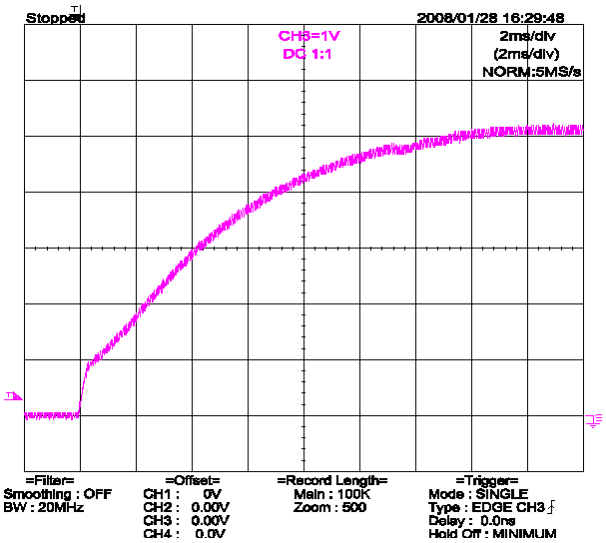

Figure 20 – Start-up Profile,
115 VAC, 1 V, 2 ms / div.

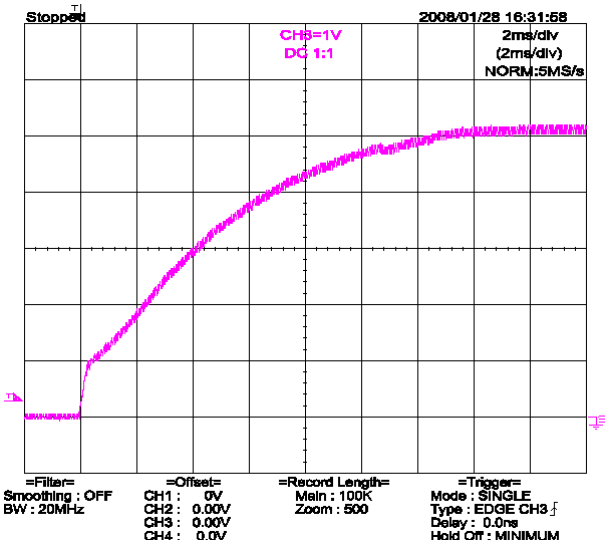

Figure 21 – Start-up Profile,
230 VAC, 1 V, 2 ms / div.

11.2.3 Output Voltage Start-up Characteristic - Battery-simulator Load

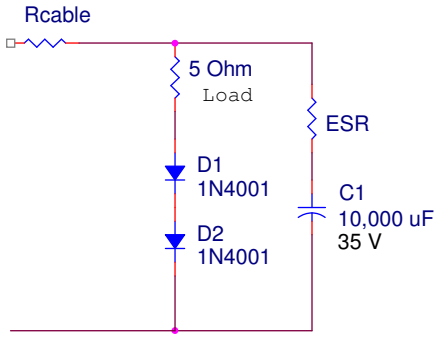

Figure 22 – Battery Simulator Schematic.

The voltage was measured at the PCB.

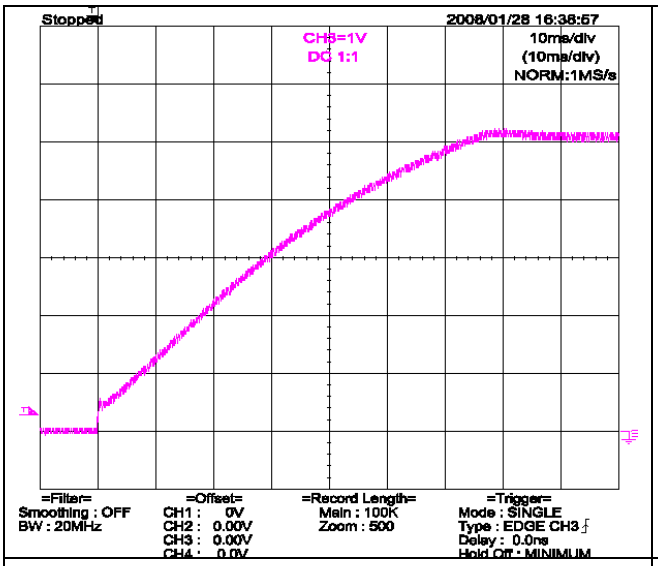

Figure 23– Start-up Profile,
115 VAC Vertical: 1 V / div.
Horizontal: 10 ms / div.

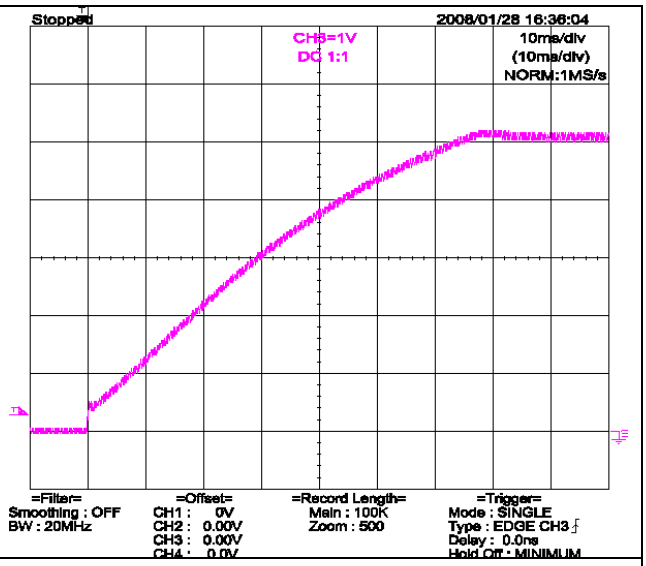

Figure 24 – Start-up Profile, 230 VAC
Vertical: 1 V / div.
Horizontal: 10 ms / div.

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11.3 Drain Voltage and Current Start-up Profile

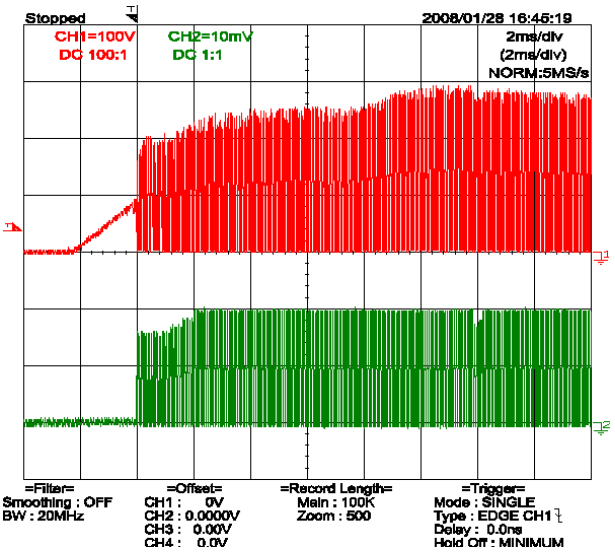

Figure 25 – 85 VAC Input and Maximum Load
Upper V_{DRAIN}, 100 V, 2 ms / div.
Lower: I_{DRAIN}, 200 mA / div.

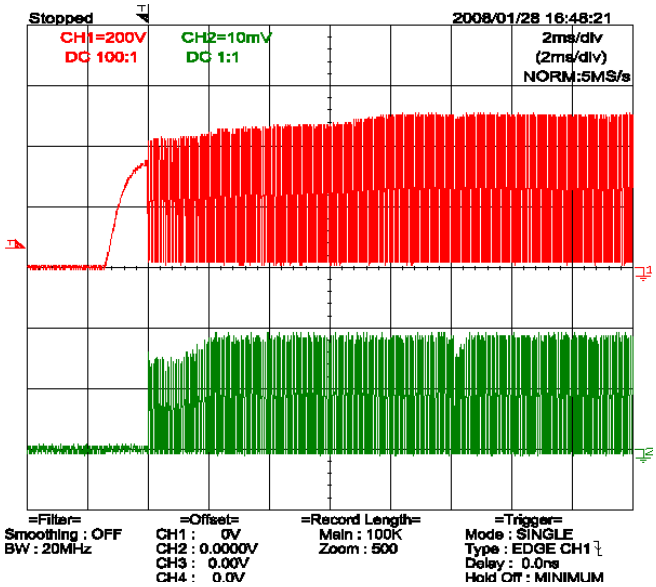

Figure 26 – 265 VAC Input and Maximum Load
Upper: V_{DRAIN}, 200 V, 2 ms / div.
Lower: I_{DRAIN}, 200 mA / div.

11.4 Load Transient Response (50% to 100% Load Step)

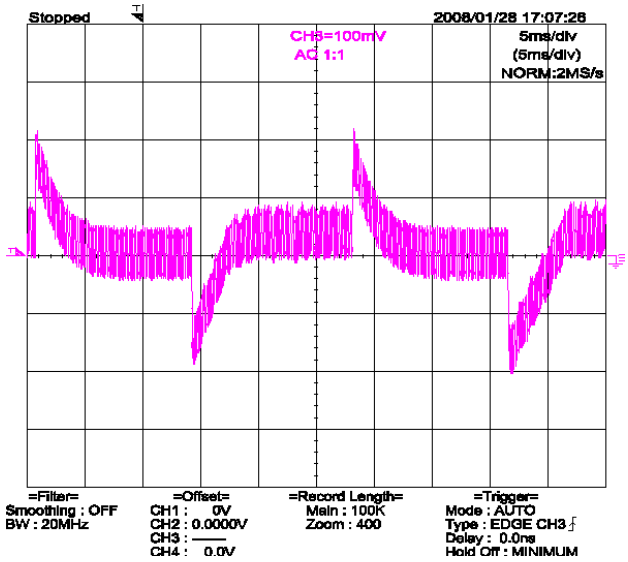

Figure 27 – Transient Response, 115 VAC
100-50-100% Load Step
Output Voltage 100 mV, 5 ms / div.

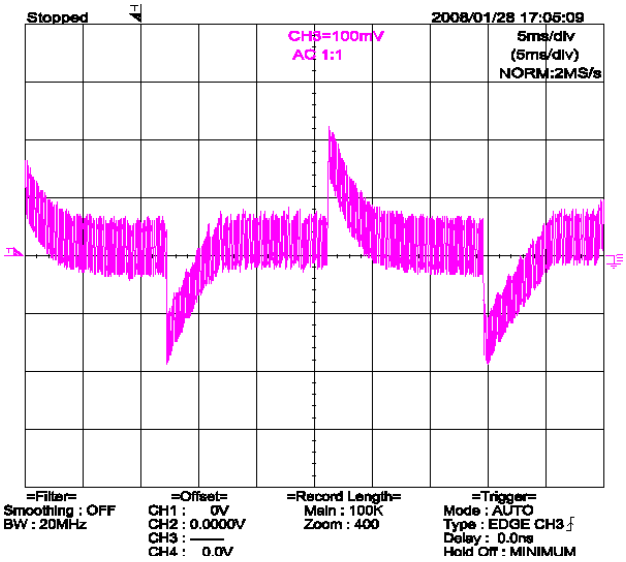

Figure 28 – Transient Response, 230 VAC
100-50-100% Load Step
Output Voltage 100 mV, 5 ms / div.

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11.5 Output Ripple Measurements

11.5.1 Ripple Measurement Technique

For DC output ripple measurements, use a modified oscilloscope test probe to reduce spurious signals. Details of the probe modification are provided in figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. Use a 0.1 µF / 50 V ceramic capacitor and 1.0 µF / 50 V aluminum electrolytic capacitor. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

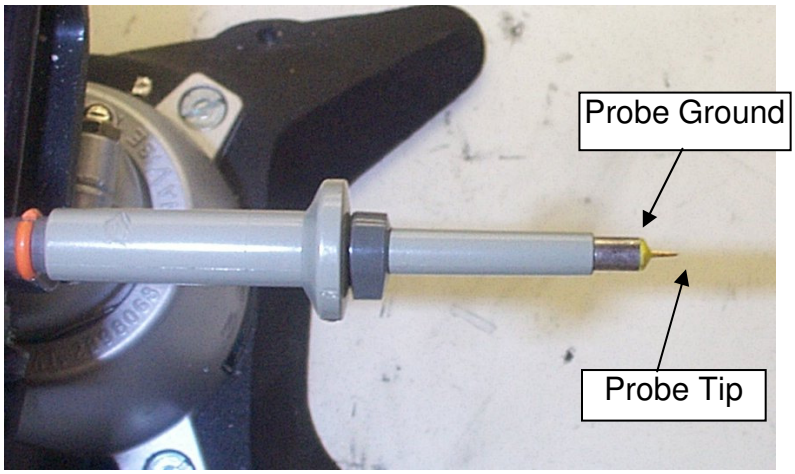

Figure 29 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

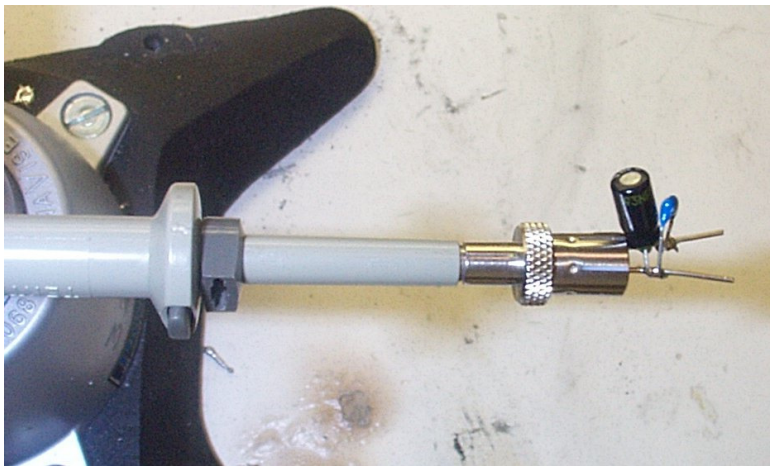

Figure 30 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

11.5.2 Ripple Measurement Results

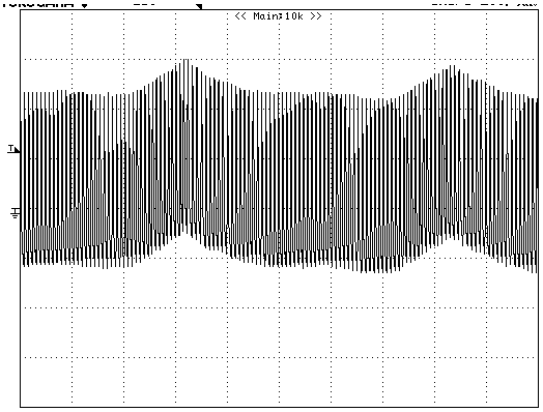

Figure 31 – Ripple, 85 VAC, Full Load, 20 mV, 200 V / div.

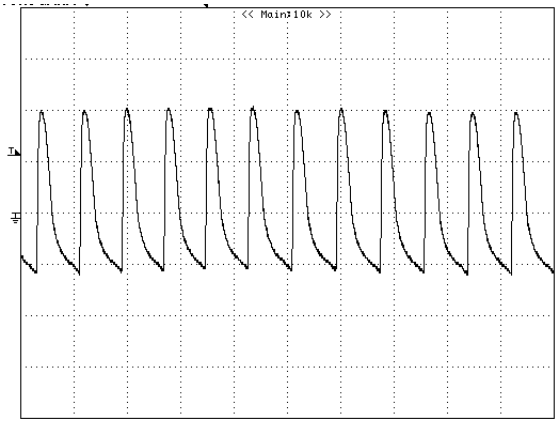

Figure 32 – Ripple, 85 VAC, Full Load, 20 mV, 20 µs / div.

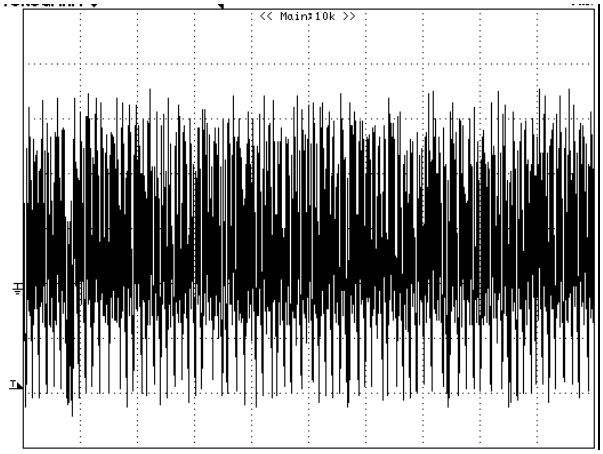

Figure 33 – Ripple, 85 VAC, Worst-case Noise, 20 mV, 5 ms / div.

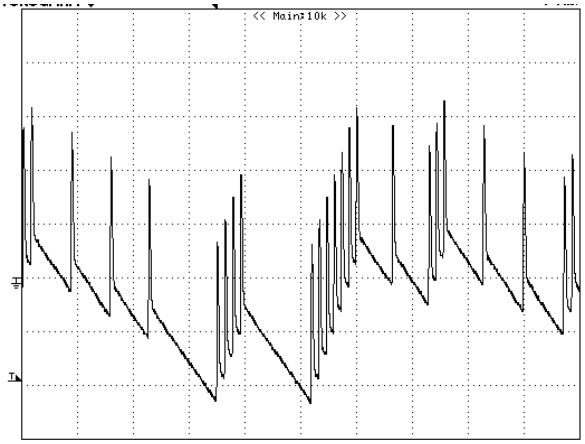

Figure 34 – Ripple, 85 VAC, Worst-case Noise, 20 mV, 100 Cs / div.

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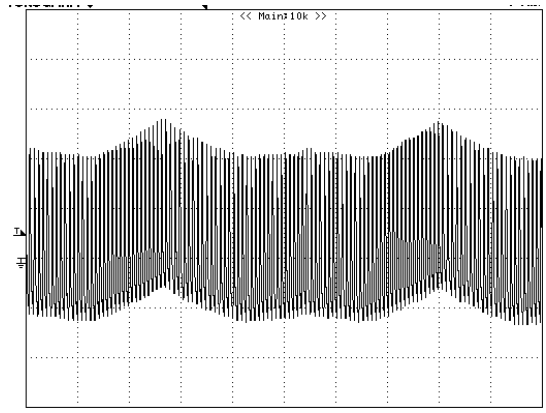

Figure 35 – Ripple, 265 VAC, Full Load, 20 mV, 200 µs / div.

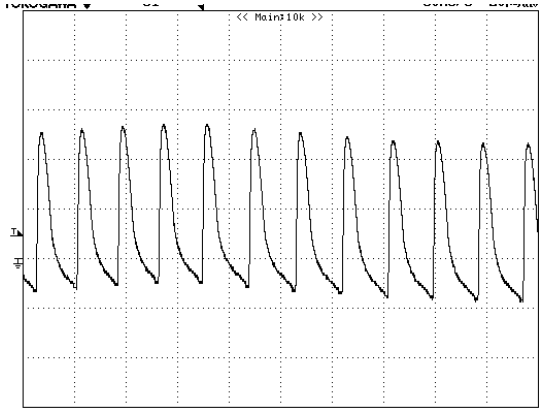

Figure 36 – Ripple, 265 VAC, Full Load, 20 mV, 20 µs / div.

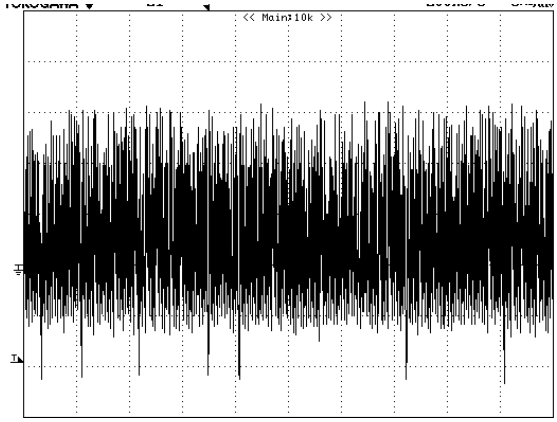

Figure 37 – Ripple, 265 VAC, Worst Case Noise, 20 mV / div, 5 ms / div.

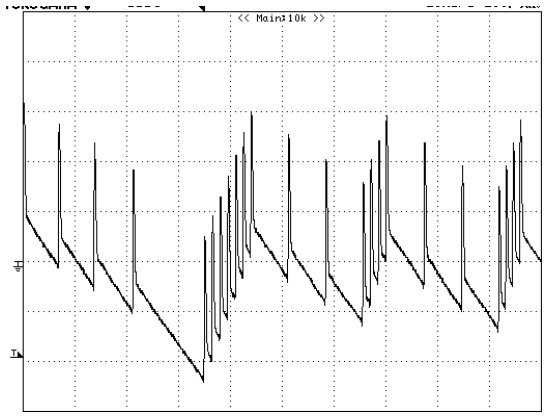

Figure 38 – Ripple, 265 VAC, Worst Case Noise, 20 mV / div, 100 µs / div.

12 Line Surge

Differential input line 1.2 µs / 50 µs surge testing to IEC61000-4-5 standards was completed on a single test unit. The input voltage was set at 230 VAC / 60 Hz. The output current was 1 A and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+500	230	L to N	90	Pass
-500	230	L to N	90	Pass
+750	230	L to N	90	Pass
-750	230	L to N	90	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass

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13 Conducted EMI

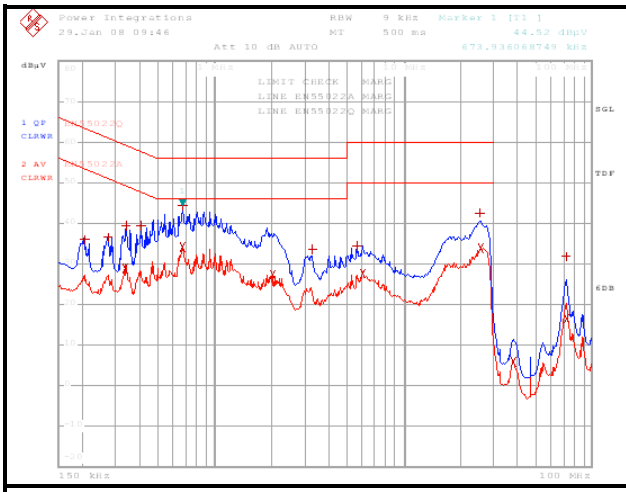

Figure 39 – 115 VAC Neutral, Output Earth Grounded.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	673.936068749 kHz	44.43	N gnd	-11.56
1	Quasi Peak	25.2115041566 MHz	42.71	L1 gnd	-17.28
1	Quasi Peak	401.705024172 kHz	39.48	L1 gnd	-18.33
1	Quasi Peak	335.832355405 kHz	39.32	L1 gnd	-19.98
1	Quasi Peak	269.806440381 kHz	36.65	N gnd	-24.46
1	Quasi Peak	202.1773373 kHz	36.15	N gnd	-27.36
1	Quasi Peak	5.66751514993 MHz	34.38	L1 gnd	-25.61
2	Average	667.263434405 kHz	34.29	N gnd	-11.70
2	Average	25.4636191981 MHz	33.91	N gnd	-16.08
1	Quasi Peak	3.27881664913 MHz	33.66	L1 gnd	-22.34
1	Quasi Peak	72.3876333654 MHz	31.79	N gnd	
2	Average	332.507282579 kHz	29.06	N gnd	-20.32
2	Average	6.01618153549 MHz	27.62	N gnd	-22.37
2	Average	2.03372014292 MHz	27.27	L1 gnd	-18.73
2	Average	72.3876333654 MHz	16.60	N gnd	
2	Average	38.2909777415 MHz	5.89	N gnd	

Figure 40 – 115 VAC Neutral, Table.

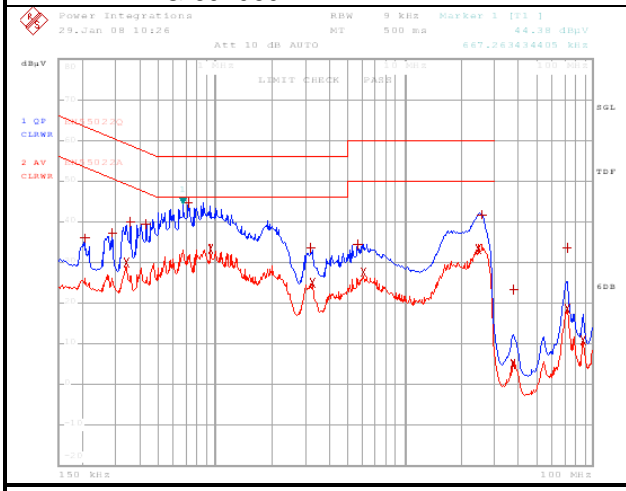

Figure 41 – 115 VAC Line, Output Earth Grounded.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	715.396717193 kHz	44.79	L1 gnd	-11.20
1	Quasi Peak	25.7182553901 MHz	41.92	L1 gnd	-18.07
1	Quasi Peak	356.492812486 kHz	39.84	L1 gnd	-18.96
1	Quasi Peak	426.417977756 kHz	39.36	L1 gnd	-17.95
1	Quasi Peak	286.404973226 kHz	37.44	L1 gnd	-23.17
1	Quasi Peak	202.1773373 kHz	36.06	N gnd	-27.45
1	Quasi Peak	5.66751514993 MHz	34.49	L1 gnd	-25.50
1	Quasi Peak	72.3876333654 MHz	33.70	N gnd	
1	Quasi Peak	3.21421100787 MHz	33.55	L1 gnd	-22.44
2	Average	945.247220176 kHz	33.54	L1 gnd	-12.46
2	Average	24.7147379243 MHz	33.48	L1 gnd	-16.51
2	Average	335.832355405 kHz	29.98	N gnd	-19.31
2	Average	6.01618153549 MHz	27.53	N gnd	-22.46
2	Average	3.27881664913 MHz	25.01	L1 gnd	-20.98
1	Quasi Peak	37.91185915 MHz	23.38	L1 gnd	
2	Average	72.3876333654 MHz	18.64	N gnd	
2	Average	88.3266692478 MHz	10.78	N gnd	
2	Average	37.5364942079 MHz	5.09	L1 gnd	

Figure 42 – 115 VAC Line, Table.

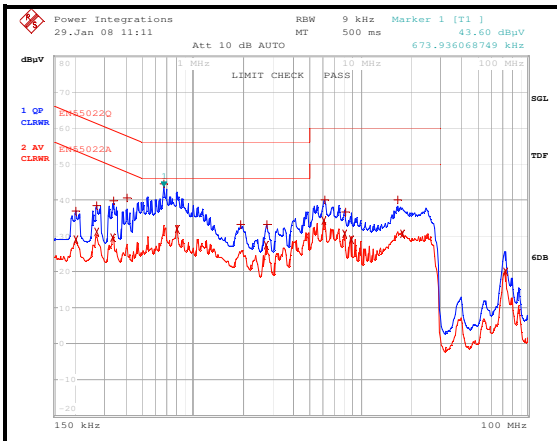

Figure 43 – 230 VAC Neutral, Output Earth Grounded.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	673.936068749 kHz	44.40	L1 gnd	-11.59
1	Quasi Peak	401.705024172 kHz	40.60	L1 gnd	-17.21
1	Quasi Peak	16.599731303 MHz	40.03	L1 gnd	-19.96
1	Quasi Peak	6.13710678435 MHz	39.88	N gnd	-20.12
1	Quasi Peak	335.832355405 kHz	39.79	L1 gnd	-19.50
1	Quasi Peak	267.135089486 kHz	38.37	N gnd	-22.83
1	Quasi Peak	200.175581485 kHz	36.85	N gnd	-26.74
1	Quasi Peak	8.18999279463 MHz	36.58	N gnd	-23.41
2	Average	6.07634335085 MHz	34.18	N gnd	-15.82
1	Quasi Peak	2.76855896362 MHz	33.25	N gnd	-22.74
1	Quasi Peak	1.93501493419 MHz	33.08	L1 gnd	-22.91
2	Average	806.126927408 kHz	31.93	N gnd	-14.06
2	Average	267.135089486 kHz	31.03	N gnd	-20.17
2	Average	17.7971587654 MHz	30.59	N gnd	-19.40
2	Average	8.10890375706 MHz	30.52	N gnd	-19.47
2	Average	332.507282579 kHz	29.60	N gnd	-19.78
2	Average	8.78078080862 MHz	29.03	N gnd	-20.96
2	Average	200.175581485 kHz	28.92	N gnd	-24.67
2	Average	2.74114748873 MHz	27.34	N gnd	-18.65
2	Average	73.111509699 MHz	20.01	N gnd	

Figure 44 – 230 VAC Neutral, Table.

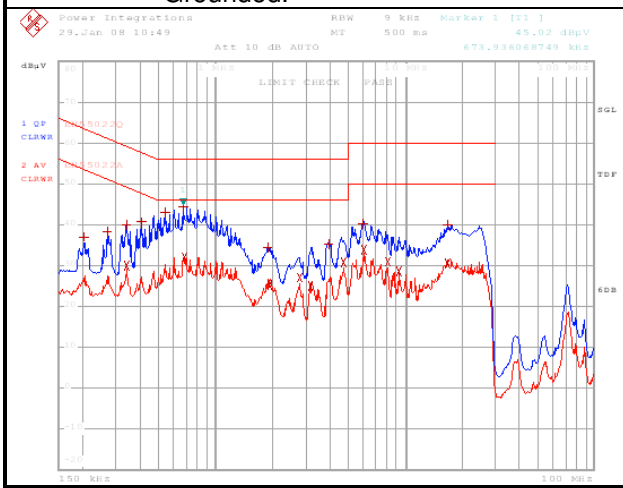

Figure 45 – 230 VAC Line, Output Earth Grounded.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	673.936068749 kHz	44.46	L1 gnd	-11.54
1	Quasi Peak	536.076911993 kHz	43.23	L1 gnd	-12.76
2	Average	680.675429436 kHz	32.13	N gnd	-13.86
2	Average	4.73814079378 MHz	30.77	N gnd	-15.22
2	Average	6.07634335085 MHz	34.02	N gnd	-15.97
1	Quasi Peak	401.705024172 kHz	40.82	L1 gnd	-16.99
2	Average	2.76855896362 MHz	27.05	N gnd	-18.94
2	Average	8.10890375706 MHz	31.02	N gnd	-18.97
2	Average	335.832355405 kHz	30.03	N gnd	-19.27
2	Average	16.765728616 MHz	30.61	L1 gnd	-19.38
1	Quasi Peak	335.832355405 kHz	39.90	L1 gnd	-19.40
1	Quasi Peak	5.95661538167 MHz	40.19	L1 gnd	-19.80
1	Quasi Peak	16.765728616 MHz	40.05	L1 gnd	-19.94
1	Quasi Peak	3.96116774068 MHz	35.37	L1 gnd	-20.62
2	Average	1.91585637048 MHz	25.34	L1 gnd	-20.65
2	Average	3.15087835298 MHz	25.11	L1 gnd	-20.88
2	Average	9.32097576636 MHz	28.60	N gnd	-21.39
1	Quasi Peak	1.87810643122 MHz	34.50	L1 gnd	-21.49
1	Quasi Peak	267.135089486 kHz	38.39	N gnd	-22.80
1	Quasi Peak	200.175581485 kHz	36.97	N gnd	-26.62

Figure 46 – 230 VAC Line, Table.

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14 Revision History

Date	Author	Revision	Description and changes	Reviewed
15-May-08	JAC	1.0	Initial Release	JD
25-Nov-08	SF	1.0	Updated no-load graph caption text in Figure 8	

Notes

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