19.2.2 Asynchronous Transmission

Asynchronous transmission begins at the next overflow of the divide-by-16 baudrate timer (transition of the baudrate clock f_{BR}), if bit R is set and data has been loaded into TBUF. The transmitted data frame consists of three basic elements:

- Start bit
- Data field (eight or nine bits, LSB first, including a parity bit, if selected)
- Delimiter (one or two stop bits)

Data transmission is double-buffered. When the transmitter is idle, the transmit data loaded in the transmit buffer register is immediately moved to the transmit shift register, thus freeing the transmit buffer for the next data to be sent. This is indicated by the transmit buffer interrupt request line TBIR being activated. TBUF may now be loaded with the next data, while transmission of the previous data continues.

The transmit interrupt request line TIR will be activated before the last bit of a frame is transmitted, that is, before the first or the second stop bit is shifted out of the transmit shift register.

Note: The transmitter output pin TxD must be configured for alternate data output.

19.2.3 Transmit FIFO Operation

The transmit FIFO (TXFIFO) provides the following functionality:

- Enable/disable control
- Programmable filling level for transmit interrupt generation
- Filling level indication
- FIFO clear (flush) operation
- FIFO overflow error generation

The 8-stage transmit FIFO is controlled by the TXFCON control register. When bit TXFEN is set, the transmit FIFO is enabled. The interrupt trigger level defined by TXFITL defines the filling level of the TXFIFO at which a transmit buffer interrupt TBIR or a transmit interrupt TIR is generated. These interrupts are always generated when the filling level of the transmit FIFO is equal to or less than the value stored in TXFITL.

Bitfield TXFFL in the FIFO status register ASCx_FSTAT indicates the number of entries that are actually written (valid) in the TXFIFO. Therefore, the software can verify, in the interrupt service routine, for instance, how many bytes can still be written into the transmit FIFO via register TBUF without getting an overrun error.

The transmit FIFO cannot be accessed directly. All data write operations into the TXFIFO are executed by writing into the TBUF register.

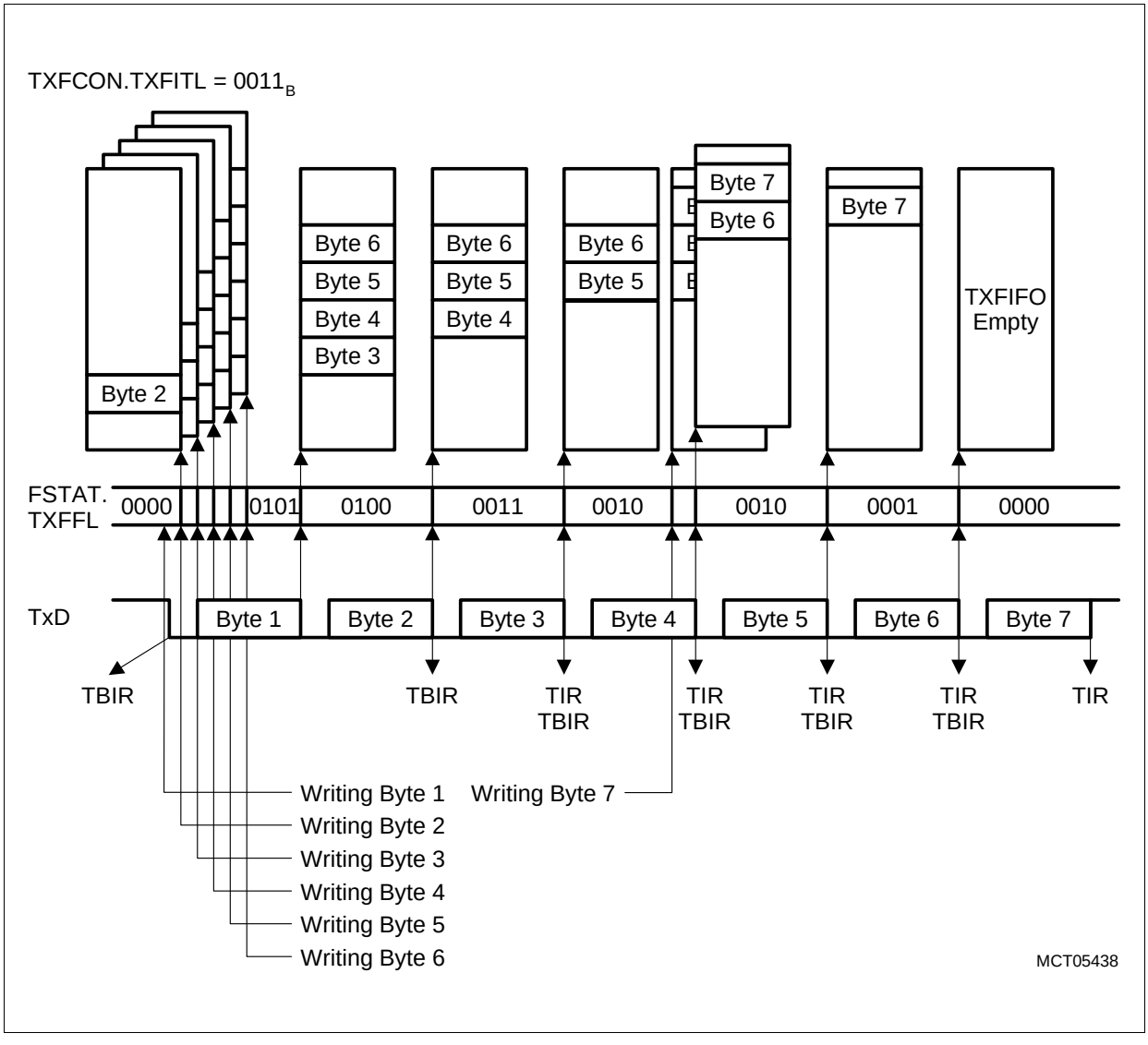

Figure 19-7 Transmit FIFO Operation Example

The example in **Figure 19-7** shows a typical 8-stage transmit FIFO operation. In this example seven bytes are transmitted via the TxD output line. The transmit FIFO interrupt trigger level TXFITL is set to 0011_B. The first byte written into the empty TXFIFO via TBUF is directly transferred into the transmit shift register and is not written into the FIFO. A transmit buffer interrupt will be generated in this case. After byte 1, bytes 2 to 6 are written into the transmit FIFO.

After the transfer of byte 3 from the TXFIFO into the transmit shift register of the ASC, 3 bytes remain in the TXFIFO. Therefore, the value of TXFITL is reached and a transmit buffer interrupt will be generated at the beginning and a transmit interrupt at the end of the byte 3 serial transmission. During the serial transmission of byte 4, another byte (byte 7) is written into the TXFIFO (TBUF write operation). Finally, after the start of the serial transmission of byte 7, the TXFIFO is again empty.

If the TXFIFO is full and additional bytes are written into TBUF, the error interrupt will be generated with bit OE set. In this case, the data byte that was last written into the transmit FIFO is overwritten and the transmit FIFO filling level TXFFL is set to maximum.

The TXFIFO can be flushed or cleared by setting bit TXFFLU in register ASCx_TXFCON. After this TXFIFO flush operation, the TXFIFO is empty and the transmit FIFO filling level TXFFL is set to 0000_B. A running serial transmission is not aborted by a receive FIFO flush operation

Note: The TXFIFO is flushed automatically with a reset operation of the ASC module and if the TXFIFO becomes disabled (resetting bit TXFEN) after it was previously enabled.