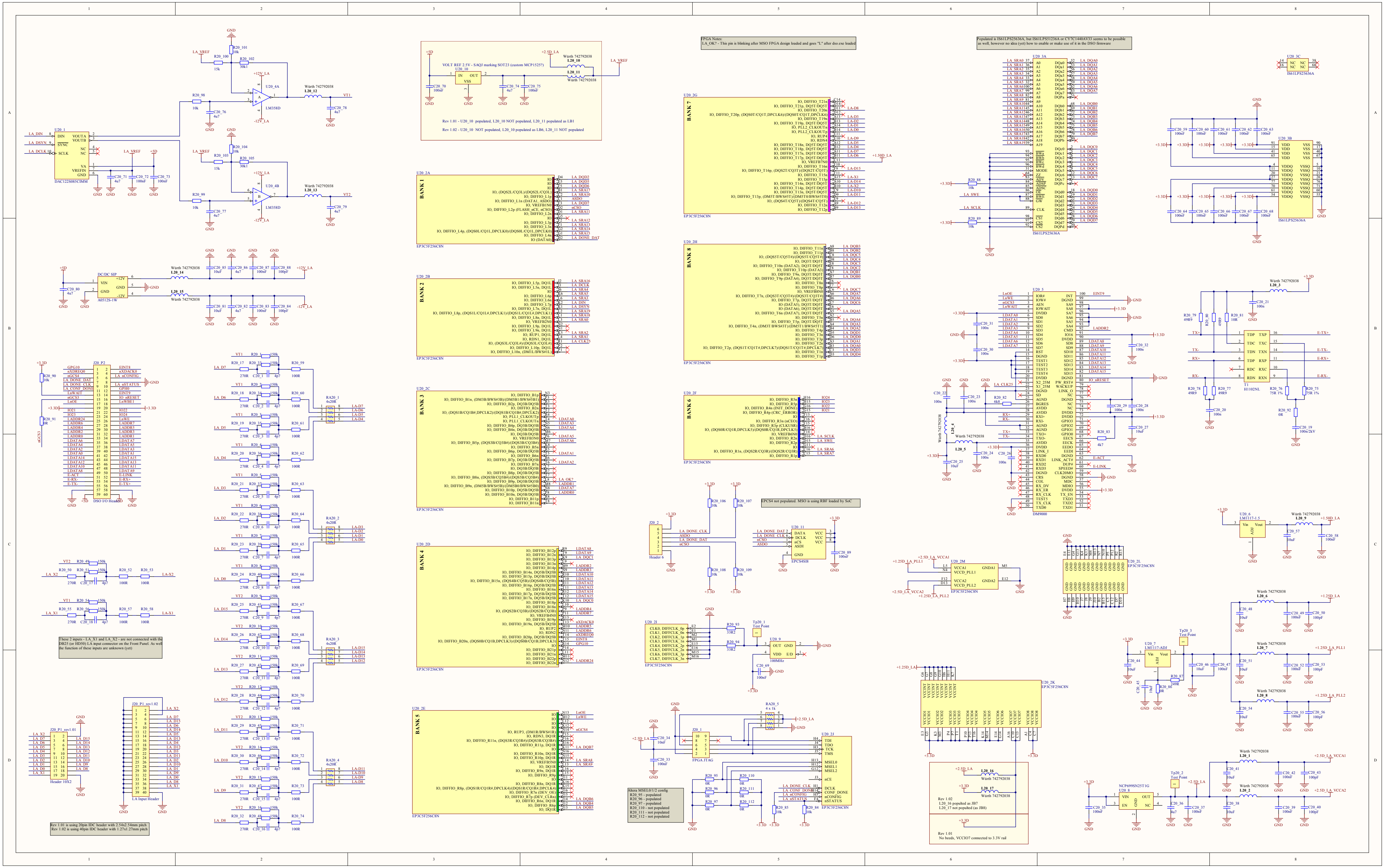
FPGA Notes:
LA_OK? - This pin is blinking after MSO FPGA design loaded and goes "L" after dso.exe loaded
Populated is IS61LPS25636A, but IS61LPS51236A or CY7C1440AV33 seems to be possible as well, however no idea (yet) how to enable or make use of it in the DSO firmware
VOLT REF 2.5V - SAQJ marking SOT23 (custom MCP1525?)
Rev 1.01 - U20_10 populated, L20_10 NOT populated, L20_11 populated as LB1
Rev 1.02 - U20_10 NOT populated, L20_10 populated as LB6, L20_11 NOT populated
These 2 inputs - LA_X1 and LA_X2 - are not connected with the DB25 (or HD50) LA input connector on the Front Panel. As well the function of these inputs are unknown (yet)
Rev 1.01 is using 20pin IDC header with 2.54x2.54mm pitch
Rev 1.02 is using 40pin IDC header with 1.27x1.27mm pitch
EPCS4 not populated. MSO is using RBF loaded by SoC
Altera MSEL0/1/2 config
R20_95 - populated
R20_96 - populated
R20_97 - populated
R20_110 - not populated
R20_111 - not populated
R20_112 - not populated
Rev 1.02
L20_16 populted as JB7
L20_17 not populated (as JB8)
Rev 1.01
No beeds, VCCIO7 connected to 3.3V rail
DAC122S085CIMM
LM358D
A0512S-1W
DSO I/O Header
LA Input Header
Header 10X2
EP3C5F256C8N
IS61LPS25636A
DM9000
H1102NL
EPCS4SI8
FPGA JTAG
LM1117-1.5
LM1117-ADJ
NCP699SN25T1G
Würth 742792038